A 39 GHz Doherty-Like Power Amplifier with 22dBm Output Power and 21% Power-Added Efficiency at 6dB Power Back-Off

Lang Chen, Lisheng Chen, *Member, IEEE*, Depeng Sun, Yichuang Sun, *Senior Member, IEEE*, Yulin Pan and Xi Zhu *Member, Senior Member, IEEE*

***Abstract*—The design of a Doherty-like power amplifier for millimetre-wave (mm-wave) applications is presented in this work. The designed power amplifier employs a novel symmetrical load-modulated balanced amplifier (S-LMBA) architecture. This design is advantageous in minimizing the undesired impedance interaction often encountered in the classic LMBA approach. Such interactions are typically due to the use of a non-50 Ω load at the isolation port of the output quadrature coupler. Moreover, magnitude and phase control networks are carefully designed to generate the specific magnitude and phase information for the designed S-LMBA. To demonstrate the proposed ideas, the S-LMBA is fabricated in a 45-nm CMOS SOI technology. At 39 GHz, a 22.1 dBm saturated output power (P_{sat}) with a maximum power-added efficiency (PAE) of 25.7% is achieved. In addition, 1.68 times drain efficiency enhancement is obtained over an ideal Class-B operation, when the designed S-LMBA is operated at 6 dB power back-off. An average output power of 13.1 dBm with a PAE of 14.4% at an error vector magnitude (EVM_{rms}) above -22.5 dB and adjacent channel power ratio (ACPR) of -23 dBc is also achieved, when a 200 MHz single carrier 64-quadrature-amplitude-modulation (QAM) signal is used. Including all testing pads, the footprint of the designed S-LMBA is only 1.56 mm^2.**

***Index Terms*—Balanced amplifier (BA), CMOS, Doherty-like amplifier, load-modulated balanced amplifier, millimeter-wave technology, monolithic microwave integrated circuit (MMIC), SATCOM.**

I. Introduction

The reduction of energy consumption is a key challenge in many wireless systems. Mobile smartphones can hardly operate the entire day without a recharge. In general, the weight of batteries typically accounts for about 70% of the total equipment carried by professionals like exploration engineers and forestry engineers. Entire new generations of 5G new radio (NR) and SATCOM-On-The-Move (SOTM) are waiting on the sidelines for more energy-efficient electronics that can last weeks instead of days. Generally speaking, in a wireless system, the power amplifier (PA) is one of the most power-hungry components. How to improve the energy efficiency of PAs at both saturated output power (known as P_{sat}) and power back-off (PBO) levels has become a popular research topic in both academia and industry. To accomplish this goal, several innovative design approaches have been recently reported in the technical literature, which are mostly based on either Doherty- or Chireix like architectures [1]-[17].

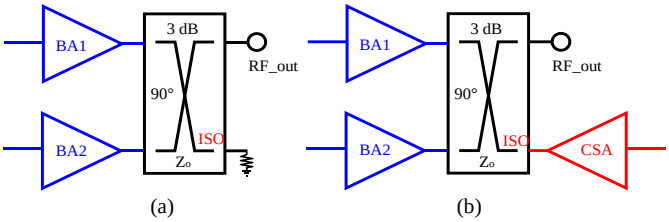

Fig. 1. Simplified block diagram of the classical coupler-based PA architectures, (a) BA, and (b) LMBA.

Recently, a novel concept called load-modulated balanced amplifier (LMBA) has been proposed and feasibility studies of introducing this for CMOS based power amplifier design have been carried out in [18]-[20]. The simplified conceptual schematic of the LMBA principle is shown in Fig. 1. As illustrated, unlike the conventional balanced amplifier (BA) architecture in which the isolated (ISO in Fig. 1) port of the 3 dB quadrature coupler is terminated by a 50 Ω resistor, the ISO port is loaded by a Class-C like amplifier in an LMBA based design, also known as control signal amplifier (CSA) or auxiliary amplifier. The CSA injects a signal to the ISO port. As a result, the load impedances seen by the balanced amplifiers (BA1 and BA2 in Fig. 1) are "modulated", depending on the magnitude and phase relationships between the control-signal path and the BA path. If certain conditions are satisfied, the efficiency of the LMBA can be enhanced at PBO levels [21]-[28]. Compared with PA based on Doherty or Chireix like architectures, the LMBA based design exhibits several intriguing features. Firstly, since a BA based architecture is obtained, outstanding input and output impedance matching over a wide bandwidth is likely to be achieved straightway, even there are undesired impedance variations. Therefore, the

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L. S. Chen and D. Sun are with the Key Laboratory of Analog Integrated Circuits and Systems (Ministry of Education), School of Microelectronics, Xidian University, Xi'an 710071, China and the Hangzhou Institute of Technology, Xidian University, Hangzhou 311200, China. (Email: chen.lisheng@ieee.org).

L. Chen and X. Zhu are with the School of Electrical and Data Engineering, Faculty of Engineering & IT, University of Technology Sydney, Ultimo, NSW 2007, Australia (e-mail: xi.zhu@uts.edu.au).

Y. Pan is with the School of Engineering and Computing, University of Central Lancashire, Lancashire PR1 2HE, UK. (E-mail: YPan15@uclan.ac.uk).

Y. Sun is with the School of Engineering and Technology, University of Hertfordshire, Hatfield AL10 9AB, U.K. (E-mail: y.sun@herts.ac.uk).

proposed design concepts can be widely used in phased array devices. Secondly, as the CSA injects a signal into the isolated port of the quadrature coupler, it naturally offers a three-way power combination that leads to an improved output power. In other words, the load-modulation network is intrinsically included into the output power combining network. Finally, as previously stated and demonstrated in [18]-[27], the proposed design can be used to improve the efficiency of PAs at different PBO levels.

However, based on our reviews of recent relevant literature in the past few years, it can be found that most existing designs are implemented on printed-circuit-board (PCB) technology with discrete transistors. The implementation of this ideas in silicon based technologies, such as SiGe, SOI, and CMOS, has not been extensively verified [18]-[20]. Therefore, the research on silicon based LMBA designs can be considered today in its infancy and, hence, it still faces some major design challenges. Generally, the theoretical analysis given in preceding LMBA design related works (e.g., [21] and [22]) assumes that the quadrature coupler is ideal. However, the on-chip quadrature coupler only has limited isolation. Therefore, the phase and magnitude errors will cause impedance mismatch between the two paths of the quadrature coupler, namely through (THRU) and coupled (COUP) ports. As a result, the output power and efficiency of PA will be deteriorated. Furthermore, since the physical size and the loss of on-chip passive circuits are usually large and high, the output power and efficiency of the PA will also be decreased.

Finally, the efficiency at PBO levels will also be reduced due to the phase or magnitude misalignment between the BA and the CSA. Regarding the magnitude network, an adaptive biasing technique with an equal (i.e., 3 dB) power splitter is a commonly used approach, which has been verified in [18] and [19]. Moreover, for the phase network, both transmission-line (TL) like and digitally controlled vector-summing approaches have been exploited in [18] and [19], respectively. However, it is still unclear if there is any alternative design solution for the magnitude and phase compensation networks. Moreover, in our recently published work in [20], although a relatively high output power is achieved, the efficiency enhancement at 6 dB PBO level is still limited.

In this work, a symmetrical LMBA (S-LMBA) architecture is proposed for on-chip implementation, which can suppress the undesired impedance variations between the BA and control signal path (CSP). In addition, since the BA and CSA are biased in different conditions, a power splitter with unequal outputs and a compensation network are also used in this proposed design.

The rest of this paper is organized as follows. In Section II, the insight of the proposed S-LMBA architecture is explored. In the Section III, every circuit block designed in the proposed S-LMBA will be carefully analysed and discussed. The measurement results of a fabricated prototype in CMOS SOI technology are given in Section IV. Finally, the main conclusions of this work are presented in Section V.

II. Insight of the S-LMBA Architecture

A. Theoretical Analysis

To demonstrate the motivation behind this work, a potential issue of the LMBA based design is illustrated in Fig. 2. It is assumed that a 3 dB quadrature coupler is employed in this design, which can be realized by means of a Z_0-referred coupled-line based solution as proposed in Fig. 2 where Z_0 = 50 Ω is the reference/port impedance. As shown in Fig. 2(a), if the load connected to the ISO port (Port 3) is different from Z_0 (i.e., $Z_3' = k \cdot Z_0$), then the input impedances at Port 2 and Port 4 can be derived from the impedance-matrix [Z] formulation as follows:

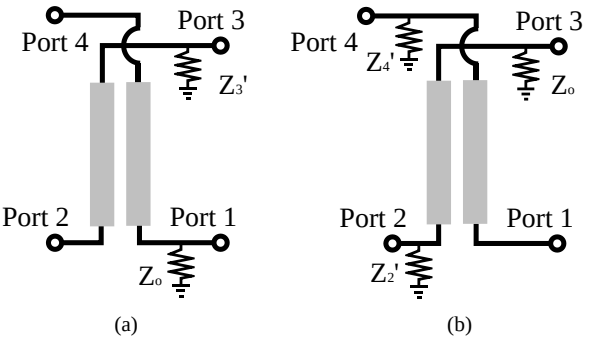


Fig. 2. The simplified schematics used for analysis, (a) ISO port is terminated by a non-50Ω load, and (b) the ISO port is terminated by a 50Ω load.

$$\begin{bmatrix} V_1 \\ V_2 \\ V_3 \\ V_4 \end{bmatrix} = Z_0 \begin{bmatrix} 0 & 0 & -j & -j\sqrt{2} \\ 0 & 0 & -j\sqrt{2} & -j \\ -j & -j\sqrt{2} & 0 & 0 \\ -j\sqrt{2} & -j & 0 & 0 \end{bmatrix} \begin{bmatrix} I_1 \\ I_2 \\ I_3 \\ I_4 \end{bmatrix} \tag{1}$$

where V_i and I_i (i = 1, 2, 3, 4) are the voltage and current waves at the i^{th} port of the coupler, respectively. Note also that [Z] in (1) corresponds to an ideal 3 dB quadrature coupler, which approximates the behaviour of the coupled line coupler in Fig. 2 at its design frequency.

At Port 1 and Port 3, the relationships between voltages and currents are as follows:

$$V_1 = -Z_0 I_1 = -V_1' \tag{2}$$

$$V_3 = -kZ_0 I_3 = -V_3'. \tag{3}$$

According to (1) and using (2) and (3), the following relationships can be established,

$$V_1 = -jV_3' - j\sqrt{2}IV_4' \tag{4a}$$

$$V_2 = -j\sqrt{2}V_3' - jV_4' \tag{4b}$$

$$V_3 = -jV_1' - j\sqrt{2}V_2' \tag{4c}$$

$$V_4 = -j\sqrt{2}V_1' - jV_2'. \tag{4d}$$

From (2), (4a) and (4c) the expressions below are derived:

$$-V_1' = -jV_3' - j\sqrt{2}V_4' \tag{5}$$

$$-kV_3' = -jV_1' - j\sqrt{2}V_2'. \tag{6}$$

By solving (5) and (6), the following relationships are found:

$$jV_1' = -\frac{j\sqrt{2}V_2' + \sqrt{2}kV_4'}{1+k} \quad (7a)$$

$$V_3' = -\frac{\sqrt{2}V_4' - j\sqrt{2}V_2'}{k+1}. \quad (7b)$$

Substituting (7a) and (7b) into (4b) and (4c), respectively, it turns out that

$$V_4 = \frac{j(1-k)V_2' + 2kV_4'}{1+k} \quad (8a)$$

$$V_2 = \frac{j(1-k)V_4' + 2V_2'}{1+k}. \quad (8b)$$

Finally, taking Z_0 into consideration, the following equations for the voltage waves at Port 2 and Port 4 are deduced:

$$V_4 = \frac{j(1-k)I_2 + 2kI_4}{1+k} Z_0 \quad (9a)$$

$$V_2 = \frac{j(1-k)I_4 + 2I_2}{1+k} Z_0. \quad (9b)$$

As shown, an important result is obtained here. When $k \neq 1$, the input impedances at Port 2 and Port 4 are no longer 50 Ω. In other words, if the load impedance at Port 3 is not 50 Ω, the port impedances at Port 2 and Port 4 will be affected. Moreover, there may be an "interaction" between these two ports in terms of impedance variations. It should be noted that the output impedance of the CSA (Class-C like amplifier) usually differs from 50 Ω in practice when it is turned off. As a result, it will have an adverse impact in terms of impedance variations at the Port 2 and Port 4.

Furthermore, as shown in Fig. 2(b), it is also interesting to investigate the case in which both Port 2 and Port 4 are terminated by a same arbitrary load impedance (i.e., $Z_2' = Z_4' = k \cdot Z_0$) and Port 3 is loaded by a Z_0 impedance. The voltage and current relationships at Ports 2-4 in this situation result to be

$$V_3 = -Z_0 I_3 = -V_3' \quad (10a)$$

$$V_2 = -kZ_0 I_2 = -kV_2' \quad (10b)$$

$$V_4 = -kZ_0 I_4 = -kV_4'. \quad (10c)$$

By substituting (10a)-(10c) into (1), the following relationships can be established:

$$V_1 = -jV_3' - j\sqrt{2}V_4' \quad (11a)$$

$$kV_2' = j\sqrt{2}V_3' + jV_4' \quad (11b)$$

$$V_3' = jV_1' + j\sqrt{2}V_2' \quad (11c)$$

$$kV_4' = j\sqrt{2}V_1' + jV_2'. \quad (11d)$$

By solving (11b)-(11d), the expressions below are obtained:

$$V_3' = j\frac{k-1}{k+1}V_1' \quad (12a)$$

$$V_4' = j\frac{\sqrt{2}}{k+1}V_1'. \quad (12b)$$

Finally, by replacing (12a) and (12b) into (11a), the following voltage and current relationship at Port 1 is derived:

$$V_1 = V_1' = Z_0 I_1 \quad (13)$$

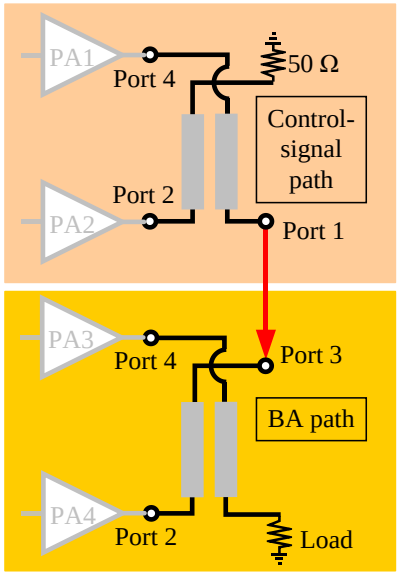


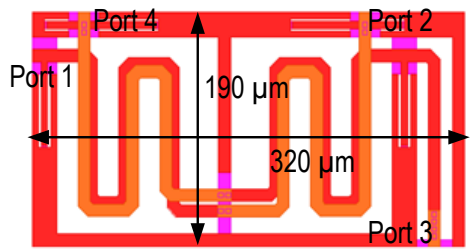
Fig. 3. Output network used for the S-LMBA-based PA design.

As can be concluded from the above analysis, for an ideal 3 dB quadrature coupler, even if Port 2 and Port 4 are loaded with non-50 Ω impedances, the input impedance at Port 1 is still 50 Ω if Port 3 is terminated by a 50 Ω load. Moreover, such input impedance robustness at Port 1 also indicates why a BA based design has superior impedance matching performance with wide bandwidth. To apply this conclusion to the LMBA design, instead of using a single-ended PA structure in the CSP (control-signal path) as in [18] and [19], a BA-like structure is proposed for implementation [29]-[31]. Consequently, the undesired impedance "interaction" between the CSP and BA paths can be minimized.

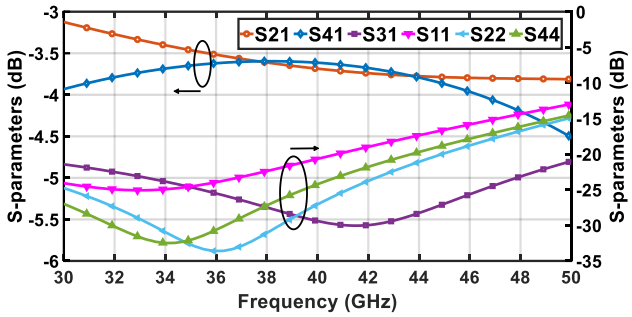
To apply the above-mentioned solution to LMBA based design, a symmetrical network is proposed in Fig. 3. As can be seen, two quadrature couplers are used in this design. The couplers used in the control-signal and the BA paths are placed on top and bottom, respectively. Moreover, Port 1 of the top coupler is connected to Isolation port of the bottom coupler. In addition, the Isolation port of the top coupler is terminated by a 50 Ω load. According to the previous theoretical analysis, the quadrature coupler at the CSP should exhibit a 50 Ω input impedance at Port 1 if its ISO port is terminated by a 50 Ω load, regardless the two Class-C like amplifiers (referred to as PA1 and PA2 in Fig. 3) are turned on or off. Likewise, if Port 1 of the quadrature coupler used at control-signal CSP has a 50 Ω input impedance and is connected with the ISO port of the quadrature coupler of the BA path, the impedance "interaction" among its two branch PAs (designated as PA3 and PA4 in Fig. 3) should be minimized. As a result, the adverse impact on the output power and efficiency due to undesired impedance variations can be minimized as well.

B. Case Studies using EM Simulated Quadrature Couplers

To further validate the above-mentioned analysis, a design example is given here. As far as a Class-C amplifier design is



(a)



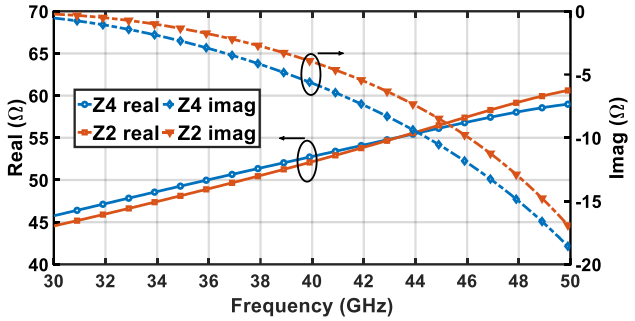
(b)

Fig. 4. Quadrature coupler used for case studies. (a) EM structure. (b) EM simulated results in terms of S-parameters.

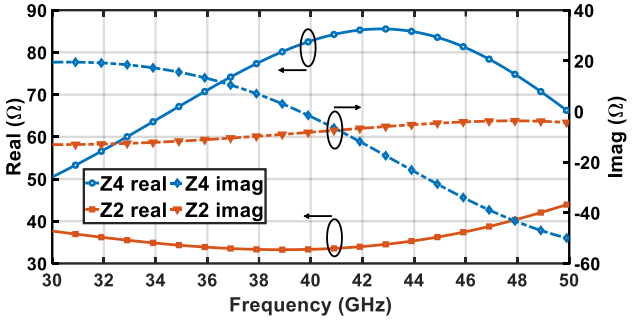
concerned, instead of having an ideal 50 Ω output impedance, the impedance can be modelled as a parallel network that consists of a resistor and a capacitor. Because of this non-50 Ω impedance, the impedances of the quadrature coupler at Port 2 and Port 4 are also varied from the ideal 50 Ω, as it has been analysed in Section II.A. Therefore, the power combining mechanism cannot be operated properly. In order to solve this issue, an additional coupler is used in the CSP, as shown in Fig. 3. In such a way, the output impedances of the Class-C like amplifiers are "separated" from the quadrature coupler used at the BA path.

To prove the claim is valid, three case studies are used here. A quadrature coupler is designed first, whose top-view is shown in Fig. 4(a). To obtain a high coupling factor, a broadside coupled structure is used. The EM simulation tool from Keysight ADS is used. The EM simulated S-parameters are given in Fig. 4(b). Insertion loss (shown as S_{41} and S_{21}) and isolation (shown as S_{31}) are two of the most important design parameters. The output power and efficiency will be decreased dramatically if both of them are not treated thoughtfully. The output of this quadrature coupler needs to be carefully improved at the EM-simulation level first. As can be seen, the designed quadrature coupler has insertion-loss levels of less than 0.7 dB and isolation levels of more than 25 dB across a bandwidth in the range 37 to 44 GHz.

Using the designed quadrature coupler, case studies are conducted. In case 1, the ISO port of the EM simulated coupler shown in Fig. 4(a) is terminated by a 50 Ω load, and the impedance from the COUP (Port 4) and THRU (Port 2) ports are plotted. As can be seen from Fig. 5(a), both the imaginary and real parts of these two impedances are aligned fairly well. However, the situation becomes quite different when the ISO port is terminated by a non-50 Ω load. In this case, a 50 Ω resistor along with a 100 fF capacitor are used. As shown in



(a)



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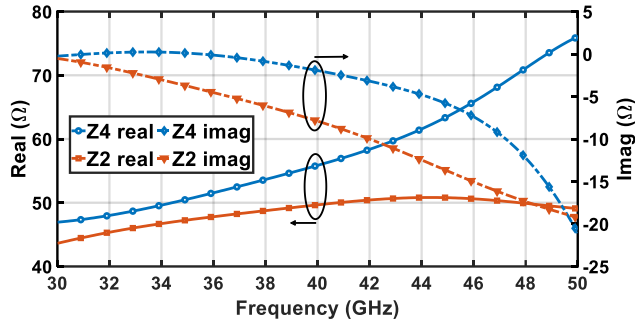


(c)

Fig. 5. EM simulation results under different cases. (a) The ISO port is 50-Ω terminated. (b) The ISO port is terminated by a non-50 Ω load. (c) The load condition used in (b) is applied to the output network shown in Fig. 3.

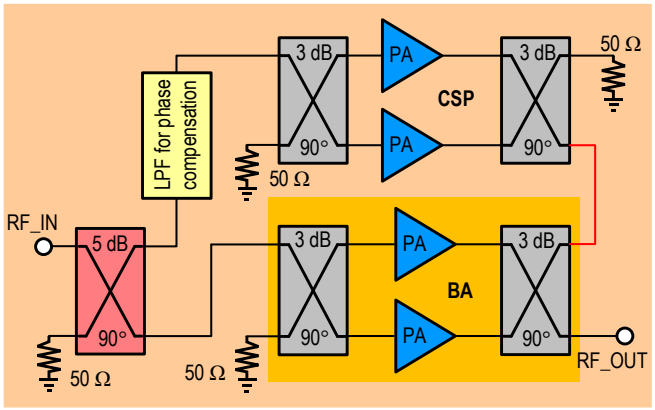
Fig. 5(b), the two impedances are widely separated, which is completely not desirable from power-combining perspective. Furthermore, as presented in Fig. 5(c), the impedance discrepancies between the two ports are significantly reduced by using the structure shown in Fig. 3. Thus, it can be firmly concluded that the presented output network is useful to maintain the correct port impedance for LMBA based design.

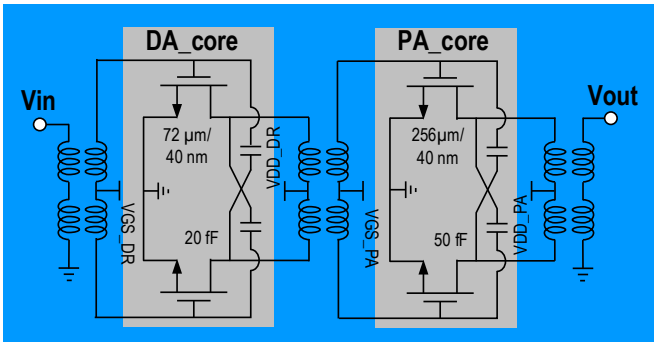
III. Design of the Symmetrical LMBA

To finally demonstrate the proposed S-LMBA architecture can be used in practice, the detailed implementation is given in this section. The overall structure of the designed S-LMBA is given in Fig. 6.

A. Design Considerations of Power Cell and Output Power-Combining Network

To obtain a relatively high output power with decent efficiency for the power-combined PAs, the power cells should also be carefully designed and implemented. Thus, this design





R_{opt}	R_{PAE}	Max P_{out}	Peak PAE
5.6 + j4.3, or 9 Ω || 340 fF	6 + j13.2, or 35 Ω || 250 fF	19.2 dBm	57.8%

Fig. 6. Simplified schematic of the designed S-LMBA.

example starts from power cell design. Both the transistor-level circuit schematic of the differential power cells and the summarized load-pull simulation results are shown in Fig. 6. Each power cell is designed with a driver amplifier (DA). To maintain a low-voltage operation, common-source (CS) configuration is used. In addition, in order to provide high stability and high power gain, capacitive neutralization has also been used in the proposed design. The same arrangement is used for both the BA and CSA designs. The only difference between them is the applied gate bias voltages.

As the design specification of this S-LMBA is to achieve a 22 dBm output power at least, the estimated output power of the power cell from the BA part needs to be around 17 dBm. To meet the overall output power requirements for the S-LMBA, a differential power cell should be used in the BA part. We need to take care of the insertion loss caused by the passive components. Based on our research, a 1.5 dB insertion loss is used in designing the BA. Therefore, an 18.5 dBm output power is required from the differential power cell used in the BA part.

According to our simulation results at 39 GHz, the optimal impedance should be 5.6+j4.3 Ω and the impedance for maximum PAE is 6+j13.2 Ω. To enhance efficiency at a 6 dB PBO level, the targeted impedance should be approximately $4R_{opt}$. Thus, in this design, the output impedance should be modulated from about 35 Ω to 9 Ω.

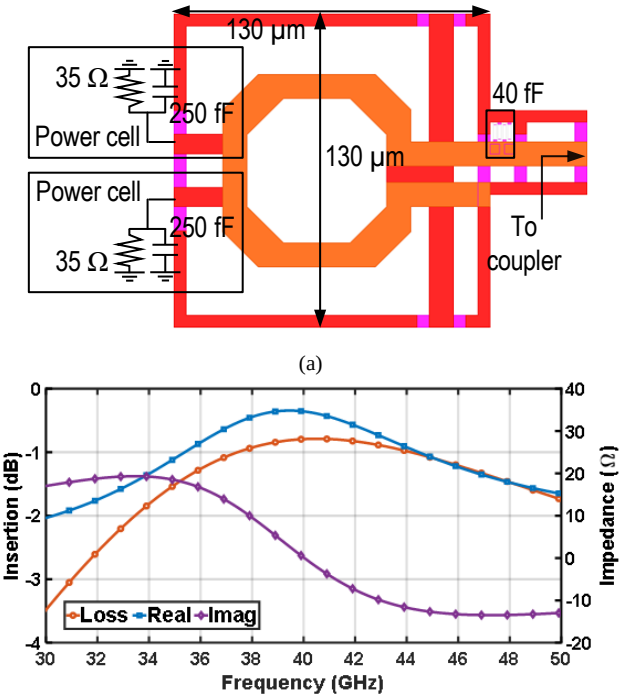


Fig. 7. The transformer used in the output power-combining network, (a) EM structure, and (b) EM simulated results. Note: the coil connected to the PA has an inductance of 125 pH, and the one connected to the coupler has an inductance of 148 pH. The coupling factor is 0.7.

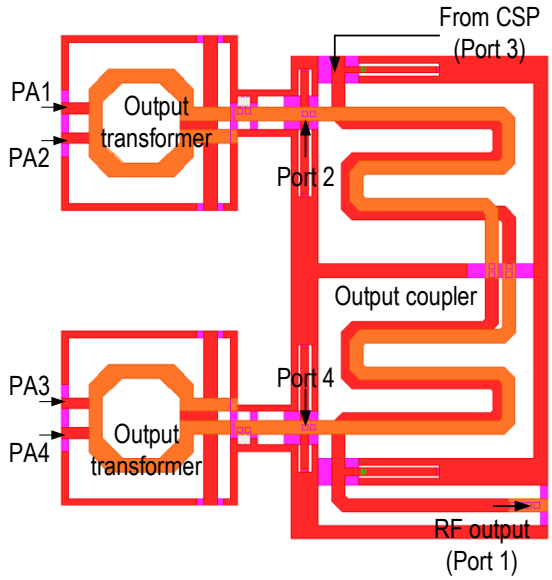


Fig. 8. The output power combining network used in this design.

To ensure the output impedance can be transferred from 35 Ω to 50 Ω, a transformer based balun is used. The top-view of the designed transformer is shown in Fig. 7(a) and the EM simulated results are presented in Fig. 7(b). As can be seen, at 39 GHz, the insertion loss of the transformer is less than 1 dB, and the real and imaginary parts of the impedance well match with the targeted impedance obtained from the load-pull simulation. Once the differential power cell is designed, the quadrature coupler based output power-combining network needs to be implemented, which consists of two transformer

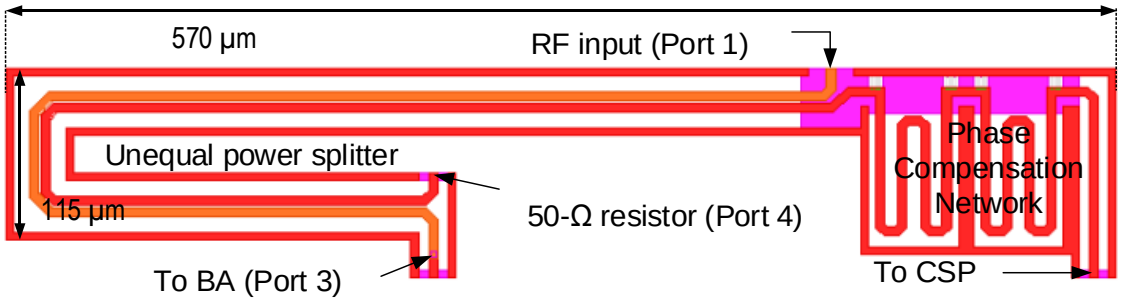
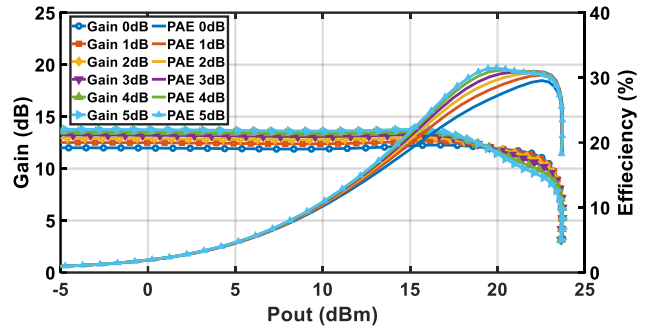
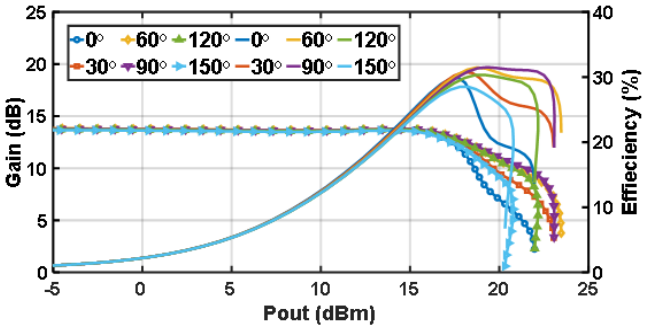


Fig. 9. Overall EM structure. Note: The C-L-C-based cell is used for LPF design (L is 100 pH and C is 20 fF).



(a)



(b)

Fig. 10. Large-signal performance of the designed S-LMBA, (a) different input power split ratio, and (b) different phase relations between the BA and the CSP.

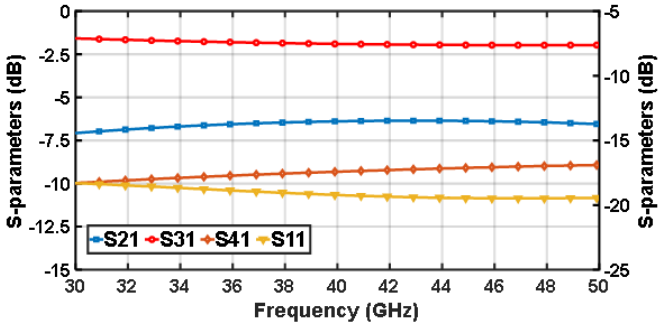
based baluns shown in Fig. 7(a), and a quadrature coupler shown in Fig. 4(a). The top-view of the overall output power-combining network is presented in Fig. 8. The two differential power cells are connected to the Port 2 and Port 4 of the quadrature coupler, the Port 3 is reserved for the connection from the control-signal path, and the Port 1 is used for output of the designed S-LMBA.

B. Design Considerations of Magnitude and Phase Compensation Networks

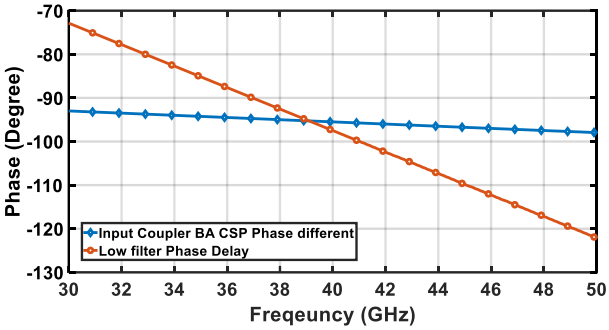
Besides minimizing the adverse impact due to impedance "interaction" in the BA path, according to the theoretical analysis presented in the original LMBA works [21]-[22], the magnitude and phase controls between the control-signal path and the BA path are also very important for efficiency enhancement at PBO level. Therefore, specific networks need to be developed to satisfy certain conditions in this regard. The overall EM structure used in this design is presented in Fig. 9. It consists of two major networks, an unequal power splitter and a phase compensation network. As can be seen, the unequal power splitter is implemented by a coupled-line based structure, and the lumped components are used to build the phase compensation network. It is different from the classical 3 dB quadrature coupler design, it is not necessary to have a strong coupling factor between two coupled lines, and the unequal power splitter is implemented by offsetting two lines. The power-splitting ratio between the CSP and BA parts should be thoughtfully determined through performance optimization so that the amplifier (biased in Class-C) used in the CSP part will only be turned on when the input power is strong enough.

To find the optimal power splitting ratio, the large-signal performance of the proposed S-LMBA is extensively appraised by providing several different power levels into the BA and CSP parts. The detailed simulation results are shown in Fig. 10(a). It can be found that the optimal performance in terms of large-signal gain and efficiency is achieved, when a 5 dB power splitting ratio is used. To make the investigation straightforward to be conducted, an ideal quadrature coupler is used in this design. Thus, the output power at both Through and Coupled ports can be increased or decreased. Unless using the coupling factor of a quadrature coupler, the magnitude difference between these two ports is used to evaluate the power-splitting ratio. Furthermore, as previously mentioned, the phase relationship between the CSA and BA also plays a critical role in this design. To find an optimal phase relationship between the two parts, parametric studies also need to be conducted. The detailed simulation results are shown in Fig. 10(b). As illustrated, the designed S-LMBA achieves an optimized performance, when the phase shifter gives a 60°…90° phase delay.

Compared with the signal at the Through port, the signal generated by the unequal power splitter has a 90° leading phase at the Coupled port. Therefore, compared with the signal at the input of CSA, the signal produced by the phase compensation network will also have a 60°…90° leading phase. Multiple options can be used to apply a 90° delay line at 39 GHz. In contrast to other structures, the transmission-like structure is quite long [18]-[20]. Therefore, a phase compensation network based on the lumped-element structure is used in this design [32]-[35]. Besides, LPF should also be used here as it generates a negative phase shift. In addition, to provide the required phase shift, the LPF is implemented by cascading two unit cells together. Each unit cell consists of a series-connected inductor with two shunt-connected capacitors.



(a)



(b)

Fig. 11. EM simulation results, (a) S-parameters of the unequal power splitter, and (b) phase responses of the LPF and unequal power splitter network.

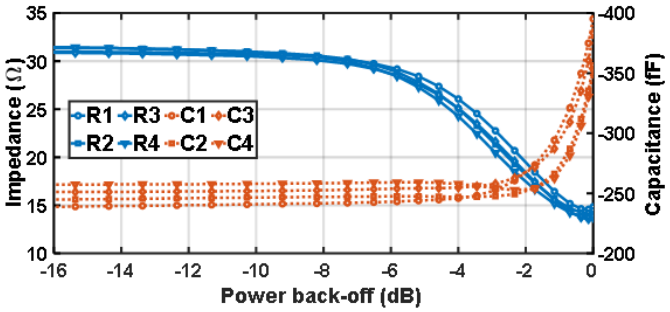


Fig. 12. Simulated load trajectories of the designed power cells. Note: R1…4 and C1…4 are referred to the power cells numbered in Fig. 8.

To obtain the determined power-splitting ratio, multiple design iterations are necessary through extensive EM simulation, so that the required gap between two metal lines can be determined. The simulation results of the designed coupler are presented in Fig. 11(a). As can be seen, the S_{41} is better than 16 dB (known as Isolation), the S_{31} (known as Through) and S_{21} (known as Coupled) are 2.1 dB and 7.2 dB at 39 GHz, respectively. Moreover, a reasonable phase difference between Through and Coupled ports is also achieved, which is less than 5° phase error. In addition, the EM simulation results in terms of phase responses of the LPF as well as the unequal power splitter are shown in Fig. 11(b). As can be found in the simulation results, the lagging phase between the CSP and BA paths is 90° at 39 GHz.

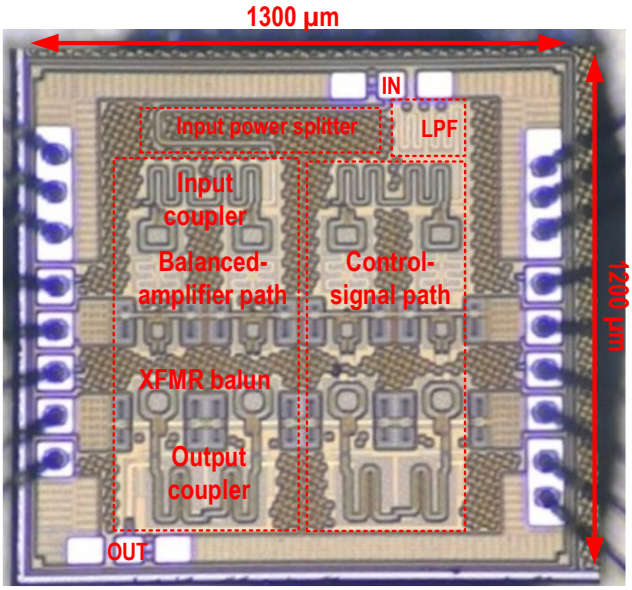


Fig. 13. Die microphotograph of the designed S-LMBA.

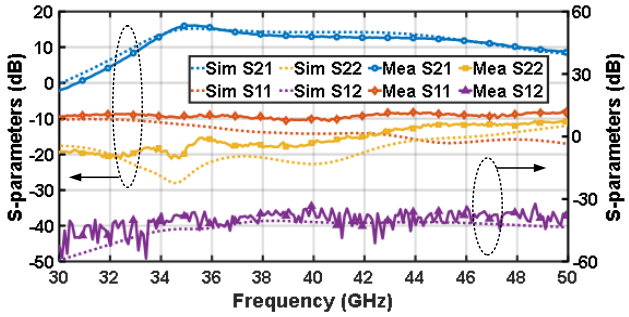
Finally, to verify the above-determined parameters are meaningful in this design, the impedance variations of all power cells are simulated, and the detailed simulation results in terms of impedance variations can be found in Fig. 12. As illustrated, the real part of the impedances of all power cells are shifted to around 13 Ω when they are operated at the saturated power level. These results match the results obtained through the theoretical analysis. It should be noted that the small impedance mismatches between each power cell are due to the magnitude and phase errors between Through and Coupled ports. Moreover, the limited isolation of the coupler might also lead to impedance mismatch.

IV. Measurement Results

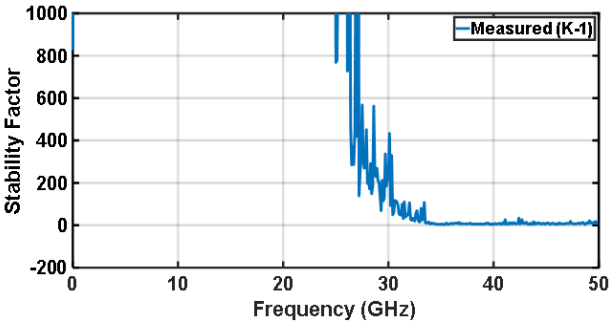
To fully demonstrate the presented theory, the standard 45nm SOI CMOS technology is used to implement the designed 39 GHz S-LMBA. The microphotograph of the fabricated sample is given in Fig. 13. The size of the proposed design is only 1.2 × 1.3 mm^2.

A. Small-Signal Performance

The performance of the designed S-LMBA is evaluated under a small-signal condition first. The measurement procedures will be simply introduced in the following part. On-wafer G-S-G probing method is used for RF measurements. To measure the S-parameters, the N5290A Network Analyzer Millimeter-wave System from Keysight Technologies is used. Since the probe calibration is necessary for ensuring accurate results, a standard Short-Open-Load-Through (SOLT) Calibration is used in our measurement. In Fig. 14(a) the S-



(a)



(b)

Fig. 14. Measurement results under small-signal conditions, (a) S-parameters, and (b) stability factor.

parameters are presented. As depicted, there is a strong concurrence between the measured data and the results obtained through electromagnetic simulation. The measured small-signal gain, the input return loas and the output return loss are 12.8 dB, -10 dB and 18 dB, respectively, at 39 GHz. In addition, to show the designed S-LMBA is unconditionally stable, the stability factor is presented in Fig. 14(b). It should be noted that as the K factor should be greater than 1 for a stable amplifier, the curve of 'K-1' is plotted for better visibility. As can be seen, the 'K-1' curve is always greater than 0 from the DC to 50 GHz, which indicates that the designed amplifier is unconditionally stable.

B. Large-Signal Performance with Continuous-Wave Signal

The performance of the designed S-LMBA is further evaluated with a continuous-wave (CW) large signal. The testbed used for this measurement is shown in Fig. 15. As illustrated, an Analog Signal Generator with a driver amplifier are used to generate a CW input signal with sufficient power. Moreover, two Power Sensors along with a coaxial directional coupler and power meter are used to monitor the power levels at the input and output of the designed S-LMBA.

The measurement results, such as saturated output power (namely P_{sat}), P1 dB, peak PAE, and PAE at 6 dB PBO level, are all presented in Fig. 16. For the main BA path, the supply voltages used for the driver and the output stages are 1 V and 1.2 V, respectively. The same arrangement is also applied for the amplifier in the CSP. The only difference between the CSP and the BA path is that only a 0.1 V gate bias voltage is used in the CSP path, while the 0.21 V and 0.23 V gate bias voltages are used for the driver stage and output stage in the BA, respectively. As illustrated, the designed S-LMBA has a

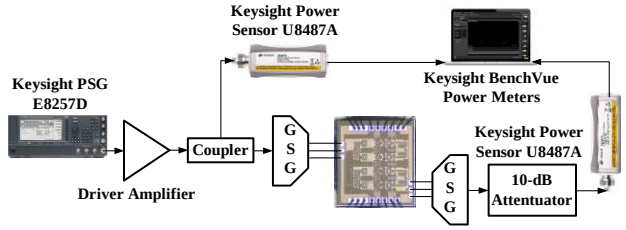


Fig. 15. Test bench used for large-signal CW characterization.

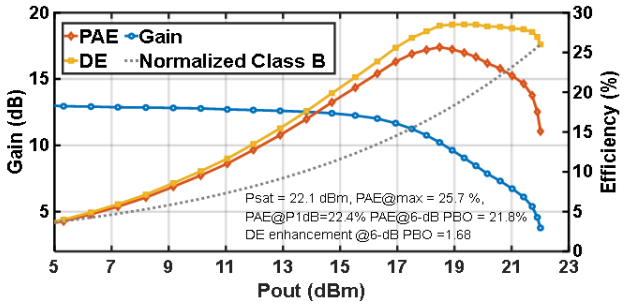


Fig. 16. Large-signal CW measurement results.

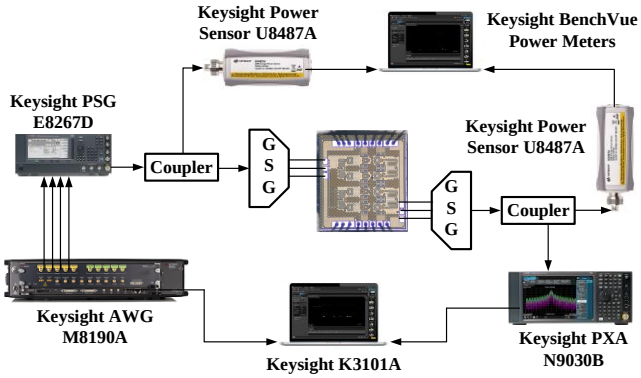


Fig. 17. Test bench used for large-signal modulated-signal characterization.

22.1 dBm P_{sat}, and a 25.7% peak PAE (namely PAE_{max}) at 39 GHz. More importantly, at 6 dB PBO from P_{sat}, the designed S-LMBA obtains a 21.8% PAE. Thus, it achieves 1.68 times drain efficiency (DE) enhancement at 6 dB PBO, compared to an ideal Class-B amplifier.

C. Large-Signal Performance with Modulated Signal

The evaluation of the designed S-LMBA with modulated signals is also carefully conducted. A 64-QAM signal with a 200 MHz modulation bandwidth is selected for testing of the performance in terms of error vector magnitude (EVM) and the adjacent channel power ratio (ACPR). The reason 200 MHz is used mainly is that the equipment is limited. The measurement equipments are connected as shown in Fig. 17. As can be seen, the modulated baseband signal is generated by an arbitrary waveform generator (AWG) first and then is up-converted to 39 GHz by a microwave vector-signal generator.

Subsequently, a modulated signal is introduced into the designed S-LMBA. After that, the amplified signal is down-converted and demodulated by a signal analyser. In addition, power sensors and directional couplers are both applied to

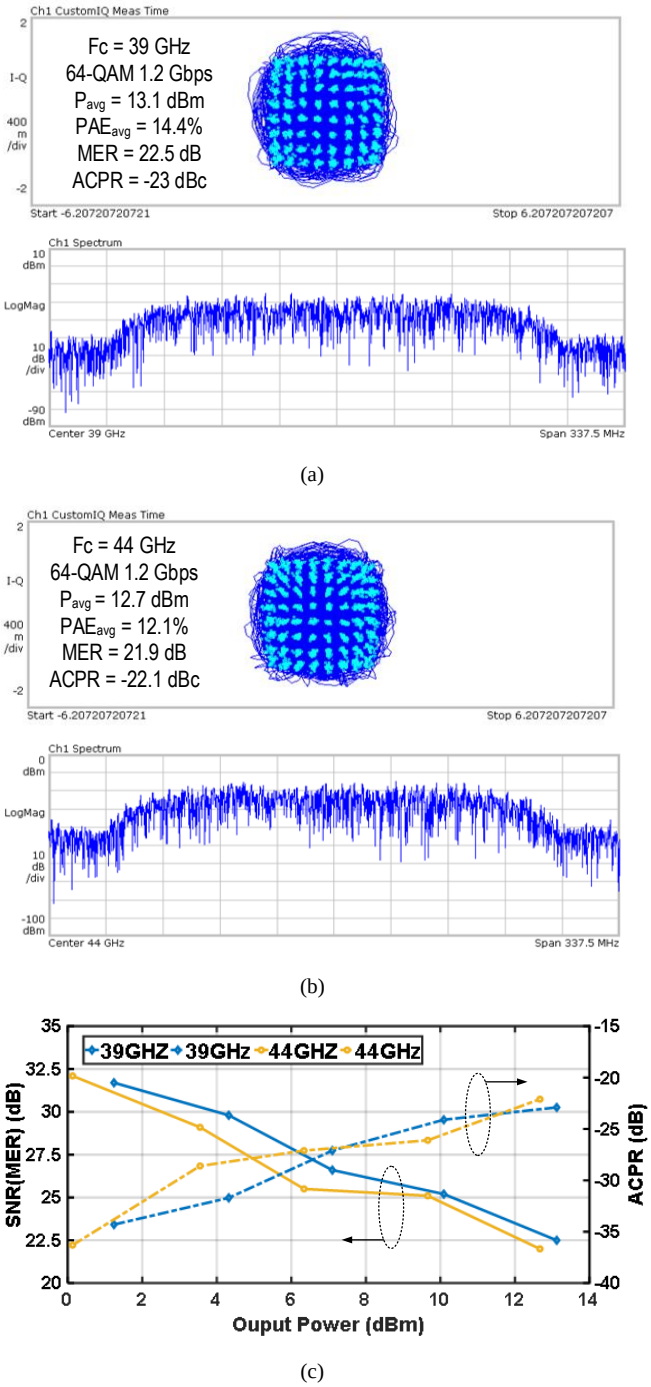


Fig. 18. EVM and ACPR measurement results with modulated signal, (a) performance at 39 GHz, (b) performance at 44 GHz, and (c) performance summary at different PBO levels.

provide more accurate results. Fig. 18 shows the measured EVM and ACPR. An average power (P_{avg}) of 13.1 dBm can be achieved without any digital pre-distortion (DPD). This design can also provide an average PAE (PAE_{avg}) of 14.4% at an EVM_{rms} of -22.5 dB and ACPR of -23 dBc.

D. Comparisons with The Other State-of-the-Art Designs

The performance of the designed S-LMBA is summarized and compared with the other previously published designs in Table I. Since different designs have a different focus, it results in different design strategies, which are well-known as trade-offs. Therefore, it is impossible to draw conclusions by comparing different designs simply. However, the advancement of the presented design still can be seen in the table.

For a reasonable comparison, three most popular technologies, namely bulk CMOS, SiGe heterojunction bipolar transistor (HBT) and silicon-on-insulator (SOI) CMOS, are included. As far as a PA design is concerned, one of the most critical design specifications is the P_{sat}, which is strongly related to the selected devices. Comparing with all three silicon based technologies, the SiGe HBT technology can inherently handle a higher supply voltage. In [12], in order to obtain high output power, a 4V supply voltage is connected. In [12], a Doherty like PA is also designed in SiGe HBT technology. Although a 1.5V supply voltage is used, the P_{sat} is only 17 dBm that is much lower in this work. Further, comparing with the design presented in [6] that is also implemented in 45nm SOI CMOS technology, this work achieves a similar P_{sat} and PAE_{max} using a 1.2 V power supply only, while the design presented in [6] uses a cascode structure with a 2 V power supply. Although it is well-known that the cascode based circuit structure could improve output power by increasing the supply voltage, there might be a reliability issue for a PA design unless a thick-gate device is used. However, this kind of device is not currently available in our design. In addition, it is worthwhile to note that although multiple quadrature couplers are used in this work, the footprint of this design is still compact, which indicates a good power density.

Moreover, from the viewpoint of architectural comparison, both linear and Doherty like designs are included in the table. The concepts of LMBAs have been discussed in several literature [21]-[23], but only a few works related to on-chip implementation [18]-[20]. Compared with the above-mentioned literature as well as the other works published, the presented work achieves the highest efficiency enhancement ratio with excellent power-added efficiency at both saturated and power back-off levels (6 dB). Therefore, it can be concluded that the proposed design is practicable for enhancing the power efficiency of the PA.

V. Conclusions

In this work, the concept of a millimeter-wave Doherty like power amplifier using a novel symmetrical load-modulated balanced amplifier architecture is analyzed and design considerations are provided in detail. To prove the presented theoretical analysis is correct, a prototype is implemented, and fabricated in 45nm SOI CMOS technology. Using a 1.2V supply voltage, the fabricated prototype has been extensively tested under different conditions. Under a small-signal condition, the designed prototype achieves a wideband matching, and a 12 dB gain is obtained at 39 GHz. In addition, excellent large-signal performance, more than 22 dBm saturated output power with more than 25% PAE is achieved. More importantly, the designed prototype shows good linearity as well. The measured EVM_{rms} is less than -22 dB, when a single-carrier 64-QAM signal with 200 MHz bandwidth is applied. Therefore, it is believed that the presented S-LMBA

TABLE I

PERFORMANCE COMPARISONS OF THE DESIGNED S-LMBA AND THE OTHER MM-WAVE STATE-OF-THE-ART DESIGNS IN SILICON-BASED TECHNOLOGIES.

	LMBA			Doherty		Linear	
	This work	[18] Chappidi IMS 20	[19] Qunaj ISSCC 21	[6] Huang ISSCC 21	[12] Hu JSSC 19	[10] Vigilante JSSC 18	[9] Chappidi JSSC 17
Tech.	45-nm SOI	65-nm CMOS	28-nm CMOS	45-nm SOI	0.13-µm SiGe	28-nm CMOS	0.13-µm SiGe
Arch.	Unequal power splitter	Equal power splitter with TL phase shifter	Equal power splitter with VS phase shifter	Coupler-based Doherty	Reconfigurable Doherty	Wideband Class AB	Frequency Reconfigurable
VDD (V)	1.2	1.1	1	2	1.5	0.9	4
Freq. (GHz)	39	33	36	42.5	37	40	40
Gain (dB)	12.8	10	18	N/A	16.6	20.8	18
P_{sat} (dBm)	22.1	20	22.6	21.8	17	15.9	23.6
PAE_{max} (%)	25.7	22.3	32	27.8	21.4	18.4	25
$PAE_{6\text{-dB PBO}}$ (%)	19	16.2*	24.2	19.6	12.6	N/A	N/A
Efficiency enhan. ratio	1.68	1.5	1.5	1.44	1.46	N/A	N/A
Mod. scheme	64-QAM	64-QAM	64-QAM	64-QAM	64-QAM	64-QAM	64-QAM
Data rate (Gb/s)	1.2[#]	6	18	3	3	1.5	3
EVM_{rms} (dB)	-22.5	-27	-25.1	-25.2	-30.3	-25[^]	-21.7**
P_{avg} (dBm)	13.1	10.6	15.5	12.6	9.5	10.1[^]	11.7**
PAE_{avg} (%)	14.4	12.1	20	15.6	19.2*	5.8[^]	8.3**
Area (mm^2)	1.56	1.47	1.44	2.28	1.76	N/A	1.02

Note: [#]limited by the analysis BW of spectrum analyser, *last-stage drain/collector efficiency, **graphical estimation, ^@34 GHz. **@ 4-dB PBO level.

architecture has the potential to be used for power amplifier design in the 5G era and beyond.

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Lang Chen received the B.S. degree in microelectronics from the University of Electronic Science and Technology of China (UESTC), Chengdu, China, in 2014, the M.S. degree in microelectronics from the University of Chinese Academy of Sciences (UCAS), Beijing, China, and The Institute of Microelectronics of Chinese Academy (MECAS), Beijing, in 2017. He received the Ph.D. degree from the University of Technology Sydney, Australia, in 2022.
His research interest includes RF/millimeter-wave (mm-wave) integrated circuits.

Lisheng Chen (Member, IEEE) received the B. Eng. degree in electrical engineering from the University of Sydney, Australia, in 2016 and the Ph.D. degree from the University of Technology Sydney, Australia, in 2022. From 2022-2023, he worked as a Post-doctoral Research Fellow with the School of Electrical and Data Engineering, University of Technology Sydney (UTS). He is currently a Professor with Xidian University.
His research focuses on RF/millimeter-wave integrated circuits.

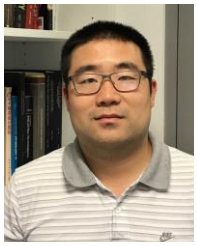
Depeng Sun received B.S., and Ph.D. degrees in microelectronics and solid-state electronics from Xidian University, Xi'an, China, in 2012, and 2022, respectively. He is currently an Assistant Professor at Xidian University, Xi'an, China. His main research interests include RF and mixed-signal integrated circuit design.

Yichuang Sun (Senior Member, IEEE) received the B.Sc. and M.Sc. degrees from Dalian Maritime University, Dalian, China, in 1982 and 1985, respectively, and the Ph.D. degree from the University of York, York, U.K., in 1996, all in communications and electronics engineering.

He is currently a Professor of Communications and Electronics, and the Head of the Communications and Intelligent Systems Research Group and the Electronic, Communication and Electrical Engineering Division, School of Engineering and Computer Science, University of Hertfordshire, U.K. He has published over 330 articles and contributed ten chapters in edited books. He has also published four text and research books: *Continuous-Time Active Filter Design* (CRC Press, USA, 1999), *Design of High Frequency Integrated Analogue Filters* (IEE Press, U.K., 2002), *Wireless Communication Circuits and Systems* (IET Press, 2004), and *Test and Diagnosis of Analogue, Mixed-Signal and RF Integrated Circuits: The Systems on Chip Approach* (IET Press, 2008). His research interests include wireless and mobile communications, RF and analogue circuits, microelectronic devices and systems, machine learning, and deep learning. He

was a Series Editor of *IEE Circuits, Devices and Systems Book Series: Design of High Frequency Integrated Analogue Filters* from 2003 to 2008. He has been an Associate Editor of IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS—I: REGULAR PAPERS from 2010 to 2011, from 2016 to 2017, and from 2018 to 2019. He is also an Editor of *ETRI Journal*, *Journal of Semiconductors*, and *Journal of Sensor and Actuator Networks*. He was the Guest Editor of eight IEEE and IEE/IET journal special issues: High-Frequency Integrated Analogue Filters in IEE Proceedings Circuits, Devices and Systems in 2000, RF Circuits and Systems for Wireless Communications in IEE Proceedings Circuits, Devices and Systems in 2002, Analogue and Mixed-Signal Test for Systems on Chip in IEE Proceedings Circuits, Devices and Systems in 2004, MIMO Wireless and Mobile Communications in IEE Proceedings Communications in 2006, Advanced Signal Processing for Wireless and Mobile Communications in IET Signal Processing in 2009, Cooperative Wireless and Mobile Communications in IET Communications in 2013, Software-Defined Radio Transceivers and Circuits for 5G Wireless Communications in IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS—II: EXPRESS BRIEFS in 2016, and the 2016 IEEE International Symposium on Circuits and Systems in IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS—I: REGULAR PAPERS. He has also been widely involved in various IEEE technical committee and international conference activities.

Yulin Pan is currently pursuing her B.Eng. degree in Electronic Engineering at a university in Lancashire, UK. She participated in a summer research program in 2023, under the guidance of Dr. Xi Zhu from the University of Technology Sydney, focusing on the design of millimeter-wave transmitters in silicon-based technologies. Her research interests include RF and mixed-signal integrated circuit design.



Xi Zhu (Member, IEEE) received the B.Eng. and Ph.D. degrees in electronic engineering from the University of Hertfordshire, Hatfield, U.K., in 2005 and 2008, respectively.

Since 2016, he has been a Lecturer with the School of Electrical and Data Engineering, University of Technology Sydney (UTS), Ultimo, NSW, Australia. He has authored or coauthored more than 100 articles in international journals and conferences. His current research interests primarily focus on the design of analog/mixed-signal integrated circuits and radio frequency integrated circuits for wireless communications.

Dr. Zhu organized and co-chaired the special session “Millimeter-Wave Integrated Circuits Design in CMOS and SiGe Technologies” in IEEE International Symposium on Circuits and Systems (ISCAS) 2019 and serves as a member of the Technical Review Board for several IEEE journals and conferences, including ISCAS that is the flagship conference organized by the IEEE CAS-S. He is currently an Associate Editor of the IEEE TCAS-II, IEEE ACCESS and IET Microwaves, Antennas & Propagation. He is also a member of the IEEE CAS-S Analog Signal Processing Technical Committees (ASPTC).