SINGLE-BIT FEEDBACK AND LIMITED ACCELERATION MECHANISM IN ATM NETWORKS

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ABSTRACT

This paper presents a new feedback congestion control mechanism for the flow control in ATM networks. This new mechanism operates based on a statistical feedback scheme. By limiting cell transmission accelerations, the new mechanism can guarantee that there are no switch buffer overflows . Analysis and simulation results show that the proposed mechanism is effective.

1. INTRODUCTION

Congestion control is critical in ATM networks. When two bursts arrive simultaneously at a node, the queue lengths may become large very fast resulting in buffer overflow. Also, the range of link speeds is growing fast as higher speed links are being introduced in slower networks of the past. At the points, where the total input rate is larger than the output link capacity, congestion becomes a problem. In order to meet the quality of service requirements, the queue service discipline should serve the guaranteed traffic in preference to the best-effort traffic[1].

Congestion-control schemes with only a single bit to convey feedback information have been used in the past for controlling congestion due to burst data traffic or multimedia traffic[2]. Considerable work has been done recently by several authors on the use of feedback for congestion control and flow control in ATM networks[3~8].

In this paper, we propose a new flow control mechanism which is based on quota single-bit feedback scheme in [6] and can guarantee cell loss free during a congestion. The proposed mechanism is a cell loss free mechanism based on statistical single-bit feedback scheme[5,6,7]. The previous similar cell free mechanism is based on an explicit feedback – continuation single-bit feedback scheme which was proposed in [8]. Simulation results show that the proposed mechanism is effective.

The rest of this paper is organised as follows. In Section 2 we describe the existing single-bit feedback schemes. Section 3 presents a new flow control mechanism. Analysis and simulation results are presented in Section 4 and a conclusion of this work is presented in Section 5.

2. SINGLE-BIT FEEDBACK

Single-bit feedback uses one bit in the cells which pass through the switches to indicate the elements along the flow path is congested or not. The source will increase or decrease its rate by some pre-decided rule upon receive the feedback. Some scheme was proposed to set the congestion bit by using two thresholds or by using random number, but they either couldn't provided accurate congestion information or may have some random statistic mistakes.

Queue length in the switch buffers is often used as the indication of congestion. Some other parameters can also be used for the same purpose. For the sake of simplicity, through out this section, we use queue occupancy as an example of congestion parameters.

2.1 "Go or Stop" Single-bit Feedback

The use of a single-bit feedback scheme for congestion control was initially proposed by Ramakrishnan and Jain (1990) [3] and is often referred to as the DECbit scheme. Another single-bit feedback-control scheme has been proposed by Mitra and Seery (1993)[4]. In both, the congestion bit in a cell is set according to the instantaneous queue-occupancy level comparing with a particular threshold. This approach to generate the single-bit feedback is called the threshold approach.

A typical scheme of the threshold approach is hysteresis algorithm[5]. In the hysteresis algorithm, two thresholds (a higher threshold and a lower threshold) are used . A bit is set 1 after the average queue occupancy has crossed above the higher threshold. Once this threshold is crossed, the bit in a cell header remains set 1 until the average queue occupancy has crossed below the lower threshold.

There exist some similar schemes of threshold approach. Some schemes replace the two thresholds in the hysteresis algorithm by only one threshold. That means to choose the higher threshold the same as the lower threshold. Some schemes replace the average queue occupancy by cell arriving rate or by other parameters which can reflect the state of congestion at the bottleneck.

The single-bit feedback generated by the threshold approach is always used as a "go or stop" signal[1,3,4,5].

2.2 Continuation Single-bit Feedback

Though the "go or stop" single-bit feedback scheme is simple and easy to be implemented, the receiver of the signal some time can not keep its transmission speed, for it often either accelerates (when a "go" signal is received) or decelerates (when a "stop" signal is received) its transmission speed. For this reason, the "go or stop" single-bit feedback scheme can hardly provide an ideal quality of service.

A single-bit feedback scheme which can provide the signal of "continuation" was proposed in [6].

The scheme is called "continue single-bit feedback scheme". Two thresholds (higher threshold and lower threshold) are used in the scheme. The congestion bit is set as follows:

- If the queue occupancy level is higher than the higher threshold, the congestion bit is set to 1;
- If the queue occupancy level is lower than the lower threshold, the congestion bit is set to 0;
- If the queue occupancy level is between the higher threshold and the lower threshold, the congestion bit is set opposite to the previous congestion bit. That is, the current congestion bit is set to 0 if the previous congestion bit was set to 1, and it is set to 1 otherwise. If the current congestion bit is the first one, then simply set it to 1.

The continuation single-bit feedback can be used as an indication of "continuation", "acceleration" or "deceleration". When a source receives a congestion bit of 0 following another bit of 0, the source is supposed to be allowed to accelerate its sending. Otherwise, when a source receives a congestion bit of 1 following another bit of 1, the source is expected to decelerate its sending. When a source receives a congestion bit of 1 following another bit of 0, or receives a congestion bit of 0 following another bit of 1, the source is supposed to allow to keep its sending speed. By this way, congestion may be avoided or limited and the transmission speed can be more smooth.

2.3 Statistical Single-bit Feedback

There exist some statistical single-bit feedback schemes, like the KM-S scheme described by Kanakia et al. [5,7] and the Quota scheme[8], in which the single bit is used to convey more accurate information about the queue occupancy and not just whether it is above/below a particular threshold. This is motivated by the key observation that although there is only one bit available per cell, a receiver gets to observe the bits set in a number of cells received over time. Thus a switch can convey more accurate information about any slowly varying quantity, such as the queue size or the link utilisation. The receiver can apply a suitable filter to the stream of received bits to extract the appropriate information

and send it back to the source, which then utilises the information to control the cell sending rate.

There are two main approaches to generate statistic single-bit feedback: the Random approach and the Quota approach.

2.3.1 Random approach

A single bit could be used to encode queue-occupancy information as that described below. Say that a switch has a single queue for waiting cells. Define multiple threshold levels to distinguish various levels of queue occupancy, and associate with each of these regions a probability P_i . Before transmitting each cell, the switch obtains a probability P which reflects the levels of queue occupancy , and generates a random real number Q between 0 and 1. The congestion bit will be set 1 if $P > Q$, otherwise the bit will be set 0. This approach is called Random approach[5,7].

2.3.2 Quota approach

Another approach to generate single-bit feedback that would convey the statistical information but no any random factor in Quota approach[8]. It is described below. Assume that we need to set the congestion bit based on queue occupancy. Let A_i denote the queue occupancy level at cycle i (A_i is between 0 and 1). Let B_i denote the congestion bit set in cycle i (B_i should be 0 or 1). Let Q_i denote a series variable, which is called quotas. A_i is set depending on the queue occupancy, while B_i and Q_i is set as follows:

$$Q_0 = 0;$$
$$\text{if } (A_i + Q_i > 0.5) \; \{ \; B_i = 1, Q_{i+1} = A_i + Q_i - 1 \; \};$$
$$\text{if } (A_i + Q_i \leq 0.5) \; \{ \; B_i = 0, Q_{i+1} = A_i + Q_i \; \}.$$

The receiver can do statistics on the feedback during a given period to evaluate the average queue occupancy level, as such B_i conveys the statistical information.

3. LIMITED ACCELERATION MECHANISM

In this section, we provide a new flow control mechanism, called Quota Limited Acceleration Mechanism. The new mechanism adopts the information provided by the quota approach

single-bit feedback to adjust the source's sending speed.

Assume that the transmission capabilities at a switch S is C (cells/second), and there are n sources $S_1, S_2, ..., S_n$ connecting to S. Assume that the amount of buffers at S is M (cells). Assume the delay of the feedback (from the moment a congestion bit is set to the moment it comes into effect) is T (seconds). Assume every switch does statistics on the congestion bits that it received during the periods of last k cycles (there is one congestion bit coming in each cycle), and each cycle lasts h seconds. Normally, the a congestion situation can be detected by the congestion bit receiver in $T + h * k /2$ seconds after it appears. Let L denotes the time $T + h * k /2$ seconds, which is the average interval between the time that congestion situation appears and the moment that the congestion situation is detected by a forward switch. There are two thresholds, higher threshold Th_1 and lower threshold Th_2 , are used in each switch to decide the transmission speed. For different message stream, the length of the periods to do statistics on congestion bits and the thresholds to decide the transmission speed may different from others.

Assign the transmission capabilities of switch S to its sources $S_1, S_2, ..., S_n$ evenly (or unevenly, according to their priorities), say C /n for each of $S_1, S_2, ..., S_n$. Let C_i denote the part of transmission capabilities of being assigned to S_i . In this case, C_i equals C /n and is called the quota of S_i. Two acceleration limits A and B are decided according to the parameters T, C, n, C_i ($i=0,1,...,n$).

For each switch S_i ($i=0,1,...,n$), if its transmission speed is lower than its quota C_i , the switch S_i is allowed to increase its sending speed with an acceleration no more than A. If switch S_i has just evaluated the congestion level in the forward switch less than Th_2 and its transmission speed is not less than its quota C_i, it is allowed to increase its sending speed with an acceleration no more than B. If switch S_i has just evaluated the congestion level in the forward switch larger than Th_1 and its sending speed is over its quota C_i, it is

expected to adjust its sending speed to its quota C_i immediately. Otherwise, if switch S_i has just evaluated the congestion level in the forward switch between Th_1 and Th_2 or its sending speed is not over its quota C_i, it is allowed to keep its current sending speed.

We can choose the parameters deliberately so that the cell loss free can be guaranteed and that the transmission capacity of the network will not be waste. If the higher threshold Th_1 is low enough and the acceleration B is small enough, the cell loss will be avoid for the reason that the buffer in the forward switch will never overflow. If the lower threshold Th_2 is high enough and the accelerations A and B is big enough, the transmission capacity can be used fully. This can be see in next section.

The parameters in such a mechanism are suggested as follows:

$$Th_1 = 1/3 \quad\dotfill(1)$$

$$Th_2 = \frac{3n}{2} * ((1-\frac{1}{n}) * C * L)^2 /M^2$$
$$+ (1-\frac{1}{n}) * C * L /M \dotfill(2)$$

$$C_i = C / n \quad\dotfill(3)$$

$$A = B = M * Th_1 / (n * L^2)$$
$$= M /(3 * n * L^2) \dotfill(4)$$

For the reason of $Th_1 \geq Th_2$, to meet the formula (1) and (2) M should satisfy the formula as follows:

$$M \geq \frac{9n}{2} * ((1-\frac{1}{n}) * C * L)^2 /M + (1-\frac{1}{n}) * C * L$$

4. ANALYSIS AND SIMULATION

4.1 Analysis

Theorem 1: If the parameters satisfy (1) and (4) described in the previous sub-section, the proposing mechanism is cell-loss free.

Proof of theorem 1: We consider the worst case the mechanism could meet, in which the queue occupancy (buffer occupancy) in S should be

highest. In this case, the transmission rates of the sources rise up with the full acceleration until a "deceleration" signal comes into effect.

When the buffer occupancy of S is nil, the total cell coming rate of S will be not larger than C. If each source of S raises its rate with an acceleration of A, the total cell coming rate will rise up with an acceleration of $n*A$. Assume it takes t seconds to fulfill the buffer as much as $Th_1 * M$. Then we have:

$$Tt_1 * M = \int_0^t (C + n * A * x)dx - C * t$$
$$= \frac{1}{2} n*A*t^2$$
$$t = \sqrt{2 * M / (3 * n * A)}.$$

After the buffer occupancy reaches $Th_1 * M$, S will set the congestion bits to reflect the situation, and it will take another L seconds to be recognized by the forward switch and to react, i.e. the total cell coming rate is dragged back to C. During this time, the amount of buffer occupancy will reach no higher than:

$$\int_0^{t+L} (C + n * A * x)dx - C * (t+L)$$
$$= \frac{1}{6} * M / L^2 * (t + L)^2$$
$$\leq \frac{1}{6} * M / L^2 * 2*(t^2 + L^2)$$
$$= M$$

This means that the buffer will by no means overflow, i.e. the proposed mechanism is cell-loss free.

Theorem 2: If the parameters satisfy (2), (3) and (4) described in the previous sub-section, the proposed mechanism would not waste any transmission capabilities, i.e., if the total transmission request of the sources of S is not less than C, S can receive enough cells to keep its transmission rate at C.

Proof of theorem 2: Again, we consider the worst case which may appear on the mechanism. It is that when the buffer occupancy drops down to

Th_2*M and S sets out to set the congestion bit to reflect the situation, only one of its sources, say S_i, is sending cells to S and the current cell coming rate is only $C_i=C/n$.

If the transmission request of S_i is not less than C, let's assume that it takes t seconds for the cell coming rate of S to reach C. Then, we have:

$$C = C_i + A * (t - L)$$

During the period from the buffer occupancy of S dropping down to $Th_2 * M$, to the cell coming rate of S to reach C, the total amount of cells that come to S should not be less than:

$$C_i * t + \frac{1}{2} * A * (t - L)^2$$

We have:

$$Th_2 * M = \frac{3n}{2} * ((1-\frac{1}{n}) * C * L)^2 / M$$

$$+ (1-\frac{1}{n}) * C * L$$

$$= \frac{1}{2} * (C - C_i)^2 / A + (C - C_i) * L$$

$$= \frac{1}{2} * (C - C_i) * (t - L) + (C - C_i) * L.$$

The total amount of cells that S could provide to be transmitted during the period should be no less than:

$$Th_2 * M + C_i * t + \frac{1}{2} * A * (t - L)^2$$

$$= \frac{1}{2} * (C - C_i) * (t - L) + (C - C_i) * L$$

$$+ C_i * t + \frac{1}{2} * (C - C_i) * (t - L)$$

$$= C * t$$

This means that S can provide enough cells to keep its transmission rate at C even during the worst period (of t seconds).

4.2 Simulation Results

The simulation results shown in figure 1 have illustrated the relationship between transmission request, transmission rate and buffer occupancy. In the simulation, the switch S has three sources which is in turn generated from a switch. We let the transmission request of each source change rapidly so that we can display its wave-form under the worst case. The parts we display in the figure include 200 cycles, where a single congestion bit is generated at every cycle.
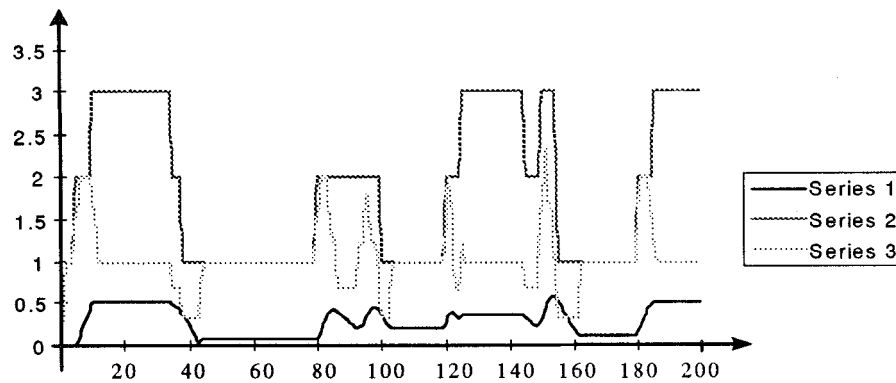

Figure 1: Graphical representation of the relationship between transmission request, transmission rate and buffer occupancy

In figure 1, Series 1 represents the buffer occupancy level in switch S. Where 1 means the buffer being full while 0 means the buffer being empty. Series 2 denotes the total transmission request of the three sources of the switch S. The request of each switch can be 1 or 0, where 1 means the source being ready to send cells (it has the transmission request) while 0 means the source having nothing to send at the moment (it hasn't transmission request). Series 3 denotes the total

cell coming rate of the switch S. The transmission rate of each source can be between 0 and 1. When a source has not transmission request, its transmission rate is zero.

From figure 1, it is clearly shown that the buffer has never been filled, however if the source keeps transmitting, the buffer will always contain some data. This means that the buffer has never overflowed, which implies that no cell was lost, and the transmission capabilities of switch S has never been wasted for the reason that the buffer has never been emptied.

5. CONCLUSION

In this paper, we have proposed a new mechanism, which is based on the quota feedback scheme. The proposed mechanism is the cell loss free mechanism based on statistical single-bit feedback scheme. We have also presented both analysis and simulation results which show that our new mechanism can guarantee cell loss free and work effectively.

REFERENCE

1. Iliadis, I.: A new feedback congestion control policy for long propagation delays. IEEE Journal on Selected Areas in Communications. Vol. 13, No. 7 (1995) 1284-1295.
2. Jain, R.: Congestion control and traffic management in ATM networks: Recent advances and a survey. Computer Networks and ISDN Systems. Vol.28, No.13 (1996) 1723-1738.
3. Ramakrishnan, K. K., Jain, R.: A binary feedback scheme for congestion avoidance in computer networks. ACM Trans Computer Systems. Vol. 8 (1990) 158-181.
4. Mitra, D., Seery, J.: New adaptive algorithms for windows and rates in high speed wide area networks based on periodic 1-bit explicit feedback. Technical Report. AT&T Bell Labs, Murray Hill, NJ, (1993).
5. Kanakia, H., Mishra, P. P.: Packet video transport in ATM networks with single-bit feedback. Multimedia Systems. Vol. 4, No. 6 (1996) 370-380.
6. Liu, H., Song, E., Sotudeh, R.: Single-bit feedback scheme for multimedia transport in ATM networks. Proceeding of 6th International Conference on Intelligent Systems. Boston, USA. (June 11-13, 1997), pp. 28-31.
7. Kanakia, H., Reibman, A. R.: An adaptive congestion control scheme for real-time pack video transport. Proceedings of ACM SIGCOMM. San Francisco, CA, (1993). IEEE/ACM trans. Networking. No. 6 (1993) 671-682.
8. Liu, H., Song, E., Sotudeh, R.: Limited acceleration mechanism for cell loss free flow control in ATM networks, Proceeding of Third Annual International Computing and Combinatorics Conference. Shanghai, China. (August 20-22, 1997).

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