Low-Cost and High-Reduction Approaches for Power Droop During Launch-On-Shift Scan-Based Logic BIST

M. Omaña, D. Rossi, E. Beniamino, C. Metra, C. Tirumurti and R. Galivanche

Abstract—During at-speed test of high performance sequential ICs using scan-based Logic BIST, the IC activity factor (AF) induced by the applied test vectors is significantly higher than that experienced during its in field operation. Consequently, power droop (PD) may take place during both shift and capture phases, which will slow down the circuit under test (CUT) signal transitions. At capture, this phenomenon is likely to be erroneously recognized as due to delay faults. As a result, a false test fail may be generated, with consequent increase in yield loss. In this paper, we propose two approaches to reduce the PD generated at capture during at-speed test of sequential circuits with scan-based Logic BIST using the Launch-On-Shift scheme. Both approaches increase the correlation between adjacent bits of the scan chains with respect to conventional scan-based LBIST. This way, the AF of the scan chains at capture is reduced. Consequently, the AF of the CUT at capture, thus the PD at capture, is also reduced compared to conventional scan-based LBIST. The former approach, hereinafter referred to as Low-Cost Approach (LCA), enables a 50% reduction in the worst case magnitude of PD during conventional logic BIST. It requires a small cost in terms of area overhead (of approximately 1.5% on average), and it does not increase the number of test vectors over the conventional scan-based LBIST to achieve the same Fault Coverage (FC). Moreover, compared to three recent alternative solutions, LCA features a comparable AF in the scan chains at capture, while requiring lower test time and area overhead. The second approach, hereinafter referred to as High-Reduction Approach (HRA), enables scalable PD reductions at capture of up to 87%, with limited additional costs in terms of area overhead and number of required test vectors for a given target FC, over our LCA approach. Particularly, compared to two of the three recent alternative solutions mentioned above, HRA enables a significantly lower AF in the scan chains during the application of test vectors, while requiring either a comparable area overhead or a significantly lower test time. Compared to the remaining alternative solutions mentioned above, HRA enables a similar AF in the scan chains at capture (approximately 90% lower than conventional scan-based LBIST), while requiring a significantly lower test time (approximately 4.87 times on average lower number of test vectors) and comparable area overhead (of approximately 1.9% on average).

Index Terms— Logic BIST, Power Droop, Test, Microprocessor

1 INTRODUCTION

THE continuous scaling of microelectronic technology enables to keep on increasing ICs' integration density and performance. This comes together with new challenges for system test and reliability. In particular, during at-speed test of high performance sequential ICs using scan (for instance microprocessors), the IC activity factor (AF) induced by the applied test vectors is significantly higher than that experienced during its in field operation [1, 2, 3, 4, 5, 6, 7, 9, 10]. Consequently, power droop (PD) may take place during both shift and capture phases, which will slow down the circuit under test (CUT) signal transitions. At capture, this phenomenon is likely to be erroneously recognized as due to delay faults. As a result, a false test fail may be generated, with consequent increase in yield loss [2, 3].

To avoid this problem when at-speed testing is performed by an ATE, some ATPG approaches have been proposed (e.g., those in [11, 12]). They use *don't care bit*s (X) to reduce the AF at capture induced by the applied test vectors. However, due to the increasing costs of ATE and the rapidly evolving microelectronic technology, at-speed testing of logic blocks is nowadays frequently performed using Logic Built-In Self-Test (LBIST) [8, 2, 4, 9]. LBIST can take the form of combinational LBIST, in case of a combinational CUT, or scan-based LBIST, in case of a sequential CUT with scan [6, 13]. In both cases, a linear feedback shift register (LFSR) generates the test vectors that are given to the CUT primary inputs, for combinational LBIST, or to the scan chain inputs, for scan-based LBIST [1, 2, 6, 14, 15]. Both combinational and scan-based LBIST schemes suffer from the PD-induced problem at capture described above.

- *M. Omaña and C. Metra are with the University of Bologna, Bologna 40133, Italy. E-mail: {martin.omana; cecilia.metra}@ unibo.it.*
- *D. Rossi was with the University of Bologna at this research time, and is now with the University of Southampton, Southampton, UK. E-mail: d.rossi@soton.ac.uk*
- *C. Tirumurti and R. Galivanche are with Intel Corporation, Santa Clara (CA), USA. E-mail: {chandra.tirumurti; rajesh.galivanche}@intel.com.*

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In case of scan-based LBIST, two basic capture-clocking schemes exist [6, 14, 16]: the launch-on-shift (LOS) scheme, and the launch-on-capture (LOC) scheme. In the LOS scheme, the test vectors are applied to the CUT at the last shift clock (CK) of the shift phase, and the CUT response is sampled on the scan chains at the following capture cycle. In the LOC scheme, instead, the test vectors are first loaded into the scan-chains during the shift phase, then, at the following capture cycle, the test vectors are applied to the CUT, and the CUT response is captured on the scan chains at a subsequent, second, capture cycle [16].

In this paper we consider the case of sequential CUTs with scan-based LBIST adopting a LOS scheme, which is frequently employed for high performance microprocessors.

Some approaches have been proposed in the literature to reduce the PD for combinational LBIST (e.g., [1, 3]), while fewer approaches exist for scan-based LBIST [2, 6, 8, 17, 18]. The solutions for combinational LBIST in [1, 3] modify the internal structure of traditional LFSRs to generate intermediate test vectors. Such vectors are inserted between each couple of original test vectors, and enable to reduce the AF of the CUT inputs, thus also the whole CUT AF [1]. Therefore, PD is reduced as well. However, these techniques are not effective in reducing PD at capture in scan-based LBIST.

To reduce PD at capture in scan-based LBIST, the solutions in [2, 6, 8, 9, 17, 18] have been proposed. Particularly, in [2] PD is reduced by alternately disabling groups of scan chains during test. This is a successful approach to reduce PD at capture during scan-based LBIST, for both the LOC and the LOS schemes. However, it requires a significant increase in number of test vectors, and consequently test time, to achieve the same Fault Coverage (FC) as with conventional scan-based LBIST.

In [8], PD at capture is reduced by a multi-cycle BIST scheme with partial observation. This solution does not significantly impact the number of test vectors compared to conventional scan-based LBIST, but enables to reduce PD at capture only during scan-based LBIST employing the LOC scheme.

The solution in [6] modifies the internal structure of traditional LBIST LFSRs to generate intermediate test vectors that increase the correlation between adjacent bits loaded in the scan chains of LOS schemes. The AF of the scan chains at capture is reduced with respect to conventional scan-based LBIST, so that the whole CUT AF at capture, thus the PD at capture, is reduced.

In [9], a test pattern generator with a pre-selected toggling level (PRESTO) is presented. It enables to scale the AF reduction in the scan chains by preselecting the number of shift cycles during which they are loaded with constant logic values. This is a successful approach to reduce PD at capture in scan-based LBIST employing the LOS scheme. However, it requires a significant increase in the number of test vectors, thus test time, to achieve the same FC as with conventional scan-based LBIST.

The solution in [17] inserts an additional phase, namely a "burst" phase, between the scan shift and capture phases. The burst phase aims at increasing the current drawn from the power supply up to a value similar to that absorbed by the CUT at capture. This way, the inductive component of PD occurs during the burst phase, and vanishes before the capture phase. Therefore, the PD at capture will consist only of the resistive component, and will be lower than that with Conventional LBIST. This solution does not impact the fault coverage and can be employed during scan-based LBIST, for both LOC and LOS schemes. However, it increases test time, as well as the total power consumed during test, with its associated negative thermal effects.

In [19], we recently proposed an approach to reduce PD at capture in scan-based LBIST adopting the LOC scheme. It enables to reduce PD at capture up to the 50% compared to conventional scan-based LBIST by replacing one test vector of the test sequence with a substitute test vector that increases the correlation between the test vectors applied at following capture cycles. However, this approach does not increase the correlation between adjacent bits of the scan chains, so that it is not effective in reducing PD at capture in scan-based LBIST adopting the LOS scheme.

Based on these considerations, in this paper we propose two approaches to reduce the PD at capture of sequential circuits with scan-based Logic BIST with Launch-On-Shift scheme. The basic idea behind our approaches, which has been introduced in [20], is to increase the correlation between adjacent bits of the scan chains with respect to conventional scan-based LBIST. This way, at capture, the AF of the scan chains is reduced with respect to conventional scan-based LBIST. As a consequence, the AF of the CUT at capture, thus the PD at capture, is also reduced compared to conventional scan-based LBIST.

Our first approach, hereinafter referred to as Low-Cost Approach (LCA), enables a reduction of PD at capture of the 50% with respect to conventional scan-based LBIST. It requires a small cost in terms of area overhead (of approximately the 1.5% on average), and does not increase the number of test vectors over those required by conventional scan-based LBIST to achieve the same FC. Compared to the recent solutions in [6, 2, 9], also able to reduce the PD at capture in scan-based LBIST using the LOS scheme, LCA features a comparable AF in the scan chains during the application of test vectors (thus featuring a comparable reduction of the PD at capture), while requiring significantly lower test time and area overhead.

Our second solution, hereinafter referred to as High-Reduction Approach (HRA), relies on further increasing the correlation between adjacent bits of the scan chains compared to LCA. It enables scalable reductions of the PD at capture up to the 87%, thus allowing maximal flexibility to the test development team concerning the PD to induce during test, in order to avoid false test fails [21]. This is achieved at limited additional cost (in terms of area overhead and required number of test vectors to achieve a target FC) over LCA. Compared to the recent solutions in [6, 2] mentioned above, HCA enables a significantly lower AF in the scan chains at capture (thus allowing a significant reduction of the PD at capture), while re-

quiring either a comparable area overhead, or significantly lower test time. Instead, compared to the recent solution in [9], HRA enables a similar AF in the scan chains at capture, while requiring a significantly lower test time and comparable area overhead.

Of course, either our LCA or HRA can be more conveniently adopted for any given CUT, based on the required amount of PD reduction at capture over Conv-LBIST, which is needed to minimize the likelihood to generate false test fails during the CUT at-speed test.

The remainder of the paper is organized as follows. In Section 2, we describe the considered, conventional scan-based LBIST. In Section 3, we introduce our proposed approaches for PD reduction at capture. In Section 4, we show a possible hardware implementation of our approaches. In Section 5, we evaluate their costs and compare them to those of conventional scan-based LBIST and to those of the alternative solutions in [2, 6, 9]. Finally, we draw some conclusions in Section 6.

2 Considered Scenario

We consider the widely adopted scan-based LBIST (hereinafter referred as Conv-LBIST) architecture represented in Fig. 1(a) [1, 4, 6, 14, 22].

The state flip-flops of the CUT are converted into scan flip-flops and arranged into many short scan chains (s scan chains in Fig. 1(a)). Additional scan flip-flops are included in order to drive and sample primary inputs (PI) and primary outputs (PO). The Pseudo-Random Pattern Generator (PRPG) is implemented by an LFSR [4, 14, 22]. The Phase Shifter (PS), enabling to reduce the correlation among the test vectors applied to adjacent scan-chains [22], consists of an XOR network expanding the number of outputs of the LFSR in order to match the number of scan chains s. At the same clock cycle (CK), the PS provides as outputs the current LFSR sequence together with many future/past sequences [22]. The Space Compactor compacts the outputs of the s scan chains to match the number of inputs of the MISR. The MISR generates a signature after the application of all test vectors, which is then compared to the expected one by the Test Response Analyzer (TRA). Finally, the BIST Controller controls all operations during scan-based LBIST.

Fig. 1(b) represents the timing of the considered Conv-LBIST employing a LOS scheme [16]. Two phases can be identified: 1) a shift phase, consisting of n shift CKs (where n is the number of scan flip-flops in the longest scan chain), during which the scan chains are filled in with test vectors, which are applied to the CUT at the last (*n-th*) shift CK; 2) a capture phase, consisting of a single capture clock, in which the CUT response to the test vectors applied at the last shift CK is sampled. Then, other n scan shift CKs are required to shift-out the CUT response and to shift-in the new test vector. In particular, during the shift phase, the phase shifter provides a new bit to each one of the s scan chains (in parallel) at each shift CK. As represented in Fig. 1(b), when employing a LOS scheme, the scan enable (SE) signal must switch to 0 between the last shift CK and the following capture cycle. We refer to the case where the shift CK presents a lower frequency than the capture CK, to reduce power consumption [16].

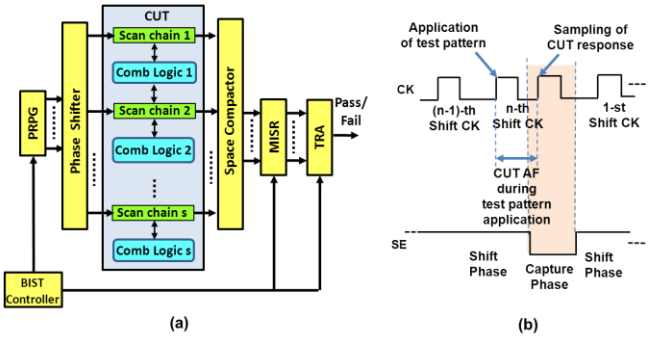

Fig. 1. Schematic representation of the: (a) considered scan-based LBIST architecture; (b) timing for the considered launch on shift clocking strategy.

In the LOS scheme, the delay effect produced by the CUT AF that can be erroneously recognized as a delay fault (with the consequent generation of a false test fail) occurs at capture, that is between the last (*n-th*) shift CK and the following capture cycle. Such a CUT AF is proportional to the AF of the scan chains at the last *n-th* shift CK [6], which is equal to the number of bits in the scan chains that change logic value between the last *n-th* and the last but one *(n-1)-th* shift CKs.

3 Proposed Approaches for AF Reduction

As previously introduced, the goal of our approach is to reduce the CUT AF at capture, since this is the AF that may result in the generation of a false test fail during LBIST. As stated above, such a CUT AF is proportional to the AF of the scan chains at the last (*n-th*) shift CK [6], which is equal to the number of bits in the scan chains that change logic value between the *(n-1)-th* and the *n-th* shift CKs. To reduce the CUT AF at capture, our approaches reduce the AF of all scan chains between the *n-th* shift CK and the previous *(n-1)-th* shift CK, by properly modifying *n-1* bits out of the n bits to be loaded in the scan chains.

3.1 Low-Cost Approach (LCA)

To reduce the AF of all scan chains between the *n-th* shift CK and the previous *(n-1)-th* shift CK, LCA increases the correlation between adjacent bits by conditionally "modifying" *n-1* bits, out of the n bits to be loaded in the scan chains. Fig. 2 shows how our approach modifies the bits b_i (i=2..n) of each scan chain m (m=1..s). In particular, at the last *n-th* shift CK:

- all bits b_i (i=2..n) that would not change logic value between the *n-th* and the *(n-1)-th* shift CKs are not changed (i.e., $b_i(n)$ keeps the same value it had at the previous shift CK $b_i(n-1)$);
- all bits b_i (i=2..n) that would change logic value between the *n-th* and the *(n-1)-th* shift CKs are substituted by a random bit, denoted by R, that can simply

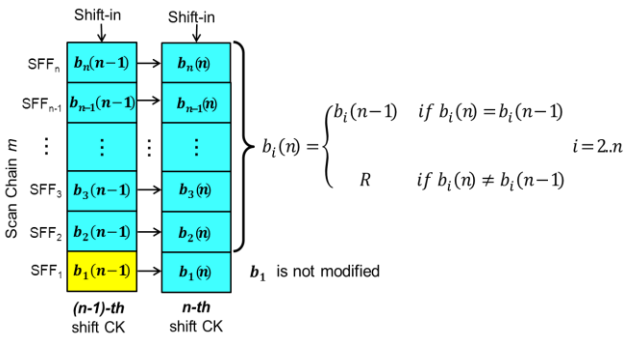

Fig. 2. Schematic representation of the LCA modification of the bits to be loaded in a generic scan chain *m* (*m=1..s*).

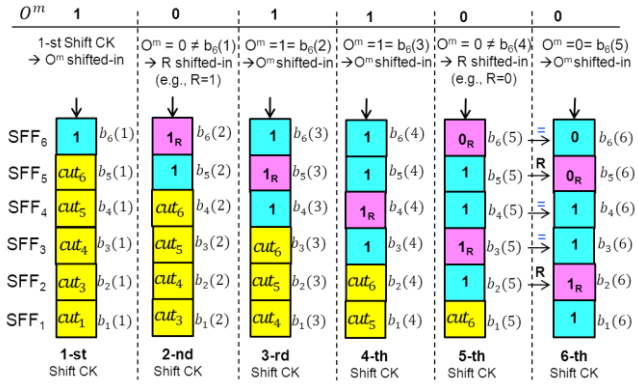

Fig. 3. Schematic representation of a scan chain *m* being filled-in according to our LCA, for the case of a scan chain length of 6 (n=6).

come from one of the outputs of the LFSR itself, as suggested in [6].

As for the first bit to be loaded into each scan chain *m* (b_1), in order to evaluate whether it changes logic value between the *(n-1)-th* and the *n-th* shift CKs and apply the bit modification strategy described above, we would need to compare it to the CUT output bit loaded into SFF_n at the previous capture cycle, whose identification would require to perform CUT logic simulation. To simplify the application of our approach, we have consequently chosen not to modify the logic value of bit b_1. We have verified that, due to the usual long length of scan chains of real ICs, this choice has a minimal impact on the effectiveness of our approach in reducing the AF of the scan chains.

As an example, Fig. 3 shows how each scan chain *m* is filled-in according to our approach, for the simple case of scan chains of length equal to 6 SFFs (*n=6*). At the 1st shift CK, our scheme shifts-into SFF_6 the logic value at the PS output O^m (a logic 1 Fig. 3). We denote by $b_i(j)$ the output value of the SFF_i at the *j-th* shift CK. At the 2nd shift CK, it is O^m=0, which is different from $b_6(1)$. Consequently, our scheme shifts-in an *R* value (in the example we assume *R*=1) into SFF_6, making $b_6(2) = R = 1$. At the 3rd shift CK it is O^m=1, which is the same as $b_6(2)$. Thus our scheme shifts-into SFF_6 the PS output O^m, making $b_6(3) = 1$. At the 4th shift CK, it is again O^m=1, which is the same as $b_6(3)$, thus our scheme shifts-into SFF_6 the logic value at O^m again, thus making $b_6(4) = 1$. At the 5th shift CK, it is O^m=0, which is different from $b_6(4)$, thus our scheme shifts-in an *R* value (*e.g., R=0*) into SFF_6, thus making $b_6(5) = R = 0$. Finally, at the 6th shift CK, it is again O^m=0, which is the same as $b_6(5)$, thus our scheme shifts-into SFF_6 the logic value at the PS output O^m, thus making $b_6(6) = 0$.

From Fig. 3 we can observe that, as described before for Fig. 2, at the last shift CK (6-*th* shift CK), the bits $b_{3,4,6}(6)$ that would not change logic value between the *5-th* and the 6-*th* shift CKs are not changed (i.e., they keep the value they had at the previous *5-th* shift CK), while the bits $b_{2,5}(6)$ that would change logic value between the *5-th* and the *6-th* shift CKs are substituted by an *R* bit (i.e., they assume a random value at the *6-th* shift CK).

Let us now briefly evaluate the AF between the *(n-1)-th* and the *n-th* shift CKs enabled by our LCA (AF_{LCA}). To simplify this evaluation, let us assume that all scan chains have the same number *n* of scan flip-flops, and that the AF between the *(n-1)-th* and the *n-th* shift CKs in each scan chain is the same for all scan chains. However, in Section 5, we will show that the derived expression for AF_{LCA} is accurate also when these simplifying assumptions are not satisfied.

AF_{LCA} can be derived by simply considering that, with the insertion of an *R* value in the bits of the scan chains that would change logic values between the *(n-1)-th* and the *n-th* shift CKs, our approach allows to halve the number of transitions in the scan chains with respect to Conv-LBIST. Therefore, under the above simplifying assumptions, it is:

$$AF_{LCA} \cong \frac{AF_{con}}{n} \cdot \left[\frac{(n-1)}{2} + 1\right] = AF_{con}\left(\frac{n+1}{2n}\right) \quad (1)$$

where AF_{con} is the AF in the scan chains between the *(n-1)-th* and the *n-th* shift CKs obtained with conventional LBIST. Thus, if $n \gg 1$ (as it is generally the case for real applications), LCA allows a reduction of approximately 50% in the AF of the scan chains at capture, thus in the CUT AF at capture, with respect to conventional LBIST.

On the other hand, our scheme loads random *R* values in the positions of the scan chains where $b_i(n)$ and $b_i(n-1)$ are different (as shown in Fig. 2). Such scan chain bits preserve the randomness of the original test vectors loaded in Conv-LBIST [6], so that, as will be shown in Section 5, the number of test vectors required to achieve a target FC is not increased compared to the original test sequence. As a result, LCA enables a CUT AF reduction at capture of approximately 50% with respect to conventional LBIST, thus enabling a significant PD reduction at capture, with no test time increase to achieve a given target FC.

3.2 High-Reduction Approach (HRA)

In order to enable scalable AF reductions at capture higher than 50%, we propose an approach that combines two methodologies to increase the correlation between adja-

cent bits to be loaded in the scan chains. They are:

1. Methodology 1 (*Met1*): we repeat the same logic value for the last two shift CKs for a given number of *t* bits out of the *n* bits to be loaded in the scan chains (i.e., these *t* bits keep the same logic values for the last two shift CKs).
2. Methodology 2 (*Met2*): we modify the logic values of the remaining *n-t-1* bits to be loaded in the scan chains as in LCA (i.e., we load random values *R* in the bits that would change logic value between the *n-th* and the *(n-1)-th* shift CKs).

By applying *Met1* and *Met2*, we can scale the achievable AF reduction at capture beyond the 50% over Conv-LBIST by simply increasing the number of *t* bits modified by *Met1*.

In principle, we could apply *Met1* to any *t* bits of the scan chains (with $t \in [0, n-1]$). However, we have verified that in order to minimize the impact on the required number of test vectors to achieve a given FC, the application of *Met1* and *Met2* should alternate, as will be shown in the following Subsections.

A. HRA with 1-out-of-2 Bits in SCs Repeating Logic Value

We modify the original bits to be loaded in the SCs by alternating 1 bit repeating the same logic value for the last two shift CKs (as per *Met1*) with 1 bit modified as per *Met2*. This way, *1-out-of-2* bits loaded in the scan chains repeats the same logic value for the last two shift CKs, as schematically shown in Fig. 4.

As for LCA, in order to simplify the application of our approach, we choose not to modify the logic value of the first bit to be loaded into each scan chain *m* (bit b_1). Thus, in this case, out of the *n* bits to be loaded in the scan chains, $t = \lceil (n-1)/2 \rceil$ bits will be modified by *Met1*, while the remaining *n-t-1* bits will be modified by *Met2* (as in LCA).

Let us now briefly evaluate the AF between the last two shift CKs allowed by the above described HRA (AF_{HRA}). To simplify this evaluation, let us assume that: 1) all scan chains have the same number *n* of scan flip-flops; 2) the AF between the *(n-1)-th* and the *n-th* shift CKs in each scan chain is the same for all scan chains; 3) the number of bits modified by *Met1* is $t = \lceil (n-1)/2 \rceil = (n-1)/2$ (i.e., *n-1* is even). However, in Section 5, we will show that the derived expression for AF_{HRA} is accurate also when the above simplifying assumptions are not satisfied.

AF_{HRA} can be derived by considering that the *t* bits of the scan chains modified as per *Met1* will present no transition between the last two shift CKs, while the *n-t-1* bits modified as per *Met2* will present a number of transitions between the last two shift CKs equal to half the number of transitions in the scan chains loaded with Conv-LBIST. Therefore, under the above simplifying assumptions, it is:

$$AF_{HRA} \cong \frac{AF_{con}}{n} \cdot \left[\frac{(n-t-1)}{2} + 1\right] = AF_{con}\left(\frac{n+2}{4n}\right) \quad (2)$$

where, as before, AF_{con} is the AF in the scan chains between the last two shift CKs obtained with conventional LBIST. Thus, if $n \gg 2$, the repetition of *1-out-of-2* bits of the scan chains will enable a reduction of approximately 75% in the AF of the scan chains at capture, thus in the CUT AF at capture, with respect to conventional LBIST.

Additionally, in Section 5 we will show that HRA with *1-out-of-2* bits repeating logic value for the last two shift CKs presents a very low increase in the number of test vectors over Conv-LBIST to achieve the same FC. This because the randomness of the original test vector is preserved by loading a random value when $b_i(n)$ and $b_i(n-1)$ differ [6], as per *Met2*.

B. HRA with 2-out-of-3 Bits in SCs Repeating Logic Value

We modify the original bits to be loaded in the SCs by alternating 2 adjacent bits repeating the same logic value for the last two shift CKs (*Met1*) with 1 bit modified as per *Met2*. This way, *2-out-of-3* bits loaded in the scan chains repeat the same logic value for the last two shift CKs, as schematically shown in Fig. 5.

As before, in order to simplify the application of our approach, we choose not to modify the logic value of the first bit to be loaded into each scan chain *m* (bit b_1). Thus, in this case, out of the *n* bits, $t = \lceil 2(n-1)/3 \rceil$ bits will be modified by *Met1*, and the remaining *n-t-1=n/3-1* bits will be modified by *Met2* (as in LCA).

Let us now briefly evaluate the AF between the last two shift CKs allowed by HRA (AF_{HRA}) with the *2-out-of-3*

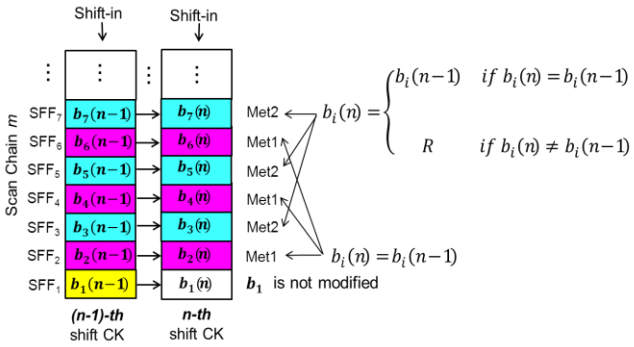

Fig. 4. Schematic representation of the methodology employed by HRA to modify the bits to be loaded in a scan chain *m* (*m=1..s*), in case of *1-out-of-2* bits of the scan chains repeating the same logic value for the last two shift CKs.

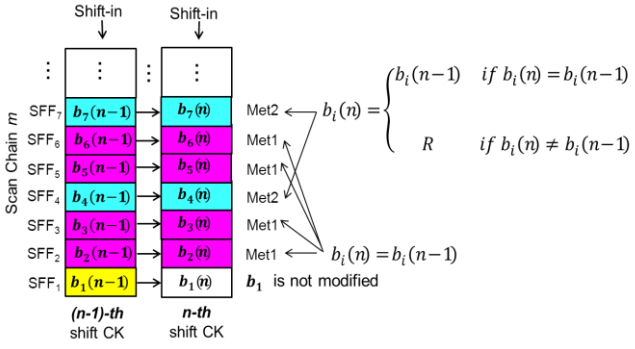

Fig. 5. Schematic representation of the methodology employed by HRA to modify the bits to be loaded in a scan chain *m* (*m=1..s*), in case of *2-out-of-3* bits of the scan chains repeating the same logic value for the last two shift CKs.

solution, as described above. As before, the following simplifying assumptions are considered: 1) all scan chains have the same number n of scan flip-flops; 2) the AF between the *(n-1)-th* and the *n-th* shift CKs in each scan chain is the same for all scan chains; 3) the number of bits modified by *Met1* is $t = \lceil 2(n-1)/3 \rceil = 2(n-1)/3$ (i.e., *2(n-1)* is divisible by 3). However, in Section 5, we will show that the derived expression for AF_{HRA} is accurate also when the above simplifying assumptions are not satisfied.

As before, AF_{HRA} can be derived by considering that the t bits of the scan chains modified by *Met1* will present no transition between the last two shift CKs, while the *n-t-1* bits of the scan chains modified by *Met2* will present a number of transitions between the last two shift CKs equal to half the number of transitions in the scan chains loaded with Conv-LBIST. It is:

$$AF_{HRA} \cong \frac{AF_{con}}{n} \cdot \left[\frac{(n-t-1)}{2} + 1\right] = AF_{con}\left(\frac{n+3}{6n}\right) \quad (3)$$

where AF_{con} has the same meaning as in (2). Thus, if $n \gg 3$, the repetition of *2-out-of-3* bits of the scan chains will enable a reduction of approximately the 83% in the AF of the scan chains at capture, thus in the CUT AF at capture, with respect to conventional LBIST.

Analogously to the *1-out-of-2* solution described in the previous subsection, HRA with *2-out-3* bits repeating logic value for the last two shift CKs presents a very low increase in the number of test vectors over Conv-LBIST to achieve the same FC.

C. Generalized HRA with m-out-of-(m+1) Bits in SCs Repeating Logic Value

We can generalize the alternation of *Met1* and *Met2* so that we load in the scan chains m adjacent bits repeating the same logic value for the last two shift CKs (*Met1*) with 1 bit modified by *Met2*. This way, *m-out-of-(m+1)* bits loaded in the scan chains repeat the same logic value for the last two shift CKs.

In this general case, out of the n bits to be loaded in the scan chains, $t = \lceil m(n-1)/(m+1) \rceil$ bits will be modified by *Met1,* while the remaining *n-t-1* bits will be modified by *Met2*.

Let us now briefly evaluate the AF between the last two shift CKs allowed by HRA (AF_{HRA}) in the general case of *m-out-of-(m+1)* bits in the SCs repeating logic value. As before, to simplify this evaluation, we assume that: 1) all scan chains have the same number n of scan flip-flops; 2) the AF between the *(n-1)-th* and the *n-th* shift CKs in each scan chain is the same for all scan chains; 3) the number of bits modified by *Met1* is $t = \lceil m(n-1)/(m+1) \rceil = m(n-1)/(m+1)$ (*i.e., m(n-1)* is divisible by *(m+1)*). However, in Section 5, we will show that the derived expression for AF_{HRA} is accurate also when the above simplifying assumptions are not satisfied.

As before, AF_{HRA} can be derived by simply considering that the t bits of the scan chains modified by *Met1* will present no transition between the last two shift CKs, while the *n-t-1* bits of the scan chains modified by *Met2* will present a number of transitions between the last two shift CKs equal to half the number of transitions in the scan chains loaded with Conv-LBIST. Therefore, under the above simplifying assumptions, the AF between the last two shift CKs enabled by our HRA (AF_{our}) in case of *m-out-of-(m+1)* repeated bits can be expressed as follows:

$$AF_{HRA} \cong \frac{AF_{con}}{n} \cdot \left[\frac{n-t-1)}{2} + 1\right] = AF_{con}\left(\frac{n+(m+1)}{2n(m+1)}\right) \quad (4)$$

where, as before, AF_{con} is the AF in the scan chains between the last two shift CKs obtained with conventional LBIST. From (4), we can easily predict that the repetition of *3-out-of-4* bits (m=3) of the scan chains will enable a reduction of approximately the 87% in the AF of the scan chains at capture, while the repetition of *4-out-of-5* bits (m=4) of the scan chains will enable a reduction of approximately the 90% in the AF of the scan chains at capture.

Therefore, for *4-out-of-5* bits in the scan chains repeating logic values, we already obtain an AF reduction at capture of approximately the 90% over Conv-LBIST. On the other hand, we have verified that for more than *4-out-of-5* bits in the scan chains repeating logic values (*e.g.,* for *5-out-of-6* bits in the scan chains repeating logic values), the increase in the number of test vectors over Conv-LBIST to achieve the same FC becomes significant.

Therefore, since HRA repeating *4-out-of-5* bits of the scan chains enables to achieve AF reductions at capture of approximately the 90%, while still not requiring a significant increase in the number of test vectors, in the rest of this paper we will consider HRA with up to a maximum of *4-out-of-5* bits repeating logic values in the scan chain.

4 Possible Implementation

In this section we present a possible hardware implementation for both our LCA and HRA approaches (described in Section 3.1 and Section 3.2, respectively).

4.1. LCA Implementation

The proposed hardware implementation is represented in Fig. 6, for the case in which the depth of the longest chain(s) is n. As shown in Fig. 6(a), for each scan chain m, our approach requires 1 multiplexer (M1), a 2-input AND, and a 2-input XOR. At each shift CK, M1 allows to load in the scan chain m: 1) the bits given on the PS output O^m (as in Conv-LBIST), when *sel*=0; 2) bits with a random value R, when *sel*=1.

When the control signal *int* is 0, the AND gate allows to make *sel*=0, thus loading into the scan chain m the bits given on the PS output O^m. Instead, when *int*=1, depending on the value of the *mod* signal generated by the XOR gate, M1 selects whether to drive the logic value on O^m or the random value R in the scan chain m. The signal *int* must be equal to 0 in the first shift CK in order to load into the scan chain the first unmodified bit, as required by our approach. Then, in the remaining *n-1* shift CKs, the signal *int* is equal to 1 in order to enable to modify the bits to be loaded into the scan chain m, when required by our approach.

As for the XOR gate, at each shift CK, it compares the logic value at the PS output O^m (to be loaded into the scan flip-flop SFF_n at the following shift CK) with the logic value b_n loaded at the output of SFF_n. Thus, the XOR makes *mod=0*, if $O^m = b_n$ (or, equivalently, if the value to be loaded by PS into the scan chain at the next shift CK is equal to the value at the SFF_n output), thus indicating that the logic value of bit b_n (output of SFF_n) at the next shift CK should be equal to the PS output O^m. Instead, the XOR makes *mod=1*, if $O^m \neq b_n$ (or, equivalently, if the value to be loaded by PS into the scan chain at the next shift CK is different from the value at the SFF_n output), thus indicating that the logic value of bit b_n (output of SFF_n) at the next shift CK should be a random value *R*. As also shown in Fig. 6(a), the bit *R* can be generated from any output of the LFSR [6], thus being not truly random. However, the effectiveness of our approach does not depend on the chosen *R* bit. At the design phase, it will be a designer's choice which output of the LFSR to consider as *R* bit. Once this is decided, our approach will enable to achieve the required CUT AF reduction at capture, by properly modifying the test vectors as described before.

Fig. 6(b) shows a possible scheme to generate the signal *int*. The scan enable (*SE*) signal feeds a standard flip-flop D (FFD), which is clocked by the complement of the shift CK signal. Therefore, at each falling edge of CK, FFD samples the value of *SE*. This way, at the falling edge of the CK pulse within the capture cycle (*t1* in Fig. 6(b)), *int* assumes a logic 0, and FFD keeps *int=0* till the falling edge of the first CK pulse in the next shift phase (*t3* in Fig. 6(b)). This way, at the rising edge of the first CK pulse within the shift phase (*t2* in Fig. 6(b)), it is *int=0*. Thus, it is *sel=0* and the first bit shifted-in the scan chain comes from the PS output O^m, as required by our scheme. Then, at time *t3*, FFD samples *SE=1* on *int*, so that, at the second shift CK, it is *int*=1, as required by our scheme. Since *SE=1* till the next capture cycle, at the following shift CKs *int* continues to be equal to 1. Therefore, as required by our scheme, it is *int=1* till the following capture cycle.

The expected increase in area overhead (AO) of the LCA in Fig. 6 over Conv-LBIST can be expressed as follows:

$$AO(\%) \cong 100\frac{s\cdot(A_{2in-MUX}+A_{2in-AND}+A_{2in-XOR})+A_{DFF}}{A_{Conv-LBIST}},$$

where, *s* is the number of scan chains, $A_{2in\text{-}MUX}$, $A_{2in\text{-}AND}$, $A_{2in\text{-}XOR}$ and A_{DFF} represent the area of a 2-input multiplexer, a 2-input AND gate, a 2-input XOR gate, and a FF D, respectively, while $A_{Conv\text{-}LBIST}$ includes the area of the CUT and the area required to implement Conv-LBIST (i.e., LFSR, PS, MISR, TRA and BIST controller in Fig. 1).

4.2. HRA Implementation

Let us start describing the hardware implementation of the HRA repeating *1-out-of-2* bits of the scan chains. It is shown in Fig. 7 for the case in which the depth of the longest chain(s) is *n*.

As shown in Fig. 7(a), for each scan chain *m*, our approach requires 2 multiplexers (M1 and M2), a 2-input AND, and a 2-input XOR. As for the LCA implementation, M1 allows to select: 1) the bits given on the PS output O^m, when *sel*=0; 2) bits with a random value *R*, when *sel*=1. The AND gate enables to make *sel*=0, thus loading into the scan chain the bits given on the PS output O^m, when *int =0*. Instead, when *int=1,* depending on the value of the *mod* signal (that is generated at the XOR gate output), M1 selects the logic value on O^m or the *R* bit. Therefore, bits at the M1 output are modified as required to implement the methodology *Met2* described before.

Moreover, at each shift CK, M2 allows to load in the scan chain *m*: 1) the bits given at the M1 output, when control signal *rep*=0; 2) the bit b_n at the output of the first scan flip-flop (SFF_n) of the scan chain, when *sel*=1. This way, when *sel=0*, M2 selects to load in the scan chain bits modified by *Met2*. Instead, when *sel*=1, M2 selects to load in the scan chain the same bit loaded at the previous shift CK, that is bits modified by *Met1*. As described before for the LCA, the bit *R* can be simply generated from any output of the LFSR, as shown in Fig. 7(a).

Similarly to the LCA implementation, the signal *int* should be equal to 0 in the first shift CK, and then equal to 1 for the remaining *n-1* shift CKs. Thus, we implement *int* as shown before in Fig. 6(a).

Moreover, in order to enable to alternately select to load in the scan chain (through M2) 1 bit repeated by *Met1* and 1 bit modified by *Met2* at following shift CKs, the signal *rep* should be generated in such a way that it switches from 0 to 1 (and vice versa), at following shift CKs. As an example, *rep* could be generated by the circuit in Fig. 7(b), where *FFD1* and *FFD2* denote D flip-flops. We use the complement of the SE signal to set *FFD1* to 1 and to reset *FFD2* to 0 at each capture phase. Thus, at the beginning of each shift phase, it is *rep*=0. Both *FFD1* and *FFD2* are clocked by the complement of the shift CK signal. Thus, at each falling edge of CK, *rep* switches alternately from 0 to 1, or vice versa. For the particular case of HRA repeating *1-out-of-2* bits of the scan chains, the

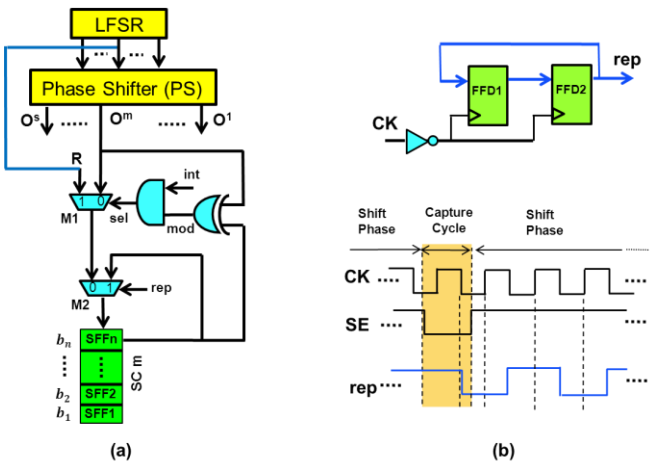

Fig. 7. Schematic representation of the proposed hardware implementation of HRA in case of repeating *1-out-of-2* bits of the scan chains: (a) extra gates required for each scan chain *m*; (b) circuit required to generate the control signal *rep*.

implementation of the *rep* signal in Fig. 7(b) can be simplified by replacing *FFD1* by a *NOT* gate.

Now let us describe the hardware implementation of the HRA repeating *2-out-of-3* bits of the scan chains. For each scan chain *m*, it requires the same circuitry shown before in Fig. 7(a), for our approach repeating *1-out-of-2* bits in the scan chains. Also in this case, the signal *int* should be equal to 0 in the first shift CK, and then equal to 1 for the remaining *n-1* shift CKs. Thus, we implement *int* as shown before in Fig. 6(a).

Instead, in order to enable to select alternately to load in the scan chain (through M2) 2 successive bits repeated by *Met1* and then 1 bit modified by *Met2*, the signal *rep* should be generated in such a way that it is *rep* =*1* for two following shift CKs, and then *rep* =0 for one shift CK. As an example, *rep* could be generated by the circuit in Fig. 8(a). As before, *FFD1*, *FFD2* and *FFD3* denote D flip-flops. We use the complement of the SE signal to set *FFD1* and *FFD2* to 1 and to reset FFD3 to 0 at each capture phase. Thus, at the beginning of each shift phase, it is *rep*=0. Initially, *FFD1* and *FFD2* are set to 1, while *FFD3* is set to 0 (*i.e.*, initially *rep*=0). *FFD1*, *FFD2* and *FFD3* are clocked by the complement of the shift CK signal. Thus, *rep* switches as shown in Fig. 8(a), as required to implement our approach repeating *2-out-of-3* bits of the scan chains.

Finally, the hardware implementation of our generalized HRA repeating *m-out-of-(m+1)* bits of the scan chains requires, also for each scan chain *m*, the same circuitry shown in Fig. 7(a) for our approach repeating *1-out-of-2* bits. Also in this case, *int* should be equal to 0 in the first shift CK, and then equal to 1, for the remaining *n-1* shift CKs. Thus, we implement *int* as shown before in Fig. 6(a).

In order to enable to select alternately to load in the scan chain (through M2) *m* successive bits repeated by *Met1* and then 1 bit modified by *Met2*, the signal *rep* should be generated in such a way that it is *rep* =0 for one shift CK, and then *rep* =1 for *m* following shift CKs. Thus, in a generalized case, *rep* could be generated by expanding the circuits shown in Fig. 8(a) to the case of *(m+1)* FFDs, as shown in Fig. 8(b). We use the complement of the SE signal to set *FFD1* … *FFDm* to 1 and to reset *FFD(m+1)* to 0 at each capture phase. Thus, at the beginning of each shift phase, it is *rep*=0. As before, all FFDs are clocked by the complement of the shift CK signal. Thus, *rep* switches as shown in Fig. 8(b), as required to implement our approach repeating *m-out-of-(m+1)* bits of the scan chains.

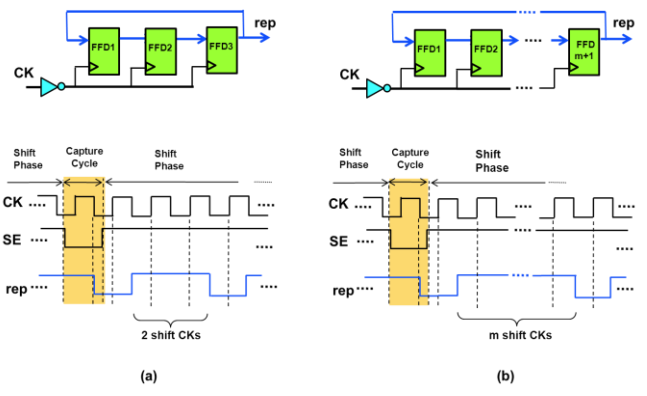

Fig. 8. Schematic representation of the: (a) circuit required to generate the control signal *rep*, in case of repeating *2-out-of-3* bits of the scan chains; (b) circuit required to generate the control signal *rep*, in the general case of repeating *m-out-of-(m+1)* bits of the scan chains.

The expected increase in area overhead (AO) of HRA over Conv-LBIST, in the general case of repeating *m-out-of-(m+1)* bits of the scan chains, can be expressed as follows:

$$AO(\%) \cong 100\frac{s\cdot(2A_{2in-MUX}+A_{2in-AND}+A_{2in-XOR})+(m+1)A_{DFF}}{A_{Conv-LBIST}},$$

where, as before, *s* is the number of scan chains, $A_{2in-MUX}$, $A_{2in-AND}$, $A_{2in-XOR}$, A_{DFF} and $A_{Conv-LBIST}$ represent the area of a 2-input multiplexer, a 2-input AND gate, a 2-input XOR gate, a FF D, and the area required to implement Conv-LBIST (including the area of the CUT), respectively.

5 Comparison

We have compared the effectiveness of our LCA and HRA with those of Conv-LBIST [13], and those of the three recent alternate solutions in [2, 6, 9] for the reduction of PD at capture in scan-based LBIST using the LOS scheme. Effectiveness has been evaluated in terms of allowed PD reduction at capture and number of test vectors required to achieve a target stuck-at FC, which can still be considered a good metric for test quality.

For our HRA, we have considered the cases of repeating *1-out-of-2*, *2-out-of-3*, *3-out-of-4* and *4-out-of-5* bits in the scan chains. The solution in [2] has been implemented considering two scan-chain groups (i.e., the case of N=2 described in [2]), thus providing a value of AF reduction at capture similar to that obtained with our LCA (*i.e.*, a reduction of approximately the 50%). As for the solution in [9], we have evaluated its costs when it features: 1) an AF reduction at capture with respect to Conv-LBIST of 50% (*i.e.*, a value of WTM = 25% in [9]), which is similar to that obtained with our LCA; 2) an AF reduction at capture with respect to Conv-LBIST of 90% (i.e., a value of WTM = 5% in [9]), which is similar to that obtained with our HRA repeating *4-out-of-5* bits in the scan chains.

As examples of CUTs, we have considered the largest four ISCAS'89 benchmarks considered also in [2, 6]. For comparison purposes, since the approach in [6] is designed to work without a PS, we have implemented all compared schemes without PS, by using an LFSR with a number of outputs equal to the number of scan chains (each with characteristic polynomials in [22] for maximal length LFSRs). The number of scan chains (SCs) of each benchmark is reported in the second row of Table I. For all benchmarks, we have considered all SCs with a length of *n=25* scan flip-flops.

For all compared solutions, we have evaluated the maximum AF of the scan chains at the last *n-th* shift CK (AF_{MAX}) which, as clarified before, is proportional to the maximum CUT AF, thus PD, at capture [6].

The number of test vectors (#TVs) required to achieve a target FC has been evaluated by means of the Synopsys

TetraMAX tool and assuming the maximum FC achievable with Conv-LBIST as target FC for each CUT. Such FC growth curves are shown in Fig. 9 for each considered benchmark circuit, as a function of the number of TVs.

We have also evaluated the area overhead (AO) required by our approaches and the solutions in [6, 9] with respect to Conv-LBIST by means of the Synopsys Design Compiler tool. We have not evaluated the AO of the solution in [2] due to the lack of implementation details in [2].

Finally, we have estimated the accuracy of Eqs. (1)-(4) in evaluating the AF_{MAX} of the scan chains at capture of our LCA and HRA, with respect to the AF_{MAX} at capture achieved by simulations performed by the Synopsys Design Compiler tool.

Table I reports the effectiveness and costs obtained for the compared solutions. The table also reports the relative variations of AF_{MAX} at capture and #TVs of the compared solutions over those of Conv-LBIST, calculated as: $\Delta\mathbf{AF_{MAX}}_{\text{ours, [2, 6, 9]}} = 100*(\mathbf{AF_{MAX}}_{\text{ ours, [2, 6, 9]}} - \mathbf{AF_{MAX}}_{\text{Conv-LBIST]}}) / \mathbf{AF_{MAX}}_{\text{ Conv-LBIST}}$) and $\Delta\mathbf{\#TV}_{\text{ours, [2, 6, 9]}} = 100*(\mathbf{\#TV}_{\text{ours, [2, 6, 9]}} - \mathbf{\#TV}_{\text{Conv-LBIST]}}) / \mathbf{\#TV}_{\text{ Conv-LBIST}}$).

From Table I we can observe that, as anticipated before, LCA enables to reduce AF_{MAX} at capture by approximately the 47% on average with respect to Conv-LBIST, with no increase in the number of test vectors over Conv-LBIST to achieve the same FC, and at a small increase in area overhead (of approximately the 1.5% on average).

Instead, compared to the solution in [6], LCA requires a considerably lower area overhead (of approximately the 30% on average), while enabling to achieve approximately the same AF_{MAX} at capture and requiring same number of test vectors.

Moreover, compared to the solution in [2], LCA requires a considerably lower number of test vectors (approximately the 40% on average), thus test time, while allowing to achieve approximately the same AF_{MAX} at capture.

On the other hand, when compared to the solution in [9] enabling approximately the same AF_{MAX} at capture (i.e., a value of WTM = 25% in [9]), LCA requires a lower number of test vectors (approximately the 12% on average), thus test time, and a slightly lower area overhead (the 1.6% on average).

Therefore, compared to the three recent alternate solutions in [2, 6] and [9] (enabling an AF_{MAX} reduction at capture of 50%), LCA features a comparable AF_{MAX} reduction at capture (ΔAF_{MAX}) over Conv-LBIST (thus also a comparable PD reduction at capture), while requiring lower test time, or area overhead.

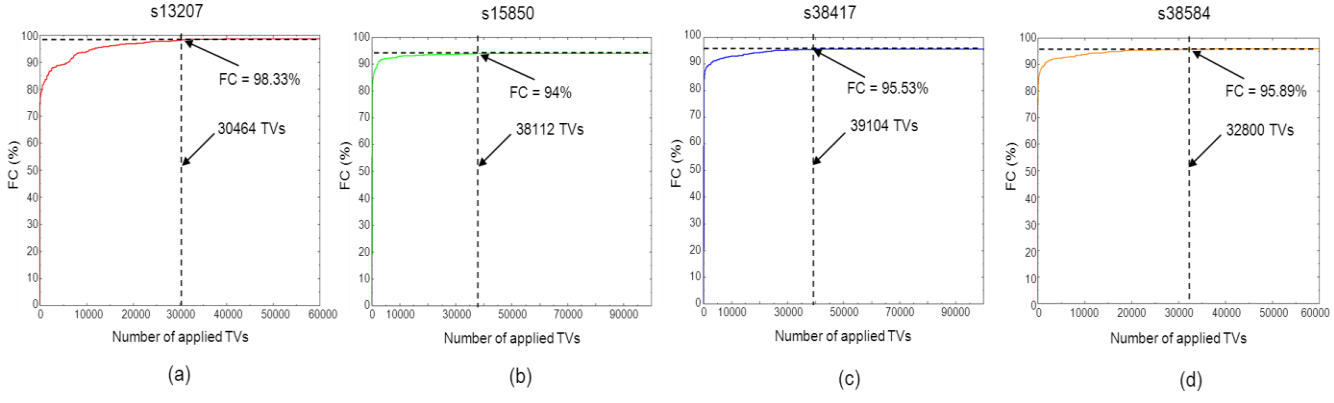

Fig 9. Fault coverage growth curves achievable with Conv-LBIST as a function of the number of TVs applied to the considered benchmarks: (a) s13207; (b) s15850; (c) s38417 and (d) s38584 circuit.

Instead, from Table I, we can observe that HRA allows to increase the reduction of the AF_{MAX} at capture over Conv-LBIST (ΔAF_{MAX}) as the number of repeated bits in the SCs increases. In particular, when only *1-out-of-2* bits of the SCs are repeated, we obtain a minimum ΔAF_{MAX} over Conv-LBIST of the 72.1% on average, at the cost of an AO of the 1.9% on average (which corresponds to an AO increase of the 24% over our LCA) and an increase in the number of TVs over Conv-LBIST of only the 1.2% on average. On the other hand, when *4-out-of-5* bits of the SCs are repeated, we obtain a ΔAF_{MAX} over Conv-LBIST of the 87.2% on average, at the cost of an AO of the 1.9% on average (which corresponds to an AO increase of the 24% over our LCA) and an increase in the number of TVs over Conv-LBIST of the 9% on average. Such a low increase in the number of TVs is in accordance with the results in [9, 6], indicating that test vectors with groups of many adjacent bits taking the same logic value do not degrade fault coverage with respect to pseudo-random test vectors, since they increase the likelihood to detect faults that are hard to detect with pseudo-random test vectors.

TABLE I. AF_{MAX} AT CAPTURE, #TV AND AO OF THE COMPARED SOLUTIONS.

		s13207	s15850	s38417	s38584
# of scan chains		28	25	67	59
Target FC		98.33%	94.00%	95.53%	95.89%
Conv-LBIST	AF_{MAX}(%)	55.4	58.8	53.8	54.6
	#TVs	**30464**	**38112**	**39104**	**32800**
Solution in [6]	AF_{MAX}(%)	33.1	34.0	32.0	31.8
	ΔAF_{MAX}	**-40.2**	**-42.2**	**-40.5**	**-41.7**
	#TV	30764	37882	39529	32697
	Δ#TV (%)	**0.98**	**-0.6**	**1.1**	**-0.31**
	AO (%)	**~2.5**	**~2.2**	**~2.1**	**~1.8**
Solution in [2] (N=2)	AF_{MAX}(%)	30.7	31.9	28.5	28.8
	ΔAF_{MAX}	**-44.6**	**-45.7**	**-47.0**	**-47.2**
	#TV	55361	42367	80635	52334
	Δ#TV (%)	**81.7**	**11.2**	**106.2**	**59.5**
	AO (%)	NA	NA	NA	NA
Solution in [9] (WTM=25%)	AF_{MAX}(%)	30.5	31.9	31.2	31.1
	ΔAF_{MAX}	**-44.9**	**-45.7**	**-42.0**	**-43.0**
	#TV	34150	41630	43522	37851
	Δ#TV (%)	**12.1**	**9.2**	**11.3**	**15.4**
	AO (%)	**3.6**	**3.1**	**3.1**	**2.7**
Solution in [9] (WTM=5%)	AF_{MAX}(%)	5.8	6.0	5.6	5.6
	ΔAF_{MAX}	**-89.6**	**-89.8**	**-89.7**	**-89.7**
	#TV	192685	153401	224848	169740
	Δ#TV (%)	**533**	**303**	**475**	**418**
	AO (%)	**3.6**	**3.1**	**3.1**	**2.7**
Our LCA	AF_{MAX}(%)	30.0	30.8	28.5	28.5
	ΔAF_{MAX} (%)	**-45.9**	**-47.6**	**-46.9**	**-47.8**
	#TV	30384	37526	38698	32817
	Δ#TV (%)	**-0.26**	**-1.54**	**-1.04**	**0.05**
	AO (%)	**~1.7**	**~1.5**	**~1.6**	**~1.4**
Our HRA (1-out-of-2)	AF_{MAX}(%)	16.0	16.2	14.8	15.0
	ΔAF_{MAX} (%)	**-71.1**	**-72.4**	**-72.5**	**-72.6**
	#TV	30498	38671	40047	33010
	Δ#TV (%)	**0.11**	**1.47**	**2.48**	**0.64**
	AO (%)	**~1.7**	**~2.1**	**~1.9**	**~1.8**
Our HRA (2-out-of-3)	AF_{MAX}(%)	11.6	11.8	12.0	11.7
	ΔAF_{MAX} (%)	**-79.1**	**-79.9**	**-77.7**	**-78.5**
	#TV	31491	39251	41248	33055
	Δ#TV (%)	**3.37**	**2.99**	**5.48**	**0.78**
	AO (%)	**~1.7**	**~2.1**	**~1.9**	**~1.8**
Our HRA (3-out-of-4)	AF_{MAX}(%)	9.0	9.0	9.3	9.4
	ΔAF_{MAX} (%)	**-83.8**	**-84.7**	**-82.8**	**-82.7**
	#TV	33952	39668	43252	33066
	Δ#TV (%)	**11.45**	**4.08**	**10.61**	**0.81**
	AO (%)	**~1.7**	**~2.1**	**~1.9**	**~1.8**
Our HRA (4-out-of-5)	AF_{MAX}(%)	7.3	7.4	6.7	7.2
	ΔAF_{MAX} (%)	**-86.9**	**87.5**	**87.5**	**-86.9**
	#TV	35225	40364	44363	33107
	Δ#TV (%)	**15.64**	**5.91**	**13.45**	**0.94**
	AO (%)	**~1.7**	**~2.1**	**~1.9**	**~1.8**

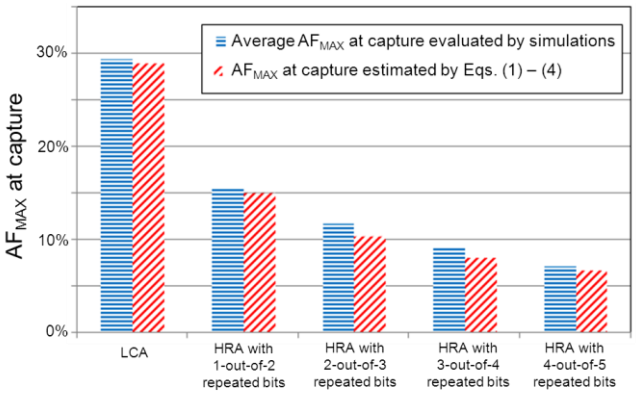

Fig. 10. Comparison, for the four considered benchmarks, of the average AF_{MAX} at capture achieved by our approaches evaluated by the Synopsys Design Compiler tool and estimated by Eqs. (1)-(4).

Compared to the solution in [6], HRA enables to achieve a considerably higher AF_{MAX} reduction (ΔAF_{MAX}) at capture, while requiring a slightly lower AO (of approximately the 12% on average) and approximately the same #TVs, thus test time, to achieve the target FC.

Compared to the solution in [2], HRA enables to achieve a considerably higher AF_{MAX} reduction (ΔAF_{MAX}) at capture, and also a considerable reduction in the #TVs (of approximately the 34% on average), thus test time, to achieve the target FC.

Moreover, HRA repeating 4-out-of-5 bits (AF_{MAX} reduction at capture of approximately 90%) is compared to the solution in [9], which enables approximately the same AF_{MAX} (i.e., a value of WTM = 5% in [9]). HRA requires a considerably lower number of test vectors (approximately 4.87 times lower on average), thus test time, and a slightly lower area overhead (the 1.2% on average).

Therefore, compared to the recent alternate solutions in [2, 6], HRA features a significantly higher AF_{MAX} reduction at capture, thus a significantly lower PD at capture, while requiring a comparable AO, or significantly lower test time. Compared to the recent alternative solution in [9], HRA features a comparable AF_{MAX} reduction (ΔAF_{MAX}) at capture over Conv-LBIST (thus also a comparable PD reduction at capture), while requiring significantly lower test time and a slightly lower area overhead.

Finally, we have evaluated the accuracy of Eqs. (1)-(4) in evaluating the AF_{MAX} at capture achieved by LCA and HRA. Fig. 10 shows, for the four considered benchmarks, the average AF_{MAX} at capture achievable with our ap-

proaches, evaluated by simulations performed by the Synopsys Design Compiler tool and estimated by Eqs. (1)-(4).

We can observe that, for LCA, the value of AF_{MAX} at capture estimated by Eq. (1) is in very good agreement with that obtained by simulations (with a difference < 1%). Similarly, for HRA with *1-out-of-2* and *2-out-of-3* repeated bits, the values of AF_{MAX} at capture estimated by Eq. (2) and (3), respectively, are in very good agreement with those obtained by simulations (with a difference of approximately 1%). Finally, for HRA with *3-out-of-4* and *4-out-of-5*, the values of AF_{MAX} at capture estimated by Eq. (4) are in very good agreement with those obtained by simulations (with a difference of approximately 1%).

6 Conclusions

We have proposed two approaches, LCA and HRA, to reduce the PD at capture in at-speed test of sequential circuits with scan-based Logic BIST using the Launch-On-Shift scheme. LCA enables a reduction of PD at capture of up to the 50% with respect to conventional scan-based LBIST, it requires a small cost in terms of area overhead (of approximately the 1.5% on average), and it does not increase the number of test vectors, over those required by conventional scan-based LBIST, to achieve the same FC. Compared to the recent alternate solutions in [6, 2, 9] for the reduction of PD at capture in scan-based LBIST using the LOS scheme, LCA features a comparable AF in the scan chains during the application of test vectors (thus featuring a comparable PD reduction at capture), while requiring significantly lower test time or area overhead.

HRA enables scalable reductions of PD at capture of up to the 87%, at limited additional cost (in terms of area overhead and required number of test vectors to achieve a target FC) over LCA. Compared to the recent alternate solutions in [6, 2] mentioned above, HCA enables a significantly lower AF in the scan chains at capture (thus allowing a significant PD reduction at capture), while requiring a comparable area overhead, or significantly lower test time. Instead, compared to the recent solution in [9], HRA enables a similar AF in the scan chains at capture, while requiring a significantly lower test time and comparable area overhead.

Either our LCA or HRA could be more conveniently adopted for any given CUT based on the required amount of PD reduction at capture over Conv-LBIST, which is needed to minimize the likelihood to generate false test fails during the CUT at-speed test.

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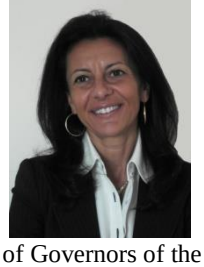
Martin Omaña received the Degree in electronics engineering from the University of Buenos Aires, Argentina in 2000 and the Ph.D. degree in electronic engineering and computer science from the University of Bologna, Italy, in 2005. He joined the University of Bologna in 2002, where he is currently a Postdoctoral Fellow. His research interests include fault modeling, on-line test, robust design, fault-tolerance, and photovoltaic systems. Dr. Omaña was a recipient of a CNR-MADESS Grant in 2002.

Daniele Rossi Daniele Rossi (M02) received the Laurea degree in electronic engineering and the Ph.D. degree in electronic engineering and computer science from the University of Bologna, Italy, in 2001 and 2005, respectively. He is currently a Senior Research Fellow at the University of Southampton, UK. His research interests include fault modeling and design for reliability and test, focusing on low power and reliable digital design, robust design for soft error and aging resiliency, and high quality test for low power systems.

Edda Beniamino received the bachelor degree in electronic engineering from the University of L'Aquila (Italy) in 2011. She received the master degree in electronic engineering from the University of Bologna in 2014. She had an internship experience as part of the thesis in Intel (Santa Clara, CA). In 2015 she received the second level master degree in Oil & Gas Plant Design from the University of Bologna in collaboration with ENI. Since July 2015 she has been working in the STAU dept. of Tecnomare S.p.A (ENI Group) as Instrumentation and Automation engineer.



Cecilia Metra is a Professor of Electronics at the University of Bologna, Italy, where she has been working since 1991, and where she received the Ph.D. in Electronic Engineering and Computer Science in 1995. In 2002, she was a Visiting Faculty Consultant for Intel Corporation in the USA. She has been Member of the Board of Governors of the IEEE Computer Society for 2013-2015, and Vice-President for Technical and Conference Activities for 2014. She is Editor in Chief of the on-line magazine "Computing Now" of the IEEE Computer Society, and member of the Editorial Boards of several professional Journals. She has been involved in the organization of several IEEE sponsored Symposia/Workshops. Her research interests are in the field of design and test of digital systems, reliable and error resilient systems' design, fault tolerance, on-line testing and fault modeling. She is an IEEE Fellow Member and a Golden Core Member of the IEEE CS, and she received three Meritorious Service Awards and two Certificates of Appreciation from the IEEE CS.

Chandrasekharan (Chandra) Tirumurti is a research scientist with the Validation and Test Solutions group at Intel Corporation based in Santa Clara, California. His current focus is on strategic manufacturing test initiatives for mainstream CPUs. An alumnus of Indian Institute of Technology, Kharagpur, India, he has wide experience in many areas of CAD and design, including simulation, data path synthesis, defect-oriented testing and fault tolerance. He has published several papers in the areas of test and fault tolerance. He mentors funded research and SRC projects actively for Intel and is an avid cricketer. He is a member of the IEEE.

Rajesh Galivanche received the MS degree in electrical and computer engineering from the University of Iowa. He is a Senior Principal Engineer in the Platforms Engineering Group at Intel. As the architect for DFT and Test Technology, he sets the strategy for research and development of design-for-test and manufacturing test technologies for Intel Core-based microprocessor and atom-based consumer SoC products. He also chaired the Intel wide task force on logic fault tolerance in Intel products. In these roles, he works closely with both the academia and the EDA industry in advancing the state-of-the-art in test and fault tolerant systems. He has published several papers in IEEE conference proceedings, three patents issued, and two patent applications pending. He served as keynote speaker in many workshops in manufacturing test and online testing related workshops. He served on the program committees of IEEE VLSI Test Symposium, and IEEE International Test Conference in the past. He is a senior member of the IEEE.