A 14mW PLL-Less Receiver in 0.18µm CMOS for Chinese Electronic Toll Collection Standard

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***Abstract*—Design of a 14mW PLL-less receiver for the Chinese electronic toll collection (ETC) system in a standard 0.18µm CMOS process is presented in this paper. Since the previously published work was mainly based on vehicle-powered systems, low power consumption is not the primary goal of such a system. In contrast, the presented system is designed for a battery-powered system. Utilizing the presented receiver architecture, the entire receiver only consumes 7.8 mA at the supply voltage of 1.8 V, which indicates a power saving of at least 38% compared with other state-of-the-art designs for the same application. To verify the performance, BER is measured to be better than 10^{-6}, which well satisfies the Chinese ETC standard. Moreover, the sensitivity of the designed receiver can be re-adjusted to -50dBm, which is required by the standard.**

***Index Terms*—ASK demodulator, electronic toll collection (ETC) and intelligent transportation system (ITS).**

I. Introduction

The electronic toll collection (ETC) system utilizing dedicated short-range communication (DSRC) at 5.8 GHz has drawn extensive attention during the past decade. Several solutions complying either with the Japanese/Korean or with the Chinese ETC standards have been presented in the literature [1-6]. The main aim of the ETC system is to exchange information between the roadside units (RSUs) and the on-board units (OBUs). In general, the RSU and the OBU are installed at the toll station and the vehicle, respectively. Both the Japanese/Korean and Chinese standards support amplitude shift key (ASK) modulation, but the required data rates are different. Since the system designed for the Japanese/Korean standard is powered by the vehicle, the primary aim is to achieve a high data rate, such as 1024 kbps and 4096 kbps with sensitivity of -60 dBm, depending on whether ASK or QPSK modulation is utilized. In contrast, the Chinese standard requires the system to be powered by a battery. Although a data rate of 256 kbps with -50 dBm sensitivity is sufficient [7] to meet the standard, the requirement of low power consumption becomes one of the critical issues, compared with previously published work in [1-5]. The trade-offs between power consumption, sensitivity and data rate need to be carefully justified, such that the best solution in terms of a figure-of-merit (FoM) for the Chinese ETC system can be achieved. In [6], a low-power receiver has been presented in a 0.13µm CMOS process for the Chinese ETC standard. Moreover, in [8], although an ultra lower power ASK demodulator is presented, but the sensitivity of the demodulator does not meet the requirement. To effectively trade-off the power consumption and sensitivity, we propose a PLL-less receiver architecture, which is fabricated in a 0.18µm CMOS process. Comparing with the work in [6], the measured results show that the receiver can achieve similar performance in terms of data rate and sensitivity with a power saving of at least 38%.

This paper is organized as follows. Section II briefly describes the design considerations and motivations for a low-power and low-data-rate receiver. The system specifications of the designed receiver are presented in Section III. In Section IV, the system architecture and circuit implementation are given. The measured results are presented in Section V, and Section VI concludes this work.

II. Design Considerations and Motivations for Low-Power and Low Data Rate Receiver

IEEE 802.15.4 is an IEEE standard for low-data-rate wireless personal-area networks (LR-WPANs), which has been established for low-power short-range wireless connectivity among portable devices, in particular at 2.4 GHz. Several approaches (such as a system approach and an operation approach) have been presented in [9-13]. Moreover, a few state-of-the-art wake-up receivers are reported in the literature, which may also be considered for the solutions of such application [14-16]. In this design, we focus on a system approach to achieve the goal of low power. As the data-rate requirement of IEEE 802.15.4 standard is similar to the Chinese ETC standard, we utilize the power consumption breakdown method as a case study to investigate how to effectively reduce the power consumption of our receiver. The typical power consumed by an IEEE 802.15.4 transceiver implemented in a 0.18µm CMOS process is in the range of 18 mW to 32 mW while the transceiver is operated in its receive mode [9-13]. The overall power consumption of the RF front-

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end and analogue baseband is less than half of the power consumed by the transceiver operating in its receive mode [9]. A similar result is also found for the design presented in [10], in which the overall power consumption of the designed receiver without PLL is only 10.8 mW. Comparing the power consumption of 10.8 mW to the power consumption of the other designs in [11-13], in which a PLL is included, shows a power saving of at least 50%. Thus, it can be concluded that both the RF front end and PLL take a large proportion of the overall consumed power in the low-power and low-data-rate low-IF receiver.

To reduce the power consumption of an ETC system, the trade-off between the consumed power and the data rate of a low-IF receiver needs to be carefully justified. As shown in [1-5], the reduction in power consumption of the overall system is not significant while the data rate goes from 4096 kbps to 1024 kbps. This is mainly due to the fact that most requirements of the RF front end and PLL remain the same, although less power is consumed at the analogue baseband due to the decreased operation frequency. Thus, the conclusion can be drawn that if a conventional low-IF architecture is chosen, the power consumption of a receiver will not be significantly reduced when the data rate goes from 1024 kbps to 256 kbps. To achieve the required sensitivity, the RF front end is always required. The remaining question is whether a PLL-less architecture can be used for the Chinese ETC system so that a significant amount of power can be saved [7].

III. System Specifications of The Designed Receiver

The system specifications of the Chinese ETC standard are quite different from the IEEE 802.15.4 standard in terms of the receiver sensitivity. In IEEE 802.15.4, the sensitivity is only defined for the worst case. Thus, the sensitivity of the receiver is the higher the better with a fixed amount of power consumption. However, in the Chinese ETC standard, the sensitivity is precisely defined to be -50 dBm. This is mainly due to the fact that each OBU should only communicate with the designated RSU in the assigned toll area so that the interference between different OBUs is minimized. As a result, the chance of getting false charging can be minimized. In order to guarantee the robustness of the designed ETC system, a 20-dB engineering margin is allowed due to device aging as well as process, voltage and temperature (P.V.T.) variations. Therefore, a sensitivity of -70 dBm is targeted in this design. To re-adjust the sensitivity of the receiver back to the required level, i.e. -50 dBm in this design, a sensitivity control scheme must be utilized. The noise figure (NF) of the receiver can be expressed as:

$$NF \le Sensitivity - \left[-174dBm/Hz + 10 \cdot \log_{10} BW\right] - SNR, \quad (1)$$

where BW is the channel bandwidth of 10 MHz and a SNR of 15 dB is required at the digital baseband. To achieve the targeted sensitivity, the NF of the receiver must be less than 19 dB. On the other hand, the linearity requirement for the Chinese ETC standard is relatively weak due to the fact that the ASK modulation scheme is utilized. There are no inter-modulation specifications defined in the standard. Instead, the maximum input power is limited to be -20 dBm, which is not difficult to achieve, if the gain of the RF front end is switchable according to the input power level.

IV. System Architecture and Circuit Implementation

The block diagram of the proposed receiver is given in Fig.1.

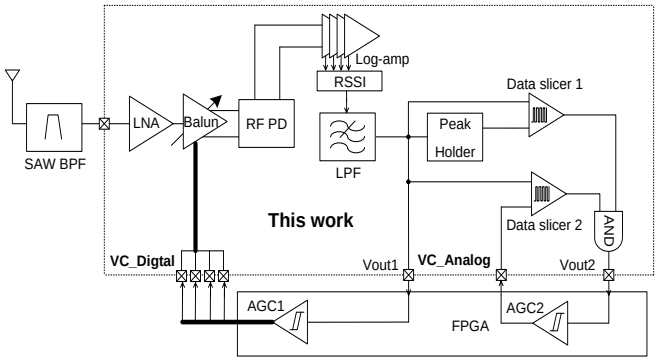

Fig. 1. Block diagram of the proposed system approach.

As can be seen from Fig. 1, two amplification stages are utilized at the RF front end. One is a fixed-gain low-noise amplifier (LNA) and the other is an active balun with variable gain functionality. A RF power detector (RFPD) is utilized to replace a down-conversion mixer while the received signal strength indicator (RSSI) and the peak holder cooperate with the data slicers to demodulate the received ASK signal. Since the strength of the received signal can vary significantly while a vehicle passes through a toll station, the RSSI is required to dynamically control the gain of the receiver. In such a way, the BER will not deteriorate. It is worth mention that a large bandwidth of the RSSI is not required, because the RF frequency has been effectively down-converted to the baseband by the RFPD block. In addition, a conventional Sallen-Key lowpass filter (LPF) is designed to remove the high-frequency noise at the output of the RSSI. The output signal of the RSSI, Vout1, is not only used for the ASK demodulation, but it is also utilized as the input signal of the automatic gain control (AGC1). The AGC1 is implemented off-chip in the FPGA, while a 4-bit digital control voltage, VC_Digital, is generated to control the gain of the active balun. The total variable gain of 32 dB with 2 dB step is achieved by the active balun, while the LNA has a fixed gain of 20 dB. By default, “1111” is generated from VC_digital to provide the highest gain. The analog signal at the Vout1 will be firstly converted to the digital stream in FPGA. If more than 10 consecutive logic-high signals are detected, then the AGC1 will decrease the gain of the active balun. On the other hand, VC_Analog is utilized to balance the trade-off between the chance of getting a false trigger and sensitivity, such that the robustness of the demodulated signal can be guaranteed. To generate VC_Analog, the AGC2 is used, which is also implemented off-chip in FPGA. It is noted that the VC_Analog needs to be adjusted first, while there is no

incoming signal at the RF front-end. During the initialization, the VC_Digital generates "1111" so that the highest gain is provided by the LNA and active balun. Then, based on the sensitivity requirement of the receiver, the VC_Analog can be accordingly adjusted by the FPGA. Once 10 consecutive logic-low signals are detected at the Vout2, the VC_Analog will be fixed and not be adjusted any more until the reset is enabled. Since the targeted sensitivity is -70 dBm, which is 20 dB better than the required specification, the sensitivity of the receiver can always be re-adjusted back to the required level through the control of VC_Analog during the initialization.

A. *Low-noise amplifier (LNA) & active balun*

As illustrated in Fig. 2, a cascode LNA is adopted at the first stage, which is designed to have a fixed gain of 10 dB and a P1dB of -15 dBm. The source inductor, L_s, is implemented by several parallel-connected bond wires while the gate inductor, L_g, is implemented by an off-chip inductor. In the second stage, two common-source (CS) amplifiers are used to form a balun, such that differential signals are generated. Each of M_3 and M_4 consists of four identical transistors, which are connected in parallel and controlled by the switches. As a result, balun also acts like a variable-gain amplifier (VGA). In the third stage, a cross-coupled-capacitors common-gate amplifier is utilized to enhance the gain without consuming any extra power [17].

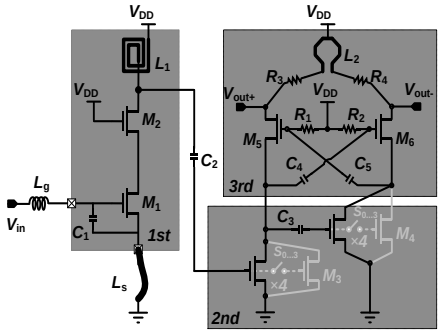

Fig. 2. Simplified schematic of the LNA and S2D VGA.

B. *RF Peak Detector (RFPD)*

In the absence of a PLL and down-conversion mixer, the frequency down-conversion is performed by the RFPD. The conventional RFPD is based on source followers as shown in Fig. 3(a).

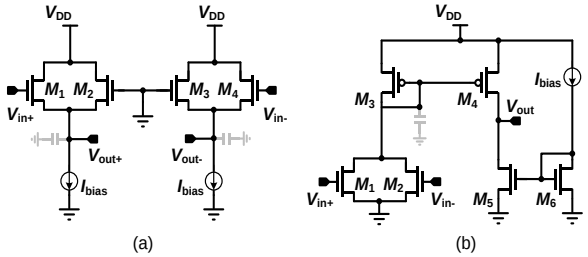

Fig. 3. Simplified schematic of the RF peak detector: (a) the conventional peak detector and (b) the RFPD used for the proposed receiver.

One of the major concerns of using source followers is that the circuit does not have any amplification capability. The input signal is inherently attenuated. Thus, it leads to a poor BER and degrades the sensitivity. To overcome this issue, a more efficient approach is presented in Fig. 3(b). The CS transistors, M_1 and M_2, are used to amplify as well as convert the voltage signal to the current domain. Then, the currents are copied through transistors $M_{3,4}$ to the output branch, in which the currents are converted back to the voltage domain.

C. *Received Signal Strength Indicator (RSSI)*

The structure of the designed RSSI is shown in Fig. 4, and is based on the successive-detection method [18]. As shown in Fig. 4, a RC network is utilized to filter out the high-frequency noise at the RSSI output. Moreover, the DC-offset voltage is extracted at the output of the limiting amplifier. Then the subtractor subtracts this DC-offset information ($V_{offset+}$, $V_{offset-}$) from the RSSI input signal ($V_{in}+$, $V_{in}-$).

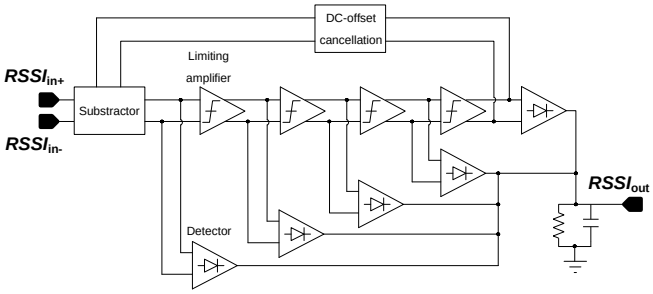

Fig. 4. Block diagram of the RSSI.

The precision of the RSSI is mainly determined by the number of sections, i.e., the number of stages of the limiting amplifier. There is a trade-off between the error and power consumption of the RSSI. A higher number of sections leads to a smaller gain error with an increased power consumption. The more detailed analysis can be found in [19]. In this design, a total gain of 40 dB is required for the receiver; four stages are utilized with a voltage gain of 12 dB at each stage to balance the gain error and power consumption. As a result, the relative error in the RSSI is smaller than 1 dB, which is satisfactory in our application.

In Fig. 5, the schematic of the limiting amplifier is shown. The diode-connected transistors, M_6 and M_7, are folded to ground as loads that parallel the input differential-pair transistors M_1 and M_2.

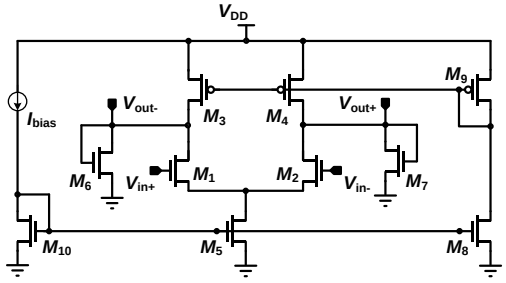

Fig. 5. The circuit implementation of the limiting amplifier.

The voltage gain of the limiting amplifier is determined by

the bias current and the device ratios. Both ratios can be designed to be insensitive to P.V.T. variations. When the signal saturates, for example, the third stage of the amplifier chain, the detector after this stage sources no current, the detectors before this stage source saturation current, and the detector of the third stage sources a variable current according to the V–I curve of the detector. The total sourcing current and the resistor R_{out} determine the output RSSI voltage. The detailed circuit implementation of the detector can be found in [18]. Although a RC LPF can be used for the DC-offset cancellation, it occupies a relatively large die area. In order to reduce the die area, two PMOS transistors are biased at their sub-threshold region so that the equivalent resistance can be controlled through the tail bias current. A larger bias current will lead to a smaller equivalent resistance; the detailed implementation can be found in [20].

D. Peak Holder and Data Slicer

A comparator is used for the data slicer. The data slicer 1 is mainly used to convert the demodulated analogue signal to the digital domain. To do so, the demodulated ASK signal is compared with the output signal of the peak holder. If the demodulated signal voltage exceeds the output signal of the peak holder, the output goes to a logic-high; otherwise, the output goes to a logic-low. As discussed in the previous section, the sensitivity of the designed receiver is targeted to be -70 dBm rather than the required -50 dBm. Thus the sensitivity of the designed receiver needs to be re-adjusted back to the Chinese ETC standard defined level. To achieve this goal, the data slicer 2 is applied as is illustrated in Fig. 1. If the output signal strength of the RSSI is not stronger than VC_Analog, regardless what the output signal of the data slicer 1 is, the AND gate is always disabled. In this way, the sensitivity of the designed receiver can be effectively controlled. Tuning the value of VC_Analog can re-adjust the sensitivity of the receiver. Moreover, it is noted that this scheme can also be used to enhance the robustness of the receiver. By increasing the value of VC_Analog, the chance of getting false trigger due to any other interference can be reduced, such that a good BER is achievable.

V. MEASUREMENT RESULTS

To verify the performance, the designed receiver is fabricated in a standard 0.18μm single-poly six-metal CMOS process. Fig. 6 shows a microphotograph of the fabricated chip and the test benches of the system, respectively. To test the function of the receiver, a previously designed 5.8 GHz ETC transmitter [21] is connected to the receiver via an attenuator while the output of the receiver is connected to a FPGA board so that the BER of the receiver can be evaluated. Meanwhile, the FPGA also provides two control signals back to the receiver. Consequently, the AGC functions can be effectively controlled by VC_Digital and VC_Analog. The measured demodulated signal at the receiver output is compared with the signal generated at the baseband of the transmitter, which are shown in Fig. 7. In Fig. 8, the calculated BER is plotted as a function of the input power with different gain settings. The BER is always better than 10^{-6}, while the input power level varies from -50 dBm to -20 dBm. As the required BER is only 10^{-5}, it is believed that the over-design margin is enough to cover BER deterioration caused by device aging and P.V.T. variations. Consequently, the sensitivity of the presented receiver can always be adjusted to the level of -50 dBm by tuning VC_Analog as discussed in the previous section. The measurement also shows that the designed receiver only consumes 7.8 mA with a 1.8V power supply, which saves at least 38% power over the one presented in [6] for the same application. Further, in Fig. 9, the measured return loss of the receiver front end is given. As illustrated, the return loss of the receiver is better than -24 dB in the relevant frequency band. The comparison between state-of-the-art designs and this work are summarized in Table I.

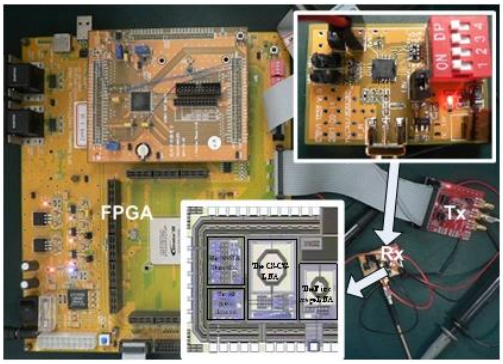

Fig. 6. Test benches of the system with die microphotograph.

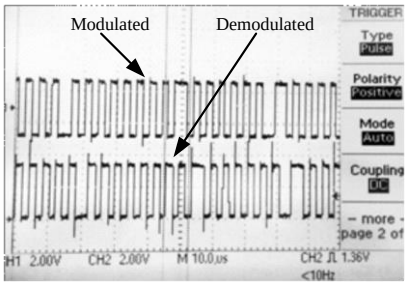

Fig. 7. The measured demodulated signal at the receiver and the signal generated at the baseband of the transmitter.

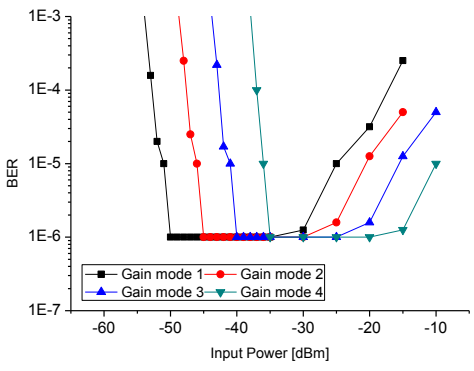

Fig. 8. The measured BER of the system with different gain settings.

TABLE I. COMPARISON OF THE STATE-OF-THE-ART DESIGNS AND THIS WORK

Reference	[1]	[2]	[3]	[4]	[5]	[6]	**This work**
Technology	SiGe BiCMOS	0.35µm SiGe BiCMOS	0.35µm SiGe BiCMOS	0.18µm CMOS	0.13µm CMOS	0.13µm CMOS	**0.18µm CMOS**
Sensitivity	N/A	N/A	N/A	-76dBm	-84dBm	-61dBm	**-50dBm**
BER	N/A	N/A	N/A	N/A	10^{-5}	N/A	**10^{-6}**
Power consumption	55mW/ 3V	65.1mA/ 3.3V	68mA/ 3.3V	52mA/ 1.8V	52mA/ 1.2V	19mA/ 1.2V	**7.8mA/ 1.8V**
Return loss	N/A	N/A	N/A	N/A	-14dB	N/A	**-24dB**

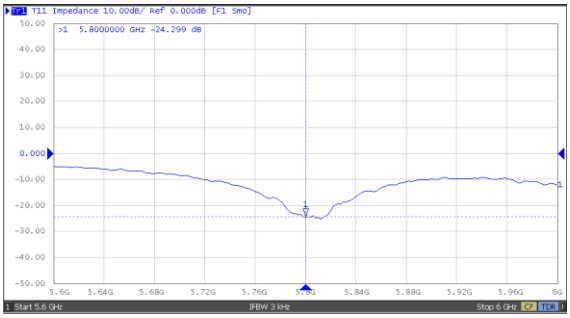

Fig. 9. The measured return loss of the receiver front end.

VI. CONCLUSION

The design of a 14mW PLL-less receiver for the Chinese ETC system has been presented in this paper. A novel system approach along with several design techniques has been utilized to reduce the power consumption of the designed receiver. To verify the performance, the designed receiver is fabricated in a 0.18µm CMOS process. The measurements show that the receiver only consumes 7.8 mA at the supply voltage of 1.8 V, which indicates a power saving of at least 38%, compared to a state-of-the-art design for the same application presented in [6]. Moreover, the calculated BER is better than 10^{-6} while the input power level varies from -50 dBm to -20 dBm, which is required by the Chinese ETC standard. The sensitivity of the receiver can also be adjusted from -70 dBm to -50 dBm by either generating the threshold voltage from a FPGA or manually tuning the threshold voltage. All in all, the designed receiver complies well with the Chinese ETC standard in terms of the sensitivity, BER and data rate. It therefore can be considered as one possible solution for the Chinese ETC system.

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