High-frequency two-input CMOS OTA for continuous-time filter applications

J.Glinianowicz, J.Jakusz, S.Szczepanski and Y.Sun

Abstract: A high-frequency fully differential CMOS operational transconductance amplifier (OTA) is presented for continuous-time filter applications in the megahertz range. The proposed design technique combines a linear cross-coupled quad input stage with an enhanced folded-cascode circuit to increase the output resistance of the amplifier. SPICE simulations show that DC-gain enhancement can be obtained without significant bandwidth limitation. The two-input OTA developed is used in high-frequency tuneable filter design based on IFLF and *LC* ladder simulation structures. Simulated results of parameters and characteristics of the OTA and filters in a standard 1.2μm CMOS process (MOSIS) are presented. A tuning circuit is also discussed.

1 Introduction

Continuous-time integrated filters have received substantial attention for high-frequency applications such as read channels in hard disc-drive systems, digital video, RF/IF filters, etc. Several integrated analogue filters with megahertz operation frequencies have been successfully implemented using the continuous-time transconductor-capacitor (Gm-C) technique [1–5].

The design of high-frequency Gm-C filters requires high-performance OTAs. One of the standard techniques to improve the CMRR, PSRR and dynamic range of analogue integrated filters is to use fully differential structures [6, 7]. Many OTAs suitable for such applications have been reported in recent years [2–5, 8–10].

The integrator is the main building block of active filters. One of the major problems in high-frequency applications is the phase error of the integrator [4, 9]. To keep the phase as close as possible to –90°, a wideband OTA with sufficiently high DC gain is required. If this can be achieved the *Q*-tuning circuit for filters will not be required.

In this paper a novel CMOS fully differential OTA with high DC gain and wide bandwidth is presented. The two-input structure is especially useful in filter design [1, 10–12], allowing to reduce the number of active components and the chip area. The proposed circuit was designed and simulated using a standard 1.2μm AMI ABN CMOS process. Application examples of filter design are also given together with a tuning system.

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2 Two-input OTA circuit description

The proposed design technique combines the cross-coupled quad input stage [5, 8–10] with the enhanced folded-cascode circuit [13–15] to increase the output resistance of the amplifier. The input stage consisting of transistors M1a–M4a and M1b–M4b in Fig. 1 is in fact a linear *V–I* converter. Using the standard square-law model for MOS transistors in their saturation region, the differential output current I_{out} can be expressed as

$$I_{out} = k_n V_B \lfloor (V_{ia+} - V_{ia-}) + (V_{ib+} - V_{ib-}) \rfloor \quad (1)$$

where $k_n = 0.5\mu_o C_{ox}(W/L)$ is the transconductance parameter (μ_o, C_{ox}, W and L are the mobility, oxide capacitance per unit area, and channel width and length, respectively), V_B is the voltage of the floating voltage source connected between points C_{R1} and C_{R2}, and $V_{ida} = (V_{ia+} - V_{ia-})$, $V_{idb} = (V_{ib+} - V_{ib-})$ are the differential input voltages. It was assumed that the transistors M1a–M4a and M1b–M4b have the same dimensions W and L. This circuit can be considered as two identical transconductance stages with output nodes connected in parallel and exhibits a perfectly linear transconductance of value $g_m = k_n V_B$. The *V–I* converter is tuneable by varying bias voltage V_B, its detailed analysis being reported in [8, 9]. As shown in Fig. 2 the control of the voltage V_B is achieved by varying the direct current I_{CF}. A similar floating voltage source of low output resistance was also described in [5, 8, 9].

The output stage employs an enhanced folded-cascode circuit and is composed of transistors M5–M12. Transistors MI17 and MI18 form the improved cascode current mirror. Since negative current-shunt feedback is used, the output resistance looking into the drains of M5/M6 is increased. Applying small-signal analysis and neglecting the body effect, the simplified expression for one of the two identical branches is given as

$$r_{d5} = r_{d6} = \lfloor r_{d9} \| r_{V-I} + r_{ds5}(1 + g_{m5} r_{d9} \| r_{V-I}) \rfloor \times (1 + g_{m7} r_{ds7}) \quad (2)$$

where $r_{d9} = r_{ds11} + r_{ds9}(1 + g_{m9} r_{ds11})$ is the output resistance of cascodes M9, M11 and M10, M12, and r_{V-I} is the

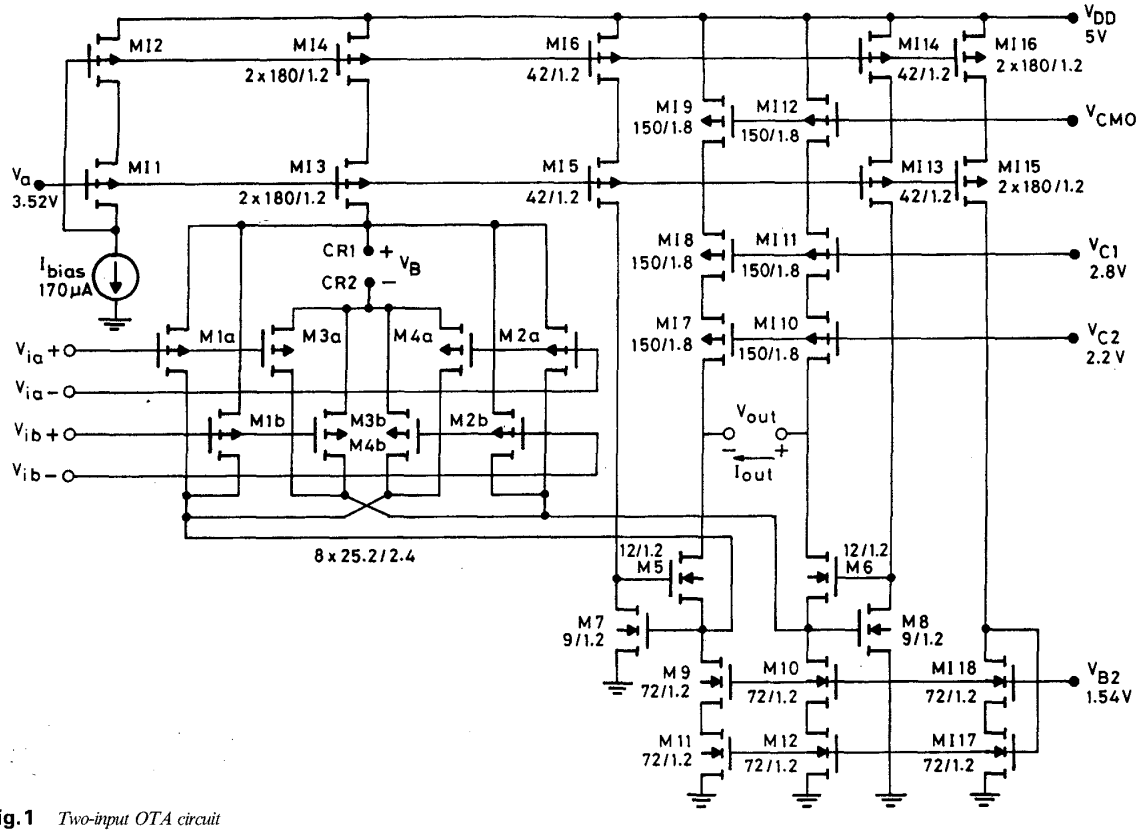

Fig. 1 *Two-input OTA circuit*

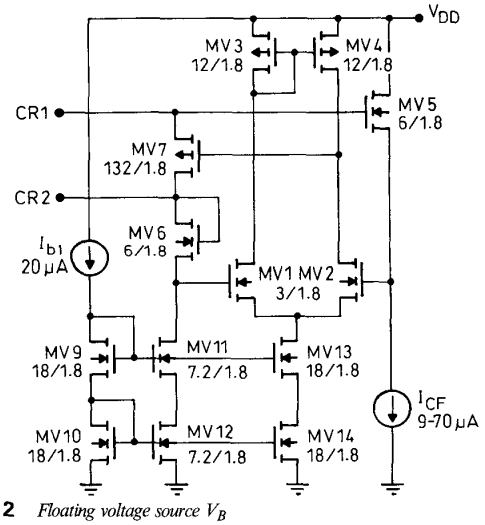

Fig. 2 *Floating voltage source V_B*

parallel connection of drain–source resistance r_{ds} of the transistors M1a, M1b, M4a, M4b or M2a, M2b, M3a, M3b. To calculate the overall differential output resistance r_{out} of the OTA in Fig. 1, the connection of p-channel transistors MI7, MI8, MI9, MI10, MI11 and MI12 forming a tripled-cascode circuit has to be taken into account. As a result, the output resistance r_{out} can be written as

$$r_{out} = 2 \cdot \{r_{d5} \| [r_{dsI7} + (1 + g_{mI7} r_{dsI7}) \times (r_{dsI8} + r_{dsI9} + g_{mI8} r_{dsI8} r_{dsI9})]\} \quad (3)$$

Thus the DC gain for both input pairs is determined as

$$A_{dDC} = g_m r_{out} \quad (4)$$

As shown in [15], DC gain enhancement by current feedback in the output cascode has no significant effect on the high-frequency response. The common-mode voltage at the output nodes is stabilised by the typical common-mode feedback loop shown in Fig. 3 [7]. The desired value is 2.5V, i.e. a half of the power supply voltage V_{DD}.

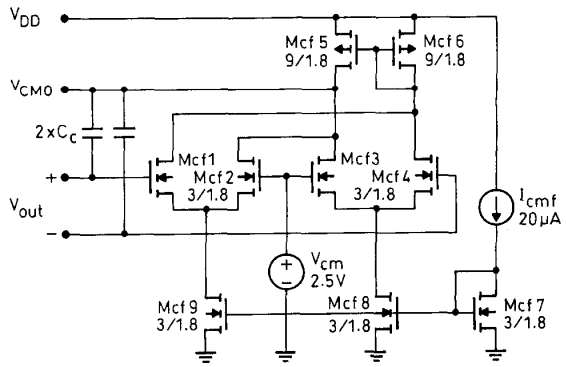

Fig. 3 *Common-mode feedback amplifier*

3 Second-order effects

Mobility reduction, body effects and channel length modulation can cause distortion in the linear transfer function in eqn. 1. An analysis of the influence of second-order effects on a similar transconductance stage has been reported in [9]. The input stage remains linear if the following scaling condition is fulfilled:

$$\frac{K_{1a,1b,2a,2b}}{K_{3a,3b,4a,4b}} = \frac{[\theta(V_q + V_{T1a,1b,2a,2b}) - 1]^4}{[\theta(V_q + V_B + V_{T3a,3b,4a,4b}) - 1]^4} \quad (5)$$

where

$$\theta = \frac{1}{T_{OX} E_{CR}} \tag{6a}$$

$$V_{Tn} = V_{To} + \gamma\left(\sqrt{\Phi - V_{BSn}} - \sqrt{\Phi}\right) \tag{6b}$$

$$V_q = -\frac{V_P + V_Q}{2} \tag{6c}$$

where K_{1a} to K_{4b} are the transconductance parameters of transistors M1a to M4b, θ is the coefficient of the effect of the electric field on the mobility, T_{OX} is the gate oxide thickness, E_{CR} is the critical field, V_{BSn} is the bulk-source voltage of transistor M_n, V_{Tn} is the threshold voltage, V_{T0} is the threshold voltage for $V_{BS} = 0$, γ is the bulk threshold parameter, Φ is the strong inversion surface potential, and V_P and V_Q are the source-gate voltages of M1a (M1b) and M2a (M2b), respectively. Because the condition in eqn. 5 is a function of tuning voltage V_B, the scaling is possible only for a given transconductance g_m of the OTA.

The channel length modulation effect of transistors M1a to M4b can be neglected owing to the application of current-shunt feedback in the output stage.

4 Simulation results

The OTA was simulated using SPICE level 3 transistor models for 1.2μm AMI ABN CMOS process. The bias current flowing through the input stage is equal to 340μA. All p- and n-channel transistors have their bulks connected to V_{DD} and GND, respectively. The main parameters of the OTA obtained from the simulation are presented in Table 1. As can be seen, the transconductance may be tuned by a decade. Implementation of the enhanced folded cascode in the output stage results in an increase of output resistance by 11 times, which increases the DC voltage gain significantly. The worst-case PSRR and worst-case CMRR were simulated assuming equal 1% mismatches in all transconductance parameters k_n and k_p, as well as in all threshold voltages V_{Tn} and V_{Tp} of MOS devices.

Table 1: Simulated results of OTA

Parameter	Value @ V_{DD} = 5 V
Transconductance range	5–50μS for I_{CF} 9–70μA
DC voltage gain	50–70dB for I_{CF} 9–70μA
THD at 10MHz, with V_{id} = 0.5V (magnitude)	< −47.1dB for I_{CF} 9–70μA
CMRR	> 46dB
PSRR	> 62dB
Equivalent input capacitance C_{in}	0.048pF
Equivalent output capacitance C_{out}	0.033pF
Power consumption	7.65mW

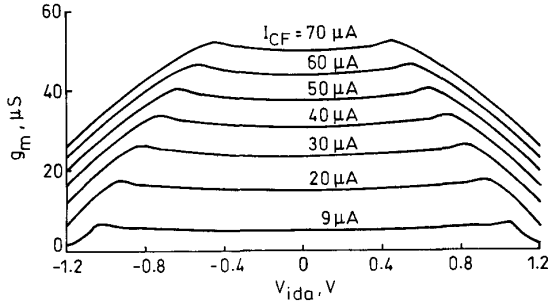

Fig. 4 *Transconductance tuning capability of complete OTA at V_{idb} = 0*

The simulated transconductance *gm* as a function of tuning current I_{CF} and input voltage V_{ida} is presented in Fig. 4. The differential voltage V_{idb} is assumed to be equal to zero. Similarly, identical characteristics can be obtained for the function of g_m against I_{CF} and V_{idb} with V_{ida} = 0. Connecting the two input pairs together doubles the transconductance achieved. As can be seen from Fig. 4 the allowed input voltage amplitude range is limited to 0.5V.

Fig. 5 shows the OTA short-circuit frequency response. The 3-dB frequency is placed in the GHz region so the OTA can be applied to high-frequency signal processing. The Gm-C integrator was simulated with the load capacitance of value 1pF connected differentially. The results are given in Fig. 6. The maximum frequency of the integrator at which the phase error is less then 1 degree, is about 85MHz. The very high DC gain is another advantage which makes the circuit very useful in systems without *Q*-tuning.

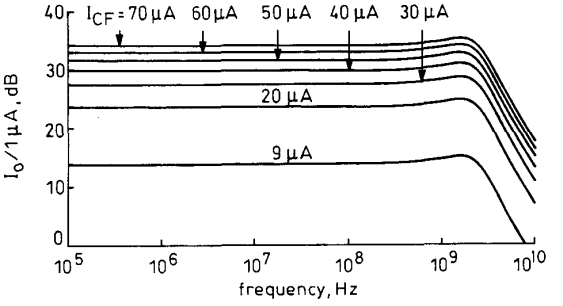

Fig. 5 *Simulated frequency response of OTA normalised to 1 μA*

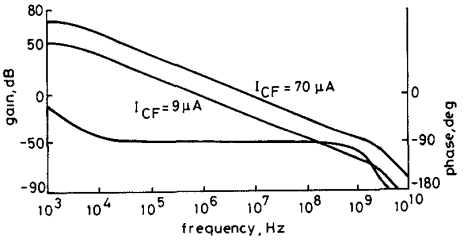

Fig. 6 *Simulated gain and phase responses of Gm-C integrator*

5 Filter examples

A tuneable 40MHz third-order elliptic filter was designed and simulated using the OTA. The normalised passive prototype and the corresponding active implementation are given in Figs. 7 and 8, respectively. The input OTA has two times the transconductance to compensate for the 6dB loss in passband. It can be seen that in every node two or four OTA stages share a capacitor. A realisation based on two-input OTAs results in the number of active elements two times lower.

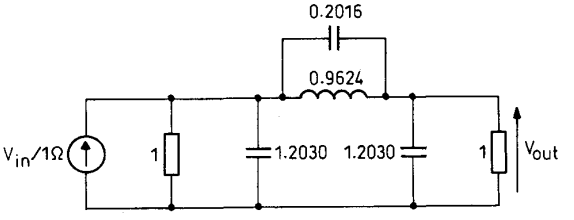

Fig. 7 *RLC prototype of third-order elliptic filter*

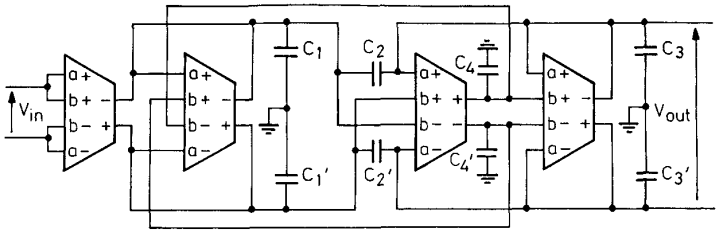

Fig. 8 *Low-pass active implementation of third-order elliptic filter based on two-input OTA*

Having in mind the accuracy of filter characteristics and the chip area, both extra and parasitic capacitances must be taken into account while designing a filter in the megahertz range. Fortunately in the filter structure considered, all input and output OTA capacitances and some extra capacitances sum which gives the following values of elements:

$C_1 = C_1' = 638\text{fF} - 2(2C_{in} + 2C_{out}) = 314\text{fF}$

$C_3 = C_3' = 638\text{fF} - 2(2C_{in} + C_{out}) = 380\text{fF}$

$C_4 = C_4' = 511\text{fF} - 2(2C_{in} + C_{out}) = 253\text{fF}$

$C_2 = C_2' = 115\text{fF}.$

Although the filter is designed to a particular frequency, it is possible to tune the cut-off frequency by varying I_{CF} in a wide range from 4 to 40MHz. High attenuation at transmission zeros is achieved owing to the excellent OTA output resistance, Fig. 9. An attenuation of the *RLC* prototype in the stopband of 28dB is achieved in active implementation.

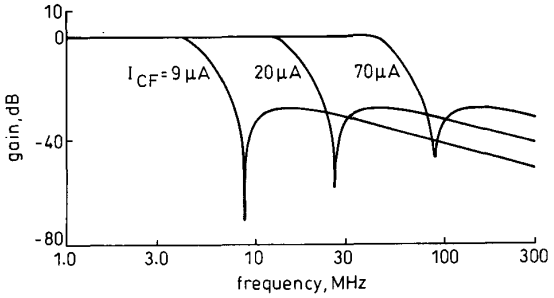

Fig. 9 *Simulated amplitude responses of elliptic filter in Fig. 8*

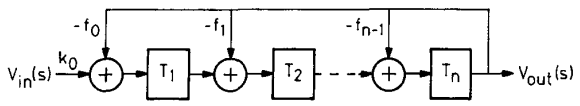

Fig. 10 *Block diagram of IFLF low-pass filter*

The two-input OTA has also been used to design a seventh-order IFLF low-pass filter. The topology of the filter is presented in Fig. 10. T_j blocks are either integrators or biquad circuits and f_j are feedback coefficients which determine the denominator of the transfer function. In general, there is a simple way to introduce gain-boost real-axis zeros or any desired transmission zeros to the transfer function by adding feedforward branches from the input to the summing nodes [1, 10–12].

The designed filter is based on the diagram in Fig. 11. Symbols 2× and 4× mean 2 or 4 unit OTAs connected in parallel. The cut-off frequency has been chosen to be 4MHz. With transconductance equal to 50μS at I_{CF} = 70μA, the following values of capacitors can be obtained:

$C_1 = C_1' = 12.64\text{pF} - 2(C_{out} + C_{in}) = 12.48\text{pF}$

$C_2 = C_2' = 5.86\text{pF} - 2(C_{out} + C_{in}) = 5.7\text{pF}$

$C_3 = C_3' = 3.62\text{pF} - 2(C_{out} + C_{in}) = 3.46\text{pF}$

$C_4 = C_4' = 2.39\text{pF} - 2(C_{out} + C_{in}) = 2.23\text{pF}$

$C_5 = C_5' = 1.71\text{pF} - 2(C_{out} + 2C_{in}) = 1.45\text{pF}$

$C_6 = C_6' = 2.12\text{pF} - 2(2C_{out} + 4C_{in}) = 1.6\text{pF}$

$C_7 = C_7' = 3.04\text{pF} - 2(4C_{out} + 11C_{in}) = 1.72\text{pF}.$

In the range of bias current I_{CF} of the OTAs the cut-off frequency of the filter varies ten times, as can be seen from Fig. 12.

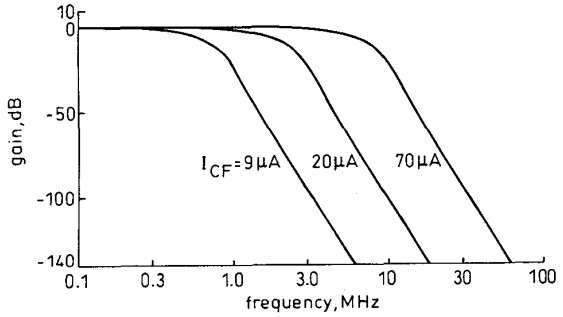

Fig. 12 *Simulated frequency response of seventh-order IFLF low-pass filter in Fig. 11*

6 Tuning system

Owing to process parameter variations, thermal effects and mismatches the tuning system is of great importance. The most common way to tune a continuous-time Gm-C circuit is a master–slave structure [3, 4]. This approach assumes a good match between the master and slave OTAs. The proposed tuning circuit consists of blocks shown in Fig. 13. This is a typical phase-locked loop (PLL) with an on-chip loop filter, thus no external components are required. The

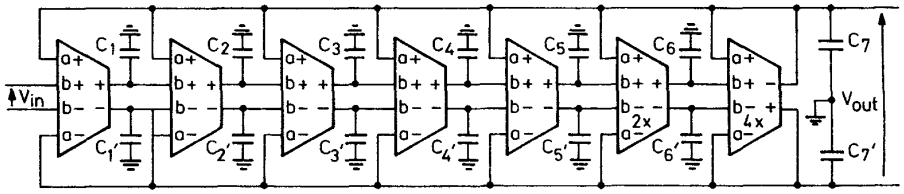

Fig. 11 *Seventh-order IFLF low-pass filter based on two-input OTA*

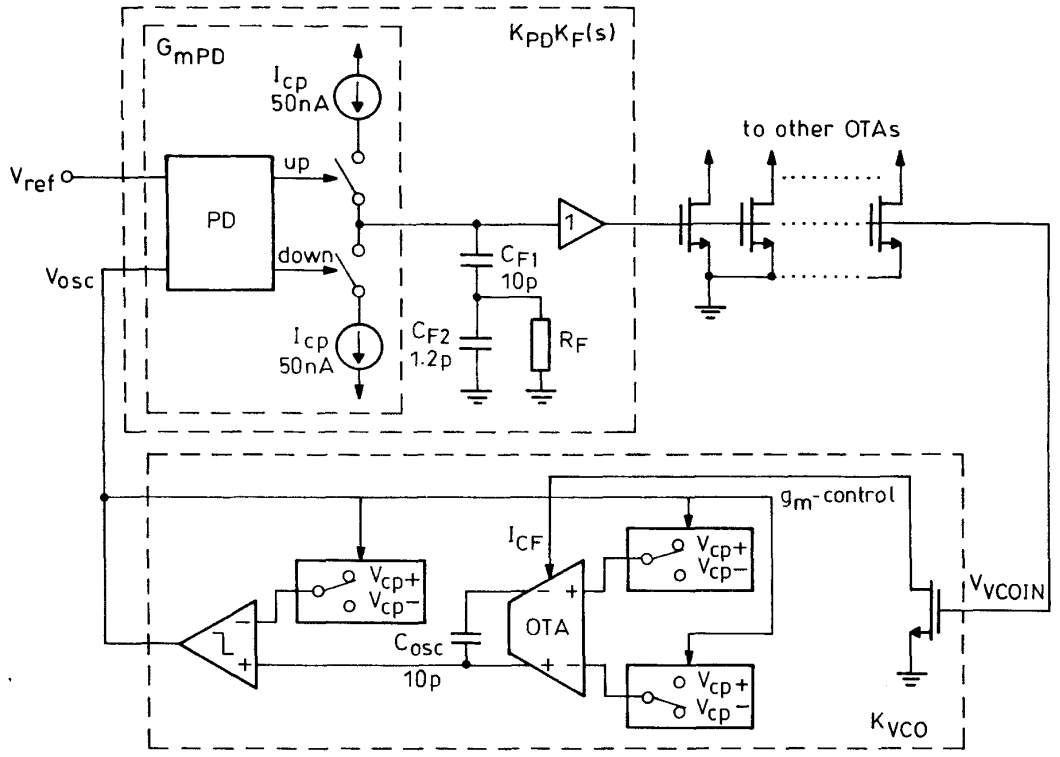

Fig. 13 *Architecture of tuning circuit*

open-loop transfer function of the PLL is written as

$$A(s) = K_{PD} \cdot K_F(s) \cdot \frac{K_{VCO}}{s} \tag{7}$$

where K_{PD} is the phase comparator gain, $K_F(s)$ represents the low-pass filter transfer function and K_{VCO} is the oscillator gain. K_{VCO} is divided by s because the frequency of the VCO output is converted to phase at the input of the phase comparator.

The phase detector subcircuit is in fact a phase–frequency one with two edge-triggered D-type flip-flops and a three-state output stage. By using current sources as the charge pump the dead zone could be reduced to zero. The PLL loop filter is of the lag–lead type, where the charge pump works as an active part. The transfer function of this block can be expressed as

$$K_{PD} \cdot K_F(s) = \frac{1 + sR_F(C_{F1} + C_{F2})}{s\frac{C_{F1}}{G_{mPD}}(1 + sR_F C_{F2})} = \frac{1 + s\tau_2}{s\tau_1(1 + s\tau_3)} \tag{8}$$

G_{mPD} is the transconductance of the charge pump, which is equal to $I_{CP}/2\pi$, i.e. 8nS. A simple RC filter can result in a very small phase margin. If a zero associated with time constant τ_2 is introduced to the filter the phase margin of the PLL can be increased to a desired value, for example, 60°, avoiding instability. Adding C_{F2} improves the attenuation of the current spikes from the phase detector. Since a typical ratio of C_{F2}/C_{F1} is about 0.1, C_{F1} can be realised as a floating capacitor between poly1 and poly2, and C_{F2} as a parasitic one to the substrate. R_F represents the resistance equivalent to the connection of several transistors polarised by a certain current. The lock range for this type of phase detector is equal to the capture range and is independent of the low-pass filter.

The connection of the tuneable Gm-C integrator based on the same OTA as those inside the filter and the comparator with hysteresis builds the VCO. Reference voltages V_{cp+} and V_{cp-} are generated internally. Increasing or decreasing the slope of the triangle voltage at the integrator's output can compensate for the changes of comparator's trip voltages with power supply. The frequency of the VCO is determined by

$$f = \frac{g_m(I_{CF})}{2C_{OSC}} = \frac{g_m(V_{VCOIN})}{2C_{OSC}} \tag{9}$$

which is independent of trip and reference voltages V_{cp+} and V_{cp-}. The transconductance $g_m(\,)$ of the OTA is tuned simultaneously with slave OTAs (forming the core of the IC) by the voltage from the phase detector/loop filter block.

7 Conclusions

A fully differential two-input CMOS OTA suitable for high-frequency analogue filter applications has been presented. The use of the two-input OTA in filter design has been illustrated, which significantly reduces the number of active elements and simplifies the structure. A tuning scheme has also been discussed. Simulation results have shown good performance of the developed CMOS OTA and its filtering applications in megahertz range. The proposed OTA can be easily expanded to have more differential inputs simply by adding more cross-coupled stages M1x–M4x connected in parallel with existing ones.

8 Acknowledgment

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