

A 0.18 μm CMOS 9mW Current–Mode FLF Linear Phase Filter with Gain Boost

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Abstract–The design and implementation of a CMOS continuous-time follow-the-leader-feedback (FLF) filter is described. The filter is implemented using a fully-differential linear, low voltage and low power consumption operational transconductance amplifier (OTA) based on a source degeneration topology. PSpice simulations using a standard TSMC 0.18 μm CMOS process with 2V power supply have shown that the cut-off frequency of the filter ranges from 55MHz to 160MHz and dynamic range is about 45dB. The group delay is less than 5% over the whole tuning range; the power consumption is only 9mW.

I. INTRODUCTION

The rapid development of battery-operated portable systems and the continuous increase of the number of different circuits and functions realized on the same chip force a reduction in power consumption. In analog circuit design, supply voltage reduction often implies major modifications of the circuit configuration, since the most important analog parameters (like speed, linearity and dynamic range) are strongly dependent on the supply voltage. For the case of computer hard disk drive (HDD), high-frequency continuous-time filters with a wide frequency tuning range are required. The linearity and dynamic range need not be very high (typically 40dB for both parameters) [1]. Read channel filters should also have programmable gain and linear phase response to equalize data pulses and minimize pulse peak shift in time, respectively. The amount of equalization and the filter group delay must be independent of each other. To achieve high speed, low voltage operation and low power consumption the most popular solution is the G_m - C type due to its open-loop structure. Several integrated continuous-time filters with high cut-off frequencies and low power consumption have been realized successfully and used for read/write channels in hard disk drive systems [2–6]. They are either based on cascade or MLF leap-frog (LF) structures. However, the work has shown that cascade structures possess higher magnitude sensitivity; filters based on simulation of passive LC ladders are not suitable for read channel applications, as

they cannot realize real zeros; MLF LF structures possess higher phase sensitivity. Analog signal processing in current domain can offer advantages for many applications and current-mode continuous-time filters have received much attention. For current signal processing and filtering, circuits are normally based on current integrators, current amplifiers, and current feedback, with current inputs to circuit nodes and current outputs from OTA output terminals. We design linear phase low-pass filters with gain boost using a current-mode MLF follow-leader-feedback filter structure, which has not previously been used for HDD applications. The filter designed has some advantages; especially it has achieved a low power consumption compared with others published designs. In this paper, our design is targeted for a cut-off frequency of 150MHz with accurate linear phase and gain boost.

The design of a fully-balanced two input four output OTA is discussed in Section II. Filter architecture and synthesis are described in Section III. The simulation results are given in Section IV, and finally conclusions are given in Section V.

II. FULLY-BALANCED OPERATIONAL TRANSCONDUCTANCE AMPLIFIER

The OTA (operational transconductance amplifier) is the dominant building block for many of the high frequency active circuit design techniques in use today. The OTA frequency and linearity characteristics directly impact on the filter performance. In this section we describe the development of a two input four output OTA. Multiple output OTA (MO-OTA) structures have been described in [7]. However, there are two drawbacks of these structures. Firstly, greater excess phase occurs due to having multiple output stages connected to a single input stage. Therefore, we add another input stage in parallel to reduce excess phase. Secondly, there is an internal node; the parasitic poles due to this affect the group delay response of the filter. This is an inherent challenge in two stage OTA design.

The presented OTA is shown below; the sources of the input transistors are connected to their substrate, which is a common P-well to prevent body effects. The presented structure uses two parallel differential pairs in the input stage. The output stages consist of eight current mirrors. The input stage currents are differentially mirrored through P-type current mirrors $M_{10,12}$ $M_{11,13}$ $M_{14,16}$ $M_{15,17}$ and N-type current mirrors $M_{18,20}$ $M_{19,21}$ $M_{22,24}$ $M_{23,25}$ to the outputs. Assuming matching between transistors, the output differential current $I_{out} = I_{output1} - I_{output4} = I_{output2} - I_{output3}$. The OTA uses two series-connected MOS transistors M_{R1} and M_{R2} in triode region [6, 8], as source degeneration resistors. The gate voltages of M_{R1} and M_{R2} are connected to the separate source followers M_9 and M_8 biased with a control current I_1 , so that both DC level shifts are identical, and tuning is obtained via I_1 without disturbing the bias current of the input stage.

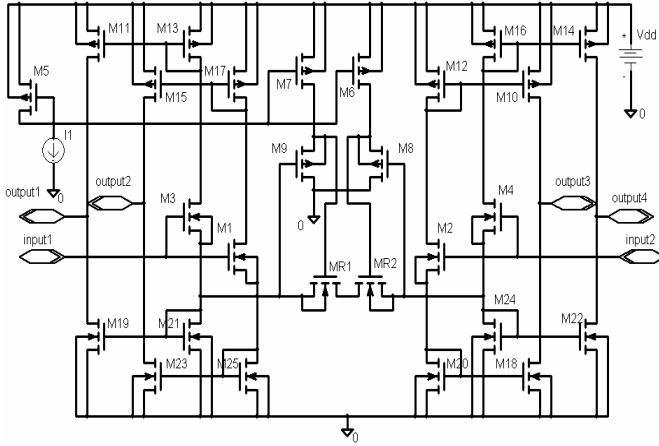


Figure 1 Fully-balanced OTA

The channel length used for these devices is the minimum length allowed by the process and the channel widths are listed as: M_1 – M_5 , $15\mu\text{m}$; M_6 , M_7 , $30\mu\text{m}$; M_8 , M_9 , $10\mu\text{m}$; M_{10} – M_{17} , $25\mu\text{m}$; M_{18} – M_{25} , $9\mu\text{m}$; M_{R1} , M_{R2} , $90\mu\text{m}$. It is worth mentioning that the geometry of the input devices also affects the DC transconductance value, and these are usually designed to be large in order to improve matching of threshold voltage V_T and K between the transconductance stages. The drain current of MOS transistors M_{R1} and M_{R2} in triode region is given by:

$$I_{R1,2} = K [(V_{GS} - V_T)V_{ds} - V_{ds}^2/2] \quad (1)$$

Where $K=0.5\mu_n C_{ox}(W/L)$ is the N-type transconductance parameter, and μ_n , C_{ox} , W and L are mobility, oxide capacitance per unit area, and channel width and length respectively. Then:

$$\begin{aligned} I_{out} &= I_{output1} - I_{output3} = I_{R1,2} - (-I_{R1,2}) \\ &= 2I_{R1,2} \end{aligned} \quad (2)$$

By substituting (2) into (1) we get:

$$I_{out} = 2K [(V_{GS} - V_T)V_{ds} - 1/2V_{ds}^2] \quad (3)$$

Note that $V_{ds} \propto V_{id}$, therefore, we get:

$$I_{out} \propto K[(V_{GS} - V_T)V_{id}] = g_m \cdot V_{id} \quad (4)$$

Where $V_{id} = V_{input1} - V_{input2}$, V_{id} is the differential input voltage and g_m is the DC transconductance of the MO-OTA given by:

$$g_m \propto K \cdot V_B \quad (5)$$

Where $V_B = V_{GS} - V_T$. From (2) and (4), we can see that the MO-OTA exhibits a linear V–I characteristic with the assumptions made. However, in practice, second-order effects such as body effects, mobility reduction, and channel length modulation will degrade the V–I function of the MO-OTA. Equation (5) shows that the transconductance value can be controlled by varying the bias voltage V_B . Thus, the allowed values of V_B determine the achievable transconductance tuning range. Figure 2 shows the simulated g_m characteristic of the MO-OTA, with the OTA outputs terminated by a short-circuit load, for different bias current I_1 .

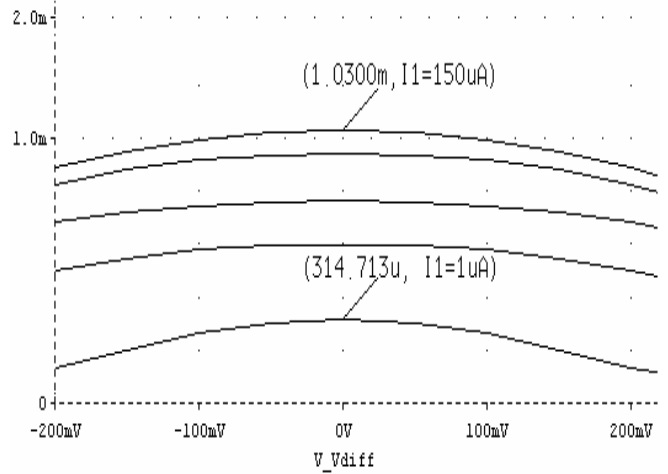


Figure 2 Simulated DC transconductance

The transconductance tuning range is from $314\mu\text{S}$ to $1030\mu\text{S}$, corresponding to values of I_1 from $1\mu\text{A}$ to $150\mu\text{A}$. The transconductance range is about 1:3.3, which is suited to HDD applications. Simulation of OTA open-circuit response with varying tuning currents is shown in Figure 3. The simulated 3dB cut-off frequencies of the OTA cell are about 612MHz and 652MHz for the minimum and maximum bias current, respectively. The DC gain is around 20dB, which is adequate for low-Q applications.

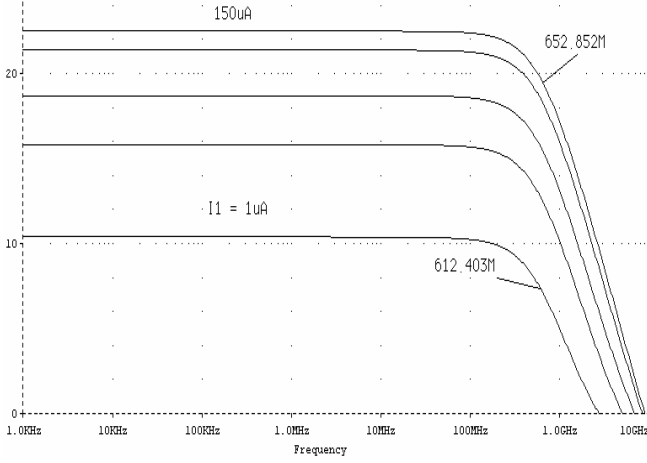


Figure 3 Simulated frequency response of OTA

III. FILTER ARCHITECTURE AND SYNTHESIS

The normalized characteristic of a seventh-order low pass equiripple linear phase filter with real zeros (3dB gain boost) at the cut-off frequency is given by:

$$H_d(s) = (s^2-1)/D(s) \quad (6)$$

With

$$D(s) = 0.055617s^7 + 0.291094s^6 + 1.095656s^5 + 2.554179s^4 + 4.255922s^3 + 4.676709s^2 + 3.176156s + 1$$

The fully balanced realization of the function in (6) using the current-mode FLF structure with output summation OTAs is shown in Figure 4. The overall transfer function of the circuit can be derived as

$$H(s) = I_{out}/I_{in} = N(s)/D(s) \quad (7)$$

Where

$$N(s) = \beta_5 \tau_6 \tau_7 s^2 + \beta_7$$

$$D(s) = \tau_1 \tau_2 \tau_3 \tau_4 \tau_5 \tau_6 \tau_7 s^7 + \tau_2 \tau_3 \tau_4 \tau_5 \tau_6 \tau_7 s^6 + \tau_3 \tau_4 \tau_5 \tau_6 \tau_7 s^5 + \tau_4 \tau_5 \tau_6 \tau_7 s^4 + \tau_5 \tau_6 \tau_7 s^3 + \tau_6 \tau_7 s^2 + \tau_7 s + 1$$

The design formulae for the equalizer can be attained by coefficient matching between (6) and (7) [9, 10].

$$\tau_1 = B_7/B_6, \tau_2 = B_6/B_5, \tau_3 = B_5/B_4, \tau_4 = B_4/B_3, \tau_5 = B_3/B_2, \tau_6 = B_2/B_1, \tau_7 = B_1, \beta_5 = 1/B_2, \beta_7 = 1$$

The resulting pole and zero parameters are:

$$\tau_1=0.19106, \tau_2=0.26568, \tau_3=0.42897, \tau_4=0.60015, \tau_5=0.91002, \tau_6=1.47244, \tau_7=3.17616, \beta_5=0.213826, \beta_7=1 \quad (8)$$

The equalizer is designed with identical unit OTAs using the CMOS OTA cell in Figure 1, with selected transconductance g_m of $800\mu S$, to improve OTA matching and facilitate design automation. The cut-off frequency of the equalizer is chosen as 150 MHz. Using the computed parameter values in (8), the capacitor values can be calculated, but the parasitic

capacitance must also be taken into account. For the circuit of Figure 1, the parasitic capacitance is about 0.2pF. The capacitance values are recalculated below:

$$C_1=C_8=0.2865pF, C_2=C_9=0.4765pF, C_3=C_{10}=0.8924pF, C_4=C_{11}=1.3283pF, C_5=C_{12}=2.3173pF, C_6=C_{13}=3.7495pF, C_7=C_{14}=7.888pF.$$

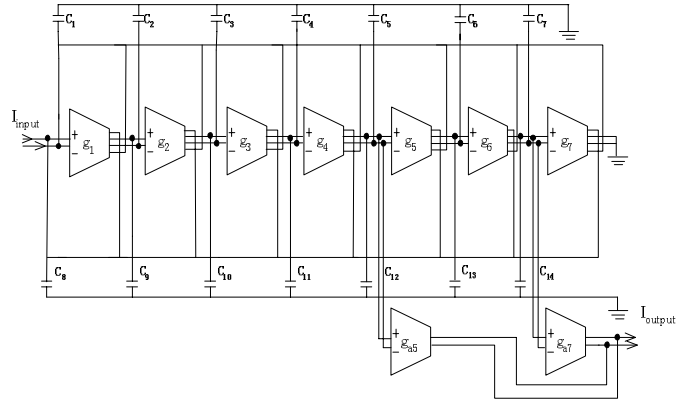


Figure 4 Seventh-order current-mode FLF OTA-C equalizer with output summation OTA network

IV. SIMULATION RESULTS

The circuit was designed and simulated using BSIM 3v3 Spice models for a TSMC 0.18 μm CMOS process available from MOSIS [11]. Figure 5 shows the magnitude response of the filter with and without the gain boost. As can be seen from Figure 5, the gain boost of the filter is about 5dB. By varying the bias current I_1 of the unit OTA cell, the tuning range of cut-off frequency without gain boost is 55–160MHz. The maximum total power consumption of the filter is about 15mW at 160MHz cut-off frequency for a single 2V power supply.

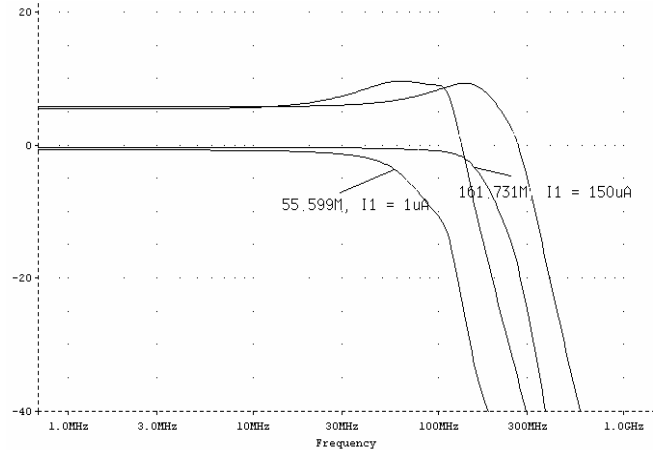


Figure 5 Simulated magnitude response of the filter without and with gain boost

The filter phase response with and without gain boost are fairly linear, as can be seen from Figure 6; the group delay has very small variation up to the cut-off frequency and it is shown that the gain boost has minimal effect on the group delay ripple of filter, with two real zeros added into the filter

response. The filter's group delay ripple for $0 \leq f \leq f_c$ is approximately 4% with the group delay below $\pm 250\text{ps}$ over the whole tuning range. This is well within the limit of the read channel filter specification. Simulation of the filter has shown a total harmonic distortion (THD) of less than 1% with a single tone of $45\mu\text{A}$ at 10MHz. The dynamic range is about 42dB and 45dB at $f_c = 55\text{MHz}$ and 160MHz, respectively.

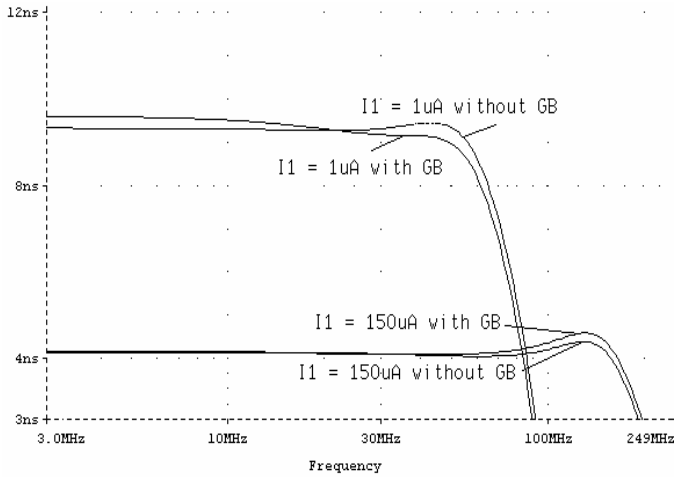


Figure 6 Simulated group delay response at $f_c=50\text{MHz}$ and 160MHz

Results from this work and some previous designs are summarized in Table 1. The performance of the filter offers significant improvements; especially the power consumption is much smaller than the other designs, making the presented filter well suitable for portable electronics products.

V. CONCLUSIONS

This paper has described a 150MHz current-mode fully-balanced seventh-order linear phase low-pass filter based on the follow-the-leader-feedback (FLF) architecture, applied to a hard disk drive read channel. A linear two-stage OTA based on source degeneration topology with a typically large transconductance has been used. Simulation results using 2V 0.18 μm CMOS show that group delay ripple is around 4%; the power consumption of proposed filter is 9mW at $f_c = 55\text{MHz}$ and 15mW at $f_c = 160\text{MHz}$. The tuning range is from 55MHz to 160MHz. These results have shown that the MLF FLF filter is well suited to HDD applications.

VI. REFERENCES

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Table 1 COMPARISON WITH OTHER 7TH-ORDER FILTER DESIGNS

Parameters	Specifications				
	[1]	[2]	[3]	[5]	This work
Reference	[1]	[2]	[3]	[5]	This work
Filter_Conf.	Cascade	VM LF	VM LF	Cascade	CM FLF
Range MHz	30-120	8-32	50-150	150-250	55-160
GDR	3%	7%	4.50%	4%	4%
DR	45dB	55dB	65dB	50dB	45dB
PC mW	120	322	216	60	9
P. Supply	2.5V	5V	2.5V	3V	2V
CMOS Tech.	0.25 μm	0.25 μm	0.25 μm	0.35 μm	0.18 μm

GDR = group delay ripple; DR = dynamic range; PC = power consumption
VM = voltage-mode; CM = current-mode