A CMOS 100MHz CONTINUOUS-TIME SEVENTH ORDER 0.05° EQUIRIPPLE LINEAR PHASE LEAPFROG MULTIPLE LOOP FEEDBACK G_m-C FILTER

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ABSTRACT

A novel 100MHz CMOS G_m-C seventh-order 0.05° equiripple linear phase low-pass multiple loop feedback (MLF) filter based on the Leapfrog (LF) topology is presented. The filter is implemented using a fully-differential linear, high performance operational transconductance amplifier (OTA) based on cross-coupled pairs. PSpice simulations in a standard TSMC 0.25μm CMOS process and with a single 5V power supply have shown that the cut-off frequency of the filter without and with gain boost ranges from 8-32MHz and 15-100MHz, respectively. With gain boost, total harmonic distortion (THD) for a differential input voltage V_{id} of 315mV_{pp} at 1MHz is less than -40dB, dynamic range at 1% THD is over 55dB, output noise with bandwidth 500MHz is only 300μV_{RMS}, and power consumption is 322mW.

1. INTRODUCTION

Modern communications and computer systems demand greatly for high performance continuous-time filters with attractive features. Filter designers confront challenges in designing filters with frequencies in VHF/GHz range, low power/low voltage, implementation using deep sub-micron technologies, simple efficient tuning techniques, and low sensitivity [1, 2]. For applications in computer hard disk drive systems, read channel filters should also have programmable gain and linear phase response to equalise data pulses and minimise pulse peak shift in time, respectively. And the amount of equalisation and the filter's group delay must be independent of each other. Most of the recent reported read channel filters are based on the well-known cascade method [3-6], however work has shown that cascade structures possess higher magnitude sensitivity than MLF filters [8, 9]. Filters based on simulation of passive LC ladders have low sensitivity, but they are not suitable for read channel applications, as they cannot realise real zeros. Recently, MLF OTA-C filters based on the inverse follow the leader feedback (IFLF) topology has been designed for read channel applications in hard disk drive systems [7]. However, no MLF OTA-C filter based on the LF configuration for such applications have been found in the literature. It is of particular interest to explore LF based MLF filters as such topology offers better performances than the IFLF structure [9]. Thus, the paper investigates the design of a 100MHz read channel equiripple linear phase G_m-C filter based on MLF LF architecture. The proposed filter is capable of realising real zeros with input OTA network [10] for programmable gain boost.

The paper is organised into four sections. Section 2 presents the OTA used, and the filter structure and design. Filter simulation results are given in Section 3, and finally major conclusions are summarised in Section 4.

2. FILTER CIRCUIT DESIGN

2.1 Operational Transconductance Amplifier

The proposed fully-differential OTA (Figure 1) is based on two cross-coupled quad cells with a cascoded current-mirror output stage. The cross-coupled input differential pairs enhance the OTA transconductance g_m linearity and overcome the conflicts between tuning range and common mode input range as occurred in source-coupled pairs. To increase output voltage swing, current-mirrors are used in the output stage, which are cascoded to compensate for decrease in GBW product due to the use of the current-mirrors. Neglecting second-order effects, the differential output current I_{out} is given by

$$I_{out} = 2K_nV_bV_{id} = g_mV_{id} \qquad (1)$$

where $K_n = 0.5\mu_nC_{ox}(W/L)_n$ is the N-type transconductance parameter, and μ_n, C_{ox}, W and L are the mobility, oxide capacitance per unit area, and channel width and length, respectively. V_b is the tuning voltage and $V_{id} = V_{in}^+ - V_{in}^-$ is the differential input voltage. $g_m = 2K_nV_b$ is the DC transconductance of the OTA, and its value is controlled by varying V_b. It is seen from (1) that the OTA exhibits a perfectly linear transconductance characteristic with the assumption made. For the filter design, a typically large g_m value of 2.5mS is used to achieve high-frequency operation of the filter.

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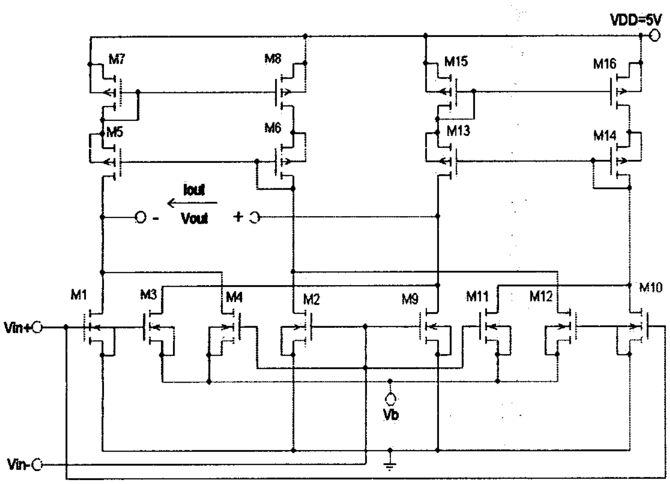

Figure 1. Unit OTA cell based on cross-coupled pairs.

2.2 Filter Synthesis

The theory and design of general all-pole and transmission zero MLF OTA-C filters including those based on the IFLF and LF topologies have been well established [10-13]. Consider the LF OTA-C filter with zero implementation in Figure 2. Using the iterative formulae presented for the universal all-pole LF configuration, together with the general transfer function of the OTA-C model with input distribution OTA network to realise gain boost zeros [10], the transfer function for the seventh-order LF filter in Figure 2 is derived as

$$H(s) = N(s)/D(s) \tag{2}$$

where $N(s) = \beta_3\tau_1\tau_2 s^2 + (\beta_3 + \beta_1)$, and

$$D(s) = \tau_1\tau_2\tau_3\tau_4\tau_5\tau_6\tau_7 s^7 + \tau_1\tau_2\tau_3\tau_4\tau_5\tau_6 s^6 + (\tau_1\tau_2\tau_3\tau_4\tau_5 + \tau_1\tau_2\tau_3\tau_4\tau_7 + \tau_1\tau_2\tau_3\tau_6\tau_7 + \tau_1\tau_2\tau_5\tau_6\tau_7 + \tau_1\tau_4\tau_5\tau_6\tau_7 + \tau_3\tau_4\tau_5\tau_6\tau_7)s^5 + (\tau_1\tau_2\tau_3\tau_4 + \tau_1\tau_2\tau_3\tau_6 + \tau_1\tau_2\tau_5\tau_6 + \tau_1\tau_4\tau_5\tau_6 + \tau_3\tau_4\tau_5\tau_6)s^4 + (\tau_1\tau_2\tau_3 + \tau_1\tau_2\tau_5 + \tau_1\tau_2\tau_7 + \tau_1\tau_4\tau_5 + \tau_1\tau_4\tau_7 + \tau_1\tau_6\tau_7 + \tau_3\tau_4\tau_5 + \tau_3\tau_4\tau_7 + \tau_3\tau_6\tau_7 + \tau_5\tau_6\tau_7)s^3 + (\tau_1\tau_2 + \tau_1\tau_4 + \tau_1\tau_6 + \tau_3\tau_4 + \tau_3\tau_6 + \tau_5\tau_6)s^2 + (\tau_1 + \tau_3 + \tau_5 + \tau_7)s + 1$$

where $\beta_j = g_{aj}/g_{mj}$ and $\tau_j = C_j/g_{mj}$ are the zero and pole parameters, respectively. Comparing the coefficients in (2) with those of the general transfer function given by

$$H_d(s) = \frac{A_2 s^2 + A_0}{B_7 s^7 + B_6 s^6 + B_5 s^5 + B_4 s^4 + B_3 s^3 + B_2 s^2 + B_1 s + 1}$$

give the design formulas as

$$\tau_7 = \frac{B_7}{B_6}, \quad \tau_6 = \frac{B_6}{B_5 - B_4\tau_7}, \quad \tau_5 = \frac{B_5 - B_4\tau_7}{B_4 - (B_3 - B_2\tau_7)\tau_6},$$

$$\tau_4 = \frac{B_4 - (B_3 - B_2\tau_7)\tau_6}{B_3 - B_2\tau_7 - [B_2 - (B_1 - \tau_7)\tau_6]\tau_5},$$

$$\tau_3 = \frac{B_3 - B_2\tau_7 - [B_2 - (B_1 - \tau_7)\tau_6]\tau_5}{B_2 - (B_1 - \tau_5 - \tau_7)\tau_4 - (B_1 - \tau_7)\tau_6},$$

$$\tau_2 = \frac{B_2 - (B_1 - \tau_5 - \tau_7)\tau_4 - (B_1 - \tau_7)\tau_6}{B_1 - \tau_3 - \tau_5 - \tau_7}, \quad \tau_1 = B_1 - \tau_3 - \tau_5 - \tau_7,$$

$$\beta_3 = \frac{A_2}{\tau_1\tau_2}, \quad \beta_1 = A_0 - \beta_3 \tag{3}$$

The normalised characteristic of a seventh-order low-pass equiripple linear phase filter with real zeros (3dB gain boost) at the cut-off frequency is given by [14]

$$H(s) = (s^2-1)/D(s) \tag{4}$$

with $D(s) = 0.055617s^7 + 0.291094s^6 + 1.095656s^5 + 2.554179s^4 + 4.255922s^3 + 4.676709s^2 + 3.176156s + 1$

The single-ended realisation of the function in (4) is as shown in Figure 2. The filter is designed with unit OTAs (Figure 1) with identical g_m of value 2.5mS to improve g_m tuning and facilitate design automation schemes. Using (3) and (4), the g_{mj}, g_{aj}, and C_j values can be computed as follows:

$g_{m1} = g_{m2} = g_{m4} = g_{m5} = 2.5$mS,

$g_{m3} = 5 \times 2.5$mS, $g_{m6} = g_{m7} = 4 \times 2.5$mS,

$g_{a1} = 2.5$mS, $g_{a3} = 4 \times 2.5$mS,

$C_1 = 5.96$pF, $C_2 = 4.01$pF, $C_3 = 16.76$pF, $C_4 = 2.95$pF,

$C_5 = 2.56$pF, $C_6 = 7.62$pF, $C_7 = 3.04$pF

In Figure 2, 4x and 5x mean parallel connections of 4 and 5 unit OTAs. The value of g_{a3} might be changed to $2g_{a3}$ or $3g_{a3}$ to give a larger gain boost of about 6dB or 9dB, respectively.

3. SIMULATION RESULTS

As the filter in Figure 2 is single-ended, the unused negative output terminal of the unit OTA (Figure 1) is grounded via a large (1GΩ) resistor. Also, a dc floating voltage (1.5V) is connected to the filter input to dc bias the OTAs for proper operation of the filter. To get the best performance, the parasitic capacitances due to the OTAs and wires are predistorted from C_j's. Figure 3 shows the magnitude response of the filter for both unboosted (input at node y, $g_{a1} = g_{a3} = 0$) and boosted (input as shown in Figure 2 with node y grounded) cases. The tuning range of cut-off frequencies without and with gain boost is 8-32MHz and 15-100MHz, respectively. The boost gain is maintained at ± 0.5dB tolerance from the design value of 3dB over the whole tuning range. Note that the filter magnitude response suffered from passband attenuation, which increases as V_b decreases. The gain loss as observed in magnitude responses is mainly due to the parasitic output conductances of the OTA. The group delay response of the filter is shown in Figure 4. Using filter group delay ripple definition [4]

$$\text{Group delay ripple} = \frac{\text{Max}[\tau(f)] - \text{Min}[\tau(f)]}{\text{Max}[\tau(f)] + \text{Min}[\tau(f)]} \tag{5}$$

where Max and Min are the maximum and minimum values of the group delay $\tau(f)$, which are taken over a specified frequency range, and the values shown in Figure 4, the filter's group delay ripple for frequency $F_c/5 \le f \le 1.1F_c$ is calculated about 7%, which is slightly higher than the minimum read channel filter specification (≤5%). This is mainly due to parasitic effects and g_m non-linearity of the unit OTA. Simulation with differential input voltage $V_{id} = V_{in} = 315mV_{pp}$ at 1MHz shows that THD is less than 1% when the tuning voltage $V_b = 0.8027V$ ($F_c = 100MHz$). All the simulations are conducted in a MOSIS TSMC 0.25μm CMOS process using a PSpice Level 7 model (BSIM3v3.1 model). Table 1 summarises the stimulated results obtained. Note the maximum differential input voltage $|V_{in}|_{max}$ in Table 1 is obtained by using its formula given in [13], that is

$$|V_{in}|_{max} = \min\left\{ \frac{V_{Tj}}{|H_j'(j\omega)|_{max}} : \text{for all related } j \right\} \tag{6}$$

where $H_j'(s)$ is the transfer function from the filter input to the differential input of the jth OTA, and V_{Tj} is the maximum linear differential input voltage of the jth OTA.

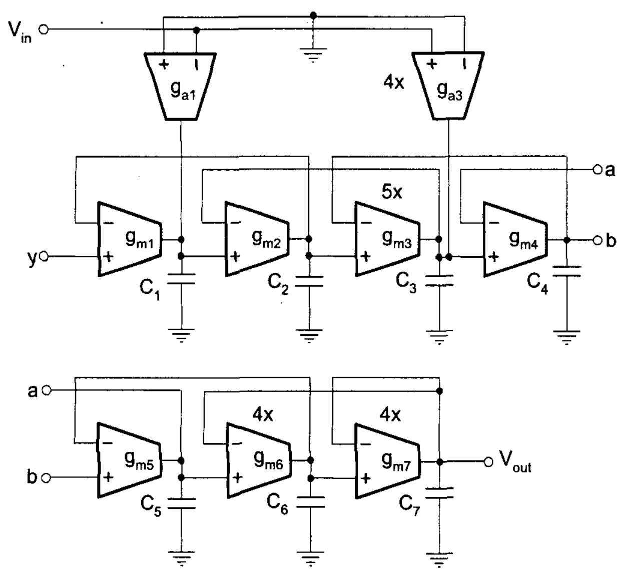

Figure 2. Seventh-order MLF LF G_m-C filter structure.

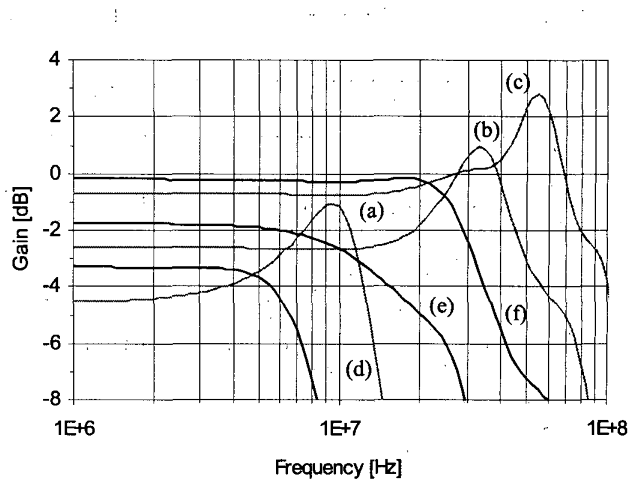

Figure 3. Stimulated magnitude response of the filter.
Thin: with boost, (a) $V_b = 0.3727V$, (b) = 0.7127V, (c) = 0.8027V
Thick: without boost, (d) = 0.3727V, (e) = 0.7377V, (f) = 1.1027V

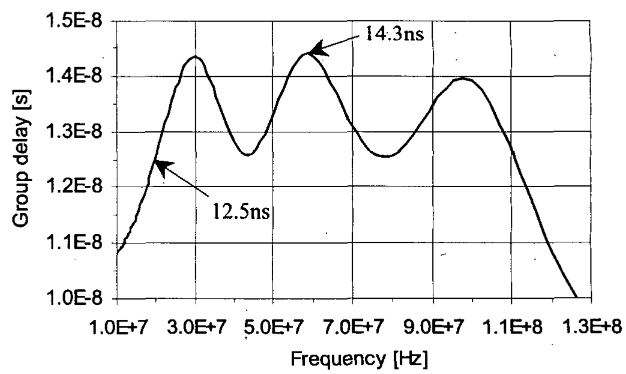

Figure 4. Stimulated group delay response of the filter with F_c = 100MHz and maximum boost.

Table 1. Summary of key filter performances stimulated with gain boost.

F_c range with gain boost	15 - 100MHz
F_c accuracy	± 5%
Gain boost range at F_c	0 - 3dB
Boost accuracy	± 0.5dB
Group delay ripple ($F_c/5 \leq f \leq 1.1\ F_c$)	7%
THD (V_{id} = 315mV_{pp} @1MHz input, F_c = 100MHz, with boost)	< -40dB
DR (THD = 1%, with boost)	> 55dB
Output noise (BW = 500MHz, with boost)	300μV_{RMS}
Maximum output voltage swing (THD = 1%, F_c = 100MHz, with boost)	500mV_{pp}
Maximum differential input voltage (with $V_{Ti} = V_T$)	$0.34V_T$
Power consumption @ 5V	322mW

4. CONCLUSIONS

A 100MHz CMOS G_m-C seventh-order 0.05° equiripple linear phase low-pass filter based on the Leapfrog (LF) architecture has been presented. A linear single-stage OTA based on cross-coupled pairs with a typically large transconductance has been used. PSpice simulations in a standard 0.25μm CMOS process with a single 5V supply voltage have shown that the filter is suitable for hard disk drive read channel applications. In particular, it should be stressed that reasonable standard simulation results were obtained just with manual fine adjustments but without actual tuning. It should be noted that better results can be expected for a fully-balanced implementation of the proposed filter. This is due to the fact that fully-balanced filter structures [15] can achieve very high common-mode rejection ratio and reduce both the even-order harmonic distortion components and the effects of power supply noise. Although work [8, 9] has shown that MLF based OTA-C filters exhibit relatively high group delay sensitivity, however reasonable group delay ripple has been obtained for the LF filter with just simple adjustments of g_m values using only floating voltages and with predistortion of capacitor values. Of course further filter performance improvements (like group delay ripple reduced to the minimum requirement of ≤5%) should be achievable by inclusion of a practical automatic tuning circuit. In addition, OTAs with higher frequency performance are important for reducing filter excess phase shifts, and thus results in reduced group delay ripple. The filter power consumption can be reduced by either scaling down the width dimension of the input MOS devices of the proposed OTA, or modifying the existing OTA to accommodate for a power supply below 5V. Other high performance OTAs are also considered.

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