A High Efficiency and Low Ripple Cross-Coupled Charge Pump Circuit

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Abstract: A fully integrated cross-coupled charge pump circuit with four-clock signals and a new method of body bias have been proposed. The new clock scheme eliminates all of the reversion power loss and reduces the ripple voltage. In addition, the largest voltage differences between the terminals of all transistors do not exceed the supply voltage. We have also solved the gate-oxide overstress problem in the conventional charge pump circuits and enhanced the reliability. The proposed charge pump circuit has been simulated using Spectre and in the TSMC 0.18um CMOS process. The simulation results show that the maximum voltage conversion efficiency of the new 3-stage cross-coupled circuit with an input voltage of 1.5V is 99.8%. Moreover, the output ripple voltage has been significantly reduced.

Key words: Cross-coupled charge pump; Reversion power loss; Ripple voltage; Four-clock signal

Proposed Charge Pump Circuit

Switched capacitor DC-DC converters or charge pumps are used to generate voltages which are higher than the supply in integrated circuits. Compared to those switched capacitor charge pumps published in the literature [1-5], in this work, a new gate cross-coupled charge pump circuit has been proposed to eliminate the reverse charge and a new bias method has also been proposed to reduce the substrate effect and improve the voltage conversion efficiency. In addition, only four-clock signal has been used in each stage, thus it is more compact than the one proposed in [6]. Traditional charge pump circuit is shown in Fig.1. This kind of circuit has the problem of reverse charge. In this paper, a four-phase clock charge pump circuit, shown in Fig. 2, is proposed to eliminate the reverse charge and a new body-side bias method is proposed to reduce the substrate effect and improve the efficiency of charge pump voltage conversion. In order to eliminate the substrate effect, all bodies of PMOS transistors are connected to the output voltage of the next stage and all bodies of NMOS transistors are connected to the input voltage of the previous stage. By these means, the leakage current has been reduced and the power supply efficiency has been optimized.

To form the gate driver circuits, four MOS transistors and two capacitors are added. In the proposed circuit, two auxiliary clock signals (CKA and CKB) are connected to two small auxiliary capacitors (C_1 and C_2). If the charge pump converters are cascaded to be an n-stage charge pump, the drive signals in the n^{th} stage should swing from nV_{DD} to $(n+1)V_{DD}$. Using the four-phase clock signal and the circuit structure proposed, the reverse loss of the charge pump has been eliminated.

The single-stage charge pump can be cascaded to obtain a higher output voltage. As a result, an n-stage charge pump without load can provide an output voltage of $(n+1)V_{DD}$. Fig. 3 shows a 3-stage charge pump based on 3 proposed single-stage charge pumps.

Simulation Results

The proposed charge pump was simulated in 0.18um CMOS technology. Simulation results of the circuit ware compared with those of [6]. Fig. 4 shows that the input voltage V_{DD} is equal to 1.5V. In the no-load condition, the output voltage of the 3-stage cross-coupled charge pump is 5.98V. The maximum voltage conversion efficiency is equal to 99.8%. In Fig. 5, the output voltages of the proposed design and other designs with different loads are compared. The proposed design works better than other designs when the load is larger than 2 kΩ.

In Fig. 6 the new charge pump is compared with the circuit in [6] with a load current of 56.21uA. The ripple voltage of the new charge pump is significantly smaller than that of the conventional cross-coupled charge pump proposed in [6].

Conclusions

This paper has presented a new charge pump structure and a new control method. The proposed structure eliminates all reversion power losses by using four non-overlapping clock signals and small auxiliary capacitors. The simulation results show a higher output voltage and low ripple voltage compared to some published results.

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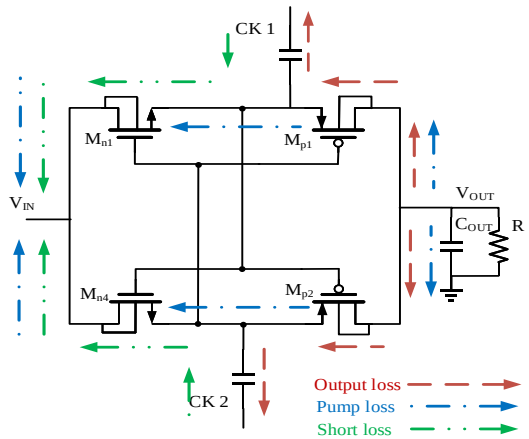

Fig.1 Conventional cross-coupled charge pump

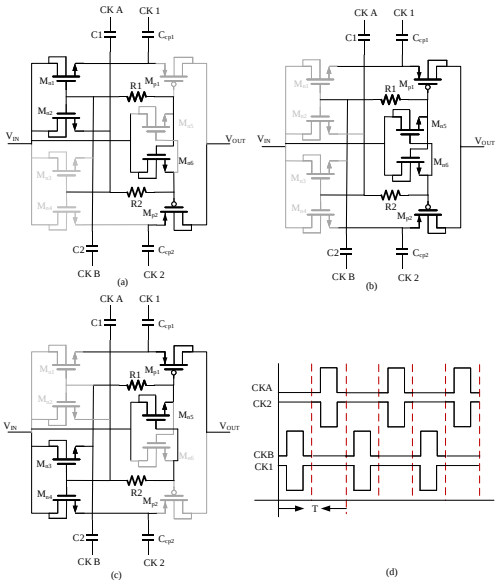

Fig. 2 The operation of proposed four phase cross-coupled charge pump

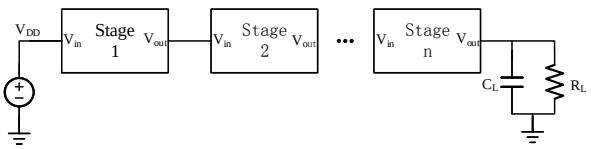

Fig. 3 Charge pump cascading for achieving a higher output voltage

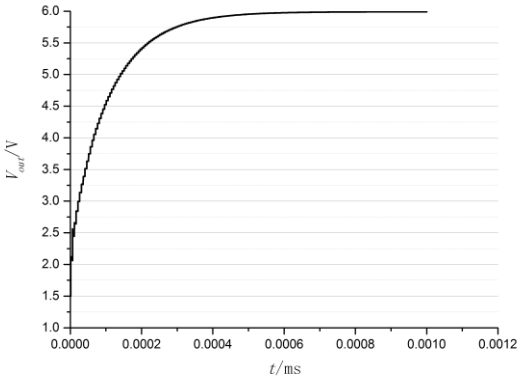

Fig. 4 Simulation of output voltage of proposed three stage charge pump

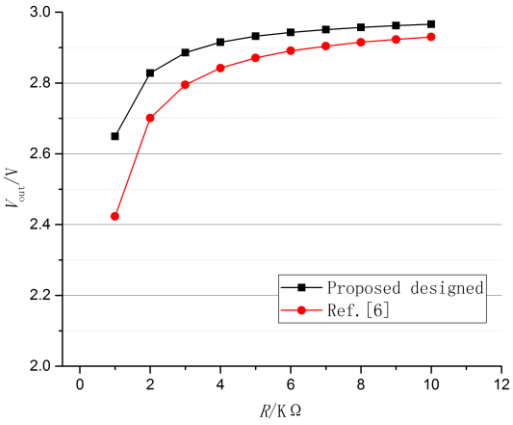

Fig. 5 Output voltage comparison of different single stage charge pump designs with different loads

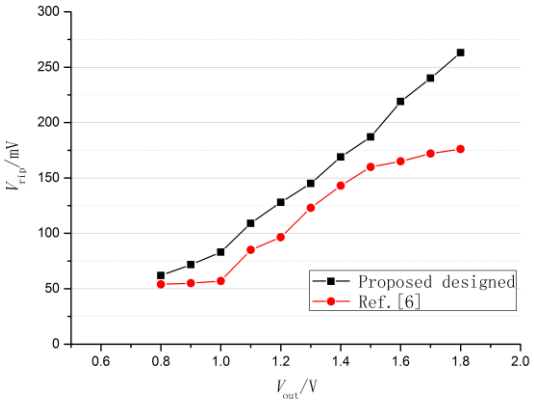

Fig. 6 Output ripple voltage comparison of different 3-stage charge pumps with different V_{out}