

A Multilevel Buck Converter Based Rectifier With Sinusoidal Inputs and Unity Power Factor for Medium Voltage (4160–7200 V) Applications

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Abstract—A novel rectifier topology for high power (0.5 to 10 MVA) current source based ac motor drives is proposed. This rectifier is composed of a multi-winding transformer, a multi-level diode rectifier and a modified multi-level buck converter. The rectifier produces near unity input power factor and sinusoidal input current under any operating conditions. In addition, the proposed rectifier features reliable operation and low manufacturing cost. In this paper, the operating principle of the proposed rectifier is introduced. A number of design issues are investigated, which include PWM switching patterns, input power factor and line current harmonic distortion. Some design considerations such as the effect of the line inductance discrepancy on system performance are addressed. Experiments on a 5 kVA/208V four-level prototype are carried out for verification.

Index Terms—Buck converter, medium voltage applications, multilevel converters, power factor control.

I. INTRODUCTION

IN MEDIUM voltage ac motor drives, an SCR rectifier is often used as a front-end converter due to its simple structure and low manufacturing cost [1]–[3]. However, the SCR rectifier injects harmonic currents into the utility grid. In addition, its power factor changes with motor operating conditions. The harmonic currents can be effectively reduced by using a twelve-pulse or eighteen-pulse rectifier configuration [4]. In the twelve-pulse configuration, two units of standard SCR rectifiers are connected to secondary windings of a twelve-pulse transformer. As a result, the *fifth*, *seventh*, *17th* and *19th* harmonic currents are canceled in the primary winding. More harmonics can be canceled when an eighteen-pulse rectifier is used. However, this configuration is unable to compensate the input power factor of the rectifier. The power factor remains low especially when the motor operates under low speeds and light load conditions.

To improve the rectifier input power factor, PWM GTO rectifiers can be employed. The use of PWM techniques has an added advantage of current harmonic elimination [5]–[7]. The GTO rectifier requires a three-phase capacitor bank connected

at its input terminals to assist the commutation of the GTO devices. However, the capacitor may be resonated with the line inductance under certain operating conditions. For example, the LC resonance might be excited by the harmonic currents produced by the rectifier, causing overvoltages. In high power applications where the equivalent damping resistance of the rectifier and utility line might be very low, some measures must be taken to suppress or eliminate the possible resonances [8].

In order to solve the above-mentioned problems, a novel current source rectifier is proposed. Fig. 1 shows a two-level buck converter based rectifier, which is composed of a multiwinding transformer, two diode rectifiers and a modified two-level buck converter. The transformer has two secondary windings with a phase shift of 30° between each other. Such an arrangement can be used to cancel low order harmonic currents generated by the diode rectifiers. The GTO buck converter provides an adjustable dc current to its load which can be a current source inverter for ac motor drives. In this paper, the two-level and three-level configurations will be introduced, followed by a detailed analysis of a four-level topology.

The proposed rectifier topologies have the following potential features.

- **Sinusoidal line current.** This is due to the use of the multi-winding transformer and multi-level diode rectifier. The dominant low order harmonic currents will be canceled by the multi-level topology and therefore will not appear in the transformer primary winding. As a result, a nearly sinusoidal line current can be achieved.

- **Near unity input power factor.** The input power factor is defined as a product of displacement power factor (DPF) and distortion factor (DF). Since the displacement power factor of the diode bridge rectifier is close to unity and the distortion factor is also close to unity due to the sinusoidal line current, a near unity input power factor can be obtained under any operating conditions.

- **No harmonic resonance.** The proposed rectifier does not require any power factor compensators or harmonic filters. As a result, resonances caused by the filters or power factor compensation capacitors used in the six-pulse or twelve-pulse SCR/GTO rectifier topologies are practically eliminated.

- **Small size of dc link choke.** In the proposed topology, the switching frequency of each GTO device is low, typically 360 Hz. However, the equivalent switching frequency at the output of the rectifier is much high, for example, 1440 Hz in the four-level configuration. The size of the dc link choke, therefore, can be reduced accordingly.

Manuscript received September 21, 2000; revised May 1, 2002. Recommended by Associate Editor L. Moran.

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Digital Object Identifier 10.1109/TPEL.2002.805600

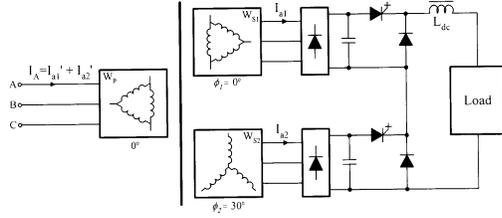


Fig. 1. Block diagram of proposed two-level buck converter based rectifier.

• **No voltage sharing problems.** In medium voltage applications, switching devices are usually connected in series to withstand the voltage. Measures should be taken to ensure equal voltage sharing among the devices both in dynamic and steady state. In the proposed rectifiers, no devices are connected in series because of the multi-level configuration.

It should be pointed out that the proposed topology requires a transformer. This may not be considered as a disadvantage in many applications. For example, in retrofit or new applications where a standard (off-the-shelf) ac motor is used, an isolation transformer between the utility supply and front-end converter is usually required to eliminate voltage stress on the motor [9], [10]. The transformer used in the proposed rectifier serves the same purpose in addition to the harmonic cancellation. Therefore, the proposed rectifier is particularly suitable for this type of applications.

II. MULTI-LEVEL RECTIFIERS AND HARMONIC ELIMINATION

A. Two-Level Buck Converter Based Rectifier

Fig. 1 shows a two-level buck converter based rectifier for use in current source fed induction motor drives. As discussed earlier, the transformer has one primary winding (W_p) and two secondary windings (W_{s1} and W_{s2}). It is assumed that the transformer is ideal and the two rectifiers are identical and three-phase balanced. It is also assumed that the transformer has the turns ratio that makes the secondary line-to-line voltages equal to half of the primary line-to-line voltages. This turns ratio ensures that the total dc voltage produced by the two rectifiers in series is the same as that of a single unit of three-phase diode rectifier directly connected to the utility grid.

The transformer windings are connected in such a way that the top secondary winding W_{s1} does not produce any phase shift with respect to the primary winding while the bottom winding W_{s2} generates a 30° phase shift. Due to the use of diode rectifiers, the secondary currents i_{a1} and i_{a2} are distorted, but they do not contain even or triplen harmonics. These two currents can be expressed as

$$i_{a1} = I_1 \sin \omega t + I_5 \sin 5\omega t + I_7 \sin 7\omega t + I_{11} \sin 11\omega t + \dots + I_n \sin n\omega t + \dots,$$

and

$$i_{a2} = I_1 \sin(\omega t + 30^\circ) + I_5 \sin 5(\omega t + 30^\circ) + I_7 \sin 7(\omega t + 30^\circ) + I_{11} \sin 11(\omega t + 30^\circ) + \dots + I_n \sin n(\omega t + 30^\circ) + \dots \quad (1)$$

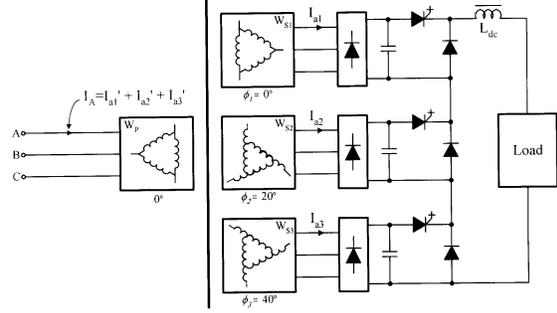


Fig. 2. Block diagram of proposed three-level rectifier.

where I_n is the amplitude of n th harmonic, $n = 1, 5, 7, 11, 13, 17, 19, \dots$

The line current i_A can be calculated by

$$i_A = i'_{a1} + i'_{a2} \quad (2)$$

where i'_{a1} and i'_{a2} are the two secondary currents, i_{a1} and i_{a2} , referred to the primary side, respectively. Since there is no phase shift between W_{s1} and W_p , the referred primary current i'_{a1} is identical to the secondary current i_{a1} except that its magnitude is reduced by half due to the transformer turns ratio, that is

$$i'_{a1} = \frac{1}{2} [I_1 \sin \omega t + I_5 \sin 5\omega t + I_7 \sin 7\omega t + I_{11} \sin 11\omega t + \dots]. \quad (3)$$

Let's now consider the other primary current i'_{a2} . All the positive-sequence current components ($n = 1, 7, 13, \dots$) in i'_{a2} are 30° behind their corresponding positive-sequence currents in i_{a2} whereas all the negative-sequence components ($n = 5, 11, 17, \dots$) in i'_{a2} are 30° ahead of their counterparts in the secondary winding (refer to Appendix I for details). The current i'_{a2} can be expressed as

$$\begin{aligned} i'_{a2} &= \frac{1}{2} [I_1 \sin(\omega t + 30^\circ - 30^\circ) + I_5 \sin(5\omega t + 150^\circ + 30^\circ) \\ &\quad + I_7 \sin(7\omega t + 210^\circ - 30^\circ) \\ &\quad + I_{11} \sin(11\omega t + 330^\circ + 30^\circ) + \dots] \\ &= \frac{1}{2} [I_1 \sin \omega t + I_5 \sin(5\omega t + 180^\circ) + I_7 \sin(7\omega t + 180^\circ) \\ &\quad + I_{11} \sin 11\omega t + \dots]. \end{aligned} \quad (4)$$

Substituting (4) and (5) into (2) yields

$$\begin{aligned} i_A &= i'_{a1} + i'_{a2} \\ &= I_1 \sin \omega t + I_{11} \sin 11\omega t + I_{13} \sin 13\omega t + \dots \end{aligned} \quad (5)$$

Equation (5) shows that two dominant current harmonics, the fifth and seventh, are eliminated due to the transformer connection. The other harmonic components (up to the 35th) and their corresponding phase angles are also calculated and listed in Table I.

B. Three-Level Buck Converter Based Rectifier

A typical three-level rectifier topology is shown in Fig. 2, where a transformer with three secondary windings having a

TABLE I
 HARMONIC CURRENTS AND THEIR PHASE ANGLES IN MULTI-LEVEL TRANSFORMERS

| n | Two-level Rectifier (Fig. 1) | | | Three-level Rectifier (Fig. 2) | | | Four-level Rectifier (Fig. 3) | | | |
|----|---------------------------------|--------------------------|---------------------------|-----------------------------------|--------------------------|-------------------------------------|----------------------------------|--------------------------|--------------------------|---|
| | $\angle I_{a1}'$ | $\angle I_{a2}'$ | $i_A = i_{a1}' + i_{a2}'$ | $\angle I_{a2}'$ | $\angle I_{a3}'$ | $i_A = i_{a1}' + i_{a2}' + i_{a3}'$ | $\angle I_{a2}'$ | $\angle I_{a3}'$ | $\angle I_{a4}'$ | $i_A = i_{a1}' + i_{a2}' + i_{a3}' + i_{a4}'$ |
| 1 | ωt | ωt | $I_1 \sin \omega t$ | ωt | ωt | $I_1 \sin \omega t$ | ωt | ωt | ωt | $I_1 \sin \omega t$ |
| 5 | $5\omega t$ | $5\omega t + 180^\circ$ | 0 | $5\omega t + 120^\circ$ | $5\omega t + 240^\circ$ | 0 | $5\omega t + 90^\circ$ | $5\omega t + 180^\circ$ | $5\omega t + 270^\circ$ | 0 |
| 7 | $7\omega t$ | $7\omega t + 180^\circ$ | 0 | $7\omega t + 120^\circ$ | $7\omega t + 240^\circ$ | 0 | $7\omega t + 90^\circ$ | $7\omega t + 180^\circ$ | $7\omega t + 270^\circ$ | 0 |
| 11 | $11\omega t$ | $11\omega t$ | $I_{11} \sin 11\omega t$ | $11\omega t + 240^\circ$ | $11\omega t + 120^\circ$ | 0 | $11\omega t + 180^\circ$ | $11\omega t$ | $11\omega t + 180^\circ$ | 0 |
| 13 | $13\omega t$ | $13\omega t$ | $I_{13} \sin 13\omega t$ | $13\omega t + 240^\circ$ | $13\omega t + 120^\circ$ | 0 | $13\omega t + 180^\circ$ | $13\omega t$ | $13\omega t - 180^\circ$ | 0 |
| 17 | $17\omega t$ | $17\omega t + 180^\circ$ | 0 | $17\omega t$ | $17\omega t$ | $I_{17} \sin 17\omega t$ | $17\omega t + 270^\circ$ | $17\omega t + 180^\circ$ | $17\omega t - 90^\circ$ | 0 |
| 19 | $19\omega t$ | $19\omega t + 180^\circ$ | 0 | $19\omega t$ | $19\omega t$ | $I_{19} \sin 19\omega t$ | $19\omega t + 270^\circ$ | $19\omega t + 180^\circ$ | $19\omega t - 90^\circ$ | 0 |
| 23 | $23\omega t$ | $23\omega t$ | $I_{23} \sin 23\omega t$ | $23\omega t + 120^\circ$ | $23\omega t + 240^\circ$ | 0 | $23\omega t$ | $23\omega t$ | $23\omega t$ | $I_{23} \sin 23\omega t$ |
| 25 | $25\omega t$ | $25\omega t$ | $I_{25} \sin 25\omega t$ | $25\omega t + 120^\circ$ | $25\omega t + 240^\circ$ | 0 | $25\omega t$ | $25\omega t$ | $25\omega t$ | $I_{25} \sin 25\omega t$ |
| 29 | $29\omega t$ | $29\omega t + 180^\circ$ | 0 | $29\omega t + 240^\circ$ | $29\omega t + 120^\circ$ | 0 | $29\omega t + 90^\circ$ | $29\omega t + 180^\circ$ | $29\omega t - 270^\circ$ | 0 |
| 31 | $31\omega t$ | $31\omega t + 180^\circ$ | 0 | $31\omega t + 240^\circ$ | $31\omega t + 120^\circ$ | 0 | $31\omega t + 90^\circ$ | $31\omega t + 180^\circ$ | $31\omega t - 270^\circ$ | 0 |
| 35 | $35\omega t$ | $35\omega t$ | $I_{35} \sin 35\omega t$ | $35\omega t$ | $35\omega t$ | $I_{35} \sin 35\omega t$ | $35\omega t + 180^\circ$ | $35\omega t$ | $35\omega t - 180^\circ$ | 0 |

n - Harmonic order

\angle - Phase angle of harmonic currents

20° phase shift between any two adjacent windings is used. The secondary currents can be written as

$$i_{a1} = \sum_{n=1, 5, 7, 11, 13, \dots}^{\infty} I_n \sin(n\omega t);$$

$$i_{a2} = \sum_{n=1, 5, 7, 11, 13, \dots}^{\infty} I_n \sin n(\omega t + 20^\circ);$$

and

$$i_{a3} = \sum_{n=1, 5, 7, 11, 13, \dots}^{\infty} I_n \sin n(\omega t + 40^\circ). \quad (6)$$

Following the same procedures discussed above, the line current can be calculated by

$$i_A = i'_{a1} + i'_{a2} + i'_{a3} \quad (7)$$

where

$$\begin{aligned} i'_{a1} &= \frac{1}{3} (i_{a1}) \\ i'_{a2} &= \frac{1}{3} \left[\sum_{n=1, 7, 13, \dots}^{\infty} I_n \sin(n\omega t + n \times 20^\circ - 20^\circ) \right. \\ &\quad \left. + \sum_{n=5, 11, 17, \dots}^{\infty} I_n \sin(n\omega t + n \times 20^\circ + 20^\circ) \right] \\ i'_{a3} &= \frac{1}{3} \left[\sum_{n=1, 7, 13, \dots}^{\infty} I_n \sin(n\omega t + n \times 40^\circ - 40^\circ) \right. \\ &\quad \left. + \sum_{n=5, 11, 17, \dots}^{\infty} I_n \sin(n\omega t + n \times 40^\circ + 40^\circ) \right]. \quad (8) \end{aligned}$$

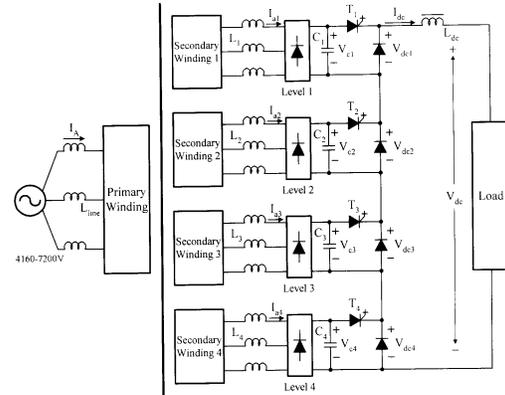


Fig. 3. Block diagram of proposed four-level rectifier.

The first term on the right hand side of (8) represents all the positive-sequence harmonic currents while the second term denotes the negative-sequence harmonic currents. According to (8), the harmonic currents and their phase angles are calculated/given in Table I. It can be seen that in the three-level rectifier, four dominant current harmonics (fifth, seventh, 11th, and 13th) are eliminated and they do not appear in the line current i_A .

C. Four-Level Buck Converter Based Rectifier

The harmonic content of the line current i_A in the four-level rectifier shown in Fig. 3 is calculated and listed in Table I as well. It can be seen that the line current does not contain any current harmonics whose order is lower than 23rd. As a result, the line current is close to sinusoidal with little distortion. The

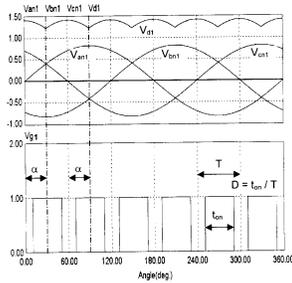


Fig. 4. Typical switching pattern and definition of gating angle α and duty cycle D .

performance of this rectifier will be analyzed in detail in the following sections.

Generally speaking, both three-level and four-level rectifiers shown in Figs. 2 and 3 can satisfy the stringent harmonic requirements specified by the IEEE Standards 519-1992 without using additional line filters. The number of levels is mainly determined by the voltage rating of the utility supply and the switching devices as well as the manufacturing cost of the rectifier. For example, with the utility line-to-line voltage of 7200 V, the average dc output voltage of the rectifier is 9720 V. Assuming that the GTO devices used in the buck converter are rated at 4500 V and the voltage safety margin for the rectifier is 1.8, the use of the four-level rectifier would give a voltage margin of 1.85 ($4500 \text{ V} \times 4/9720 \text{ V}$). We also consider to use the three-level design but the voltage rating of the switching device has to increase. The use of 6000 V devices can also achieve the voltage margin of 1.8. The design engineer in this case has to calculate the manufacturing cost of the two designs and then determine which one should be selected for construction.

III. SWITCHING PATTERN

A. Typical Switching Pattern

Fig. 4 illustrates a typical switching pattern proposed for the GTO device T_1 in the four-level rectifier, where V_{an1} , V_{bn1} and V_{cn1} are the phase voltages of the transformer secondary winding; V_{d1} is the dc output voltage of the diode rectifier with the dc filter capacitor C_1 disconnected, and V_{g1} is the gate signal for T_1 . The definition of GTO gating angle α and duty cycle D is also shown in Fig. 4. The gating signal for GTOs used in the other three buck converters is exactly the same except a 15° phase shift among each other, which is also the phase shift between the secondary windings of the transformer.

B. Switching Frequency 360 Hz

The switching frequency of high power switching devices is usually limited by the device switching characteristics. For GTO thyristors, it is typically around several hundred Hertz. An added advantage of using low switching frequencies is the low switching losses. For the multi-level configuration, it is possible to design a switching pattern with a low switching frequency for each GTO thyristor while the equivalent switching frequency at the output of the multi-level rectifier could be increased.

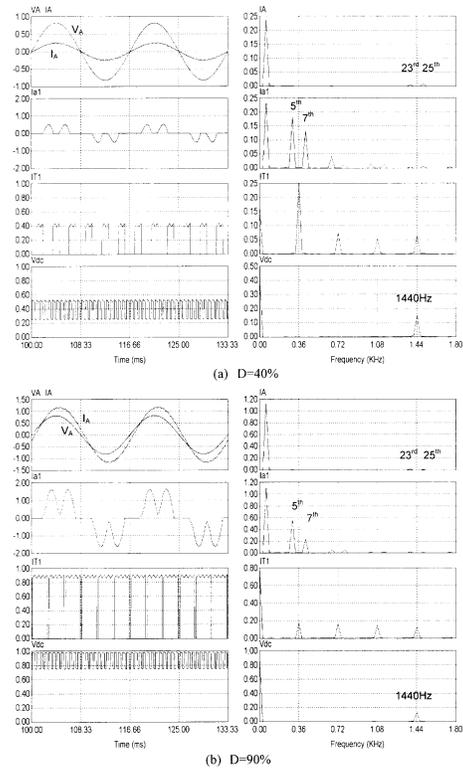


Fig. 5. Simulated waveforms at a switching frequency of 360 Hz.

Let's assume that the switching frequency of GTO thyristors is 360 Hz, which is also the frequency of the ripple voltage at the output of the diode rectifiers. This arrangement makes it possible for GTO switching to be synchronized with the ac input voltage of the diode rectifiers. Fig. 5 shows simulated waveforms when the buck converter operates at 360 Hz with a gating angle of 30° and duty cycle of 40% and 90%, respectively. The rectifier input current I_{a1} has two humps per half cycle, a typical waveform produced by the diode rectifier with a dc filter capacitor. The harmonic content of I_{a1} is also illustrated in Fig. 5. Although the rectifier input current I_{a1} is rich in harmonics, the line current I_A is nearly sinusoidal, in which the lowest order harmonic current is 23rd.

The current flowing through T_1 is also shown in Fig. 5. The GTO currents in the other three converters have exactly the same waveshape as I_{T1} except a phase shift of 15° between any two adjacent buck converters. As a result, the switching frequency that the load sees is 1440 Hz ($360 \text{ Hz} \times 4$). The relatively high switching frequency makes the dc choke size small and thus improves system dynamic performance.

C. Other Switching Frequency

Simulation results when the buck converter operates at 180 Hz and 400 Hz are shown in Fig. 6. With a switching frequency of 180 Hz, the input current of the diode rectifier I_{a1} is no longer quarter-wave symmetrical, producing even harmonic currents such as 2nd and 4th. These harmonic currents cannot be canceled by the multi-winding transformer. Fig. 6(b) shows the simulated waveforms when the buck converter has a switching frequency of 400 Hz. Since the operation of the buck converter at this

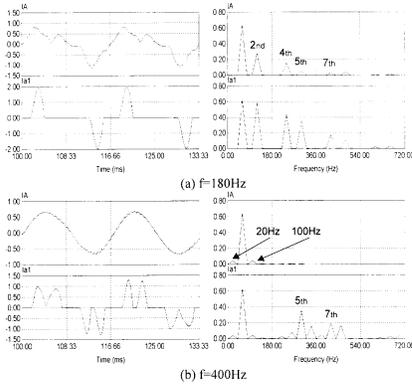


Fig. 6. Simulated results at switching frequencies of 180 Hz and 400 Hz ($D = 66.7\%$).

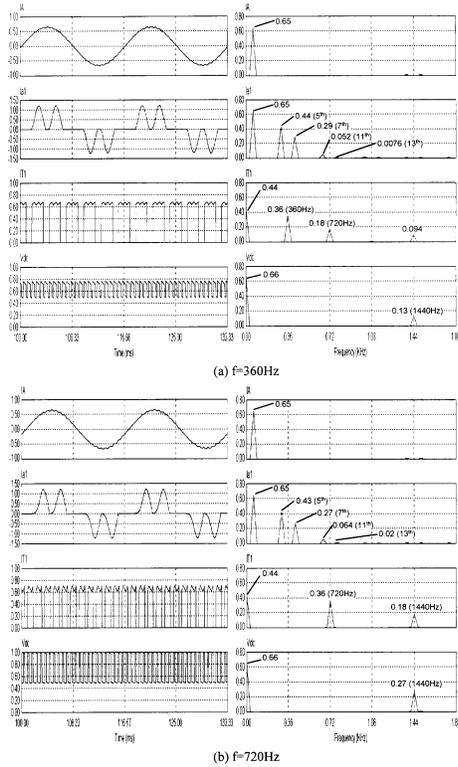


Fig. 7. Simulated results at switch frequencies of 360 Hz and 720 Hz ($D = 66.7\%$).

frequency cannot be synchronized with the diode rectifier input voltage, the rectifier input current I_{a1} is not periodical, which produces noncharacteristic (noninteger) harmonics (e.g., 20 Hz and 100 Hz components as shown in the figure). The frequency of noncharacteristic harmonics could be lower than the fundamental, and therefore it is usually difficult to eliminate them.

The simulated waveforms when the buck converter operates at 360 Hz and 720 Hz are given in Fig. 7(a) and (b), respectively. It can be observed that i) the waveforms of the line current i_A at the switching frequency of 360 Hz and 720 Hz are almost identical and ii) the waveforms and harmonic content of the rectifier input current i_{a1} are very close. This is due to the fact that the i_{a1} waveform is mainly determined by the size of the line reactor and dc link capacitor as well as the average value of the dc voltage. Therefore, the GTO switching frequency has little effect on the waveforms of i_A or i_{a1} .

It should be pointed out that the increase of the switching frequency from 360 Hz to 720 Hz does not double the equivalent switching frequency of the dc output voltage V_{dc} . As mentioned earlier, the GTO gate signals in the four-level rectifier should be 15° out of phase in order to maintain a balanced operation. When the GTO operates at 360 Hz, its switching period is $1/360$ seconds, which is equal to 60° interval of the line frequency of 60 Hz. The four GTO devices in the buck converter will be gated on one by one every 15° , resulting in an equivalent switching frequency of 1440 Hz at the rectifier output. With the GTO operating at 720 Hz, its switching period is equal to 30° interval of the line frequency. Since the GTO's should be turned on every 15° , two devices have to be gated on and off simultaneously, resulting in an equivalent switching frequency of 1440 Hz ($720 \text{ Hz} \times 2$). In addition, the 700 Hz operation also generates higher voltage ripples in V_{dc} , which is not desirable. It can be concluded from the above analysis that the switching frequency of 360 Hz is suitable for use in the proposed multi-level rectifiers.

It is interesting to note that the amplitude of the 5th and 7th harmonic currents in i_{a1} when the GTO operates at 360 Hz is negligibly higher than that shown in Fig. 7(b) whereas the amplitude of the 11th and 13th harmonic currents generated by the 720 Hz operation is negligibly higher than that shown in Fig. 7(a). This phenomenon supports our earlier claim that the GTO switching frequency has little effect on the waveforms of i_{a1} or i_A .

IV. LINE CURRENT THD AND POWER FACTOR

A. Line Current THD

The line current THD is one of the important system specifications. The level of the line current distortion is related to the line inductance, duty cycle of the buck converter, loading conditions, etc. The line inductance exhibits a high impedance for harmonic currents. The larger the line inductance, the lower the input current THD. In most cases the line inductance including the transformer leakage inductances, if any, is in the range of $0.05 \sim 0.15$ per unit.

Fig. 8 shows the THD of the line current versus duty cycle D with load resistance as a parameter. The line current THD decreases with the duty cycle as well as the load resistance. The THD at the rated load is less than 2%, suggesting that the line current is virtually sinusoidal. It should be pointed out that the line inductance used in simulation is only 0.05 pu, which is considered the worst case. The THD can be further reduced with a larger line inductance. The simulation also reveals that the value of the dc capacitor has little effects on the line current distortion, and therefore the simulation results are not presented here.

B. Input Power Factor

The input power factor is defined as

$$PF = DF \cdot DPF = \frac{1}{\sqrt{1 + THD^2}} \cdot \cos \varphi \quad (9)$$

where

$$DF = \frac{1}{\sqrt{1 + THD^2}} \quad (\text{Distortion Factor}); \quad (10)$$

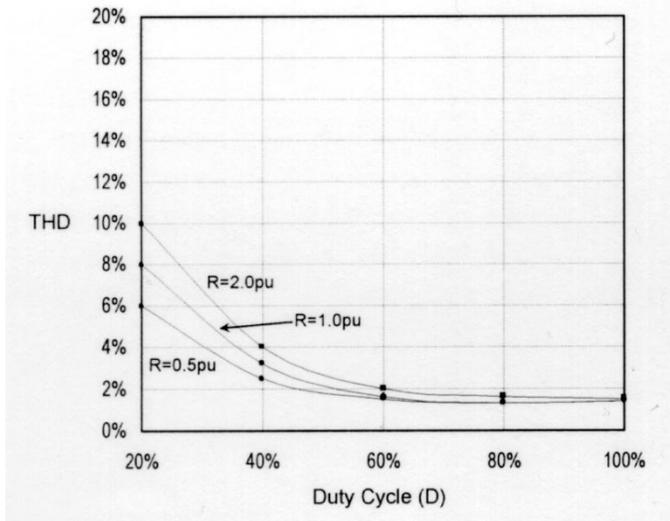


Fig. 8. Line current THD versus duty cycle D .

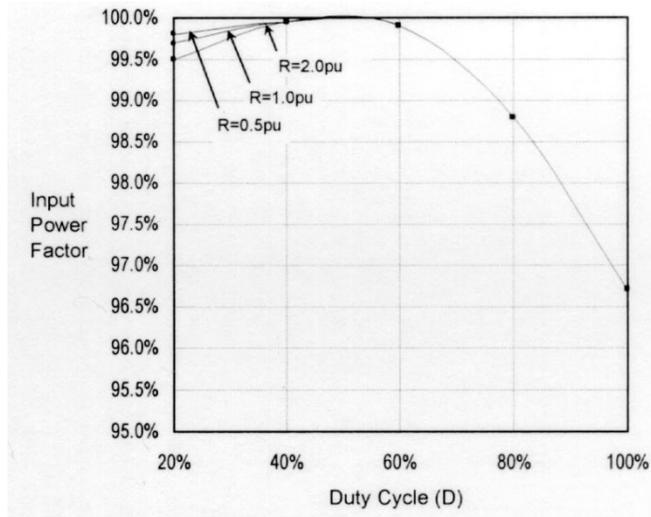


Fig. 9. Input power factor versus duty cycle D ($C = 0.5$ pu, $L_{line} = 0.05$ pu).

$$DPF = \cos \varphi \quad (\text{Displacement Power Factor}); \text{ and} \quad (11)$$

φ —phase displacement between the fundamental components of the line voltage and current.

Based on the above definition, the input power factor of the proposed four-level rectifier is calculated and presented in Fig. 9. This figure illustrates that the input power factor is mainly associated with the duty cycle. The worst case occurs at duty cycle of 100%, at which the power factor is still considered high (96.7%). This figure also indicates that the loading of the rectifier has little effect on its power factor, which is a desirable feature.

V. DESIGN CONSIDERATIONS

When designing the proposed multi-level rectifier, one should address a number of design considerations. One of the considerations is the dc voltage ripple and its relationship with system parameters. Another is the line inductance discrepancy and its effect on the current harmonic distortion. Other considerations

such as gating angle selection and secondary winding THD will also be explored.

A. Capacitor Voltage Ripple

The dc capacitor at the diode rectifier output terminals is used to reduce dc voltage ripples. In order to minimize the manufacturing cost, the size of the dc capacitor should be optimized. The dc ripple voltage ΔV_C is also affected by a number of other system parameters such as ac line inductances (including transformer leakage inductances), duty cycle of the buck converter and loading conditions. Since this is a rather complex problem, computer simulations are carried out to assist the analysis. The simulation results are presented in Fig. 10.

Fig. 10(a) shows the effects of switching duty cycle on the capacitor voltage ripple with the dc capacitor as a parameter. The ripple voltage ΔV_C is a nonlinear function of the duty cycle D . The maximum ripple voltage occurs at the duty cycle of 66.7%. This figure also shows that the ripple voltage can be decreased by increasing the dc capacitor. A substantial amount of ripple voltage reduction can be achieved when the dc capacitor is increased from 0.5 pu to 1.0 pu. The voltage ripple ΔV_C as a function of the line inductance is shown in Fig. 10(b). It can be observed that an increase in the line inductance can reduce the dc ripple voltage, especially when a small size dc capacitor is used.

As mentioned earlier, the proposed rectifier is primarily developed for use in current source based ac motor drives. When the motor operates at a reduced speed with rated torque, its stator voltage is reduced while the stator current is rated. Under this operating condition, the rectifier output voltage is reduced whereas its dc current remains rated. This implies that the equivalent load resistance R can be less than one per unit. The curves shown in Fig. 10(c) take this operating condition into account. The dc ripple voltage ΔV_C is a function of the dc current as well as the dc load resistance. When the dc resistance decreases from 1.0 pu to 0.5 pu, the ripple voltage increases from about 24% to 40% at the rated dc current. The substantial increase in ΔV_C should be considered when the rectifier is designed for use in ac motor drives.

B. Gating Angle

Further investigation is carried out to study the relationship between the GTO gating angle α and line current THD. The simulation reveals that the gating angle α has little effect on the line current THD. For example, when the buck converter operates at 360 Hz with various gating angles, the simulated waveforms and their corresponding harmonic spectra are very close to those given in Fig. 5. No substantial differences are observed, and therefore these waveforms are not provided here. However, the above stated phenomenon does not necessarily mean that the GTO gating pulses do not have to be synchronized with the utility line voltage. Without synchronization, sub-harmonic currents may be generated by the multilevel rectifier.

C. Harmonic Currents in Secondary Winding

The harmonic content of the current in the transformer secondary windings is mainly associated with the dc capacitor size and switching duty cycle. Fig. 11 illustrates the effect of the dc

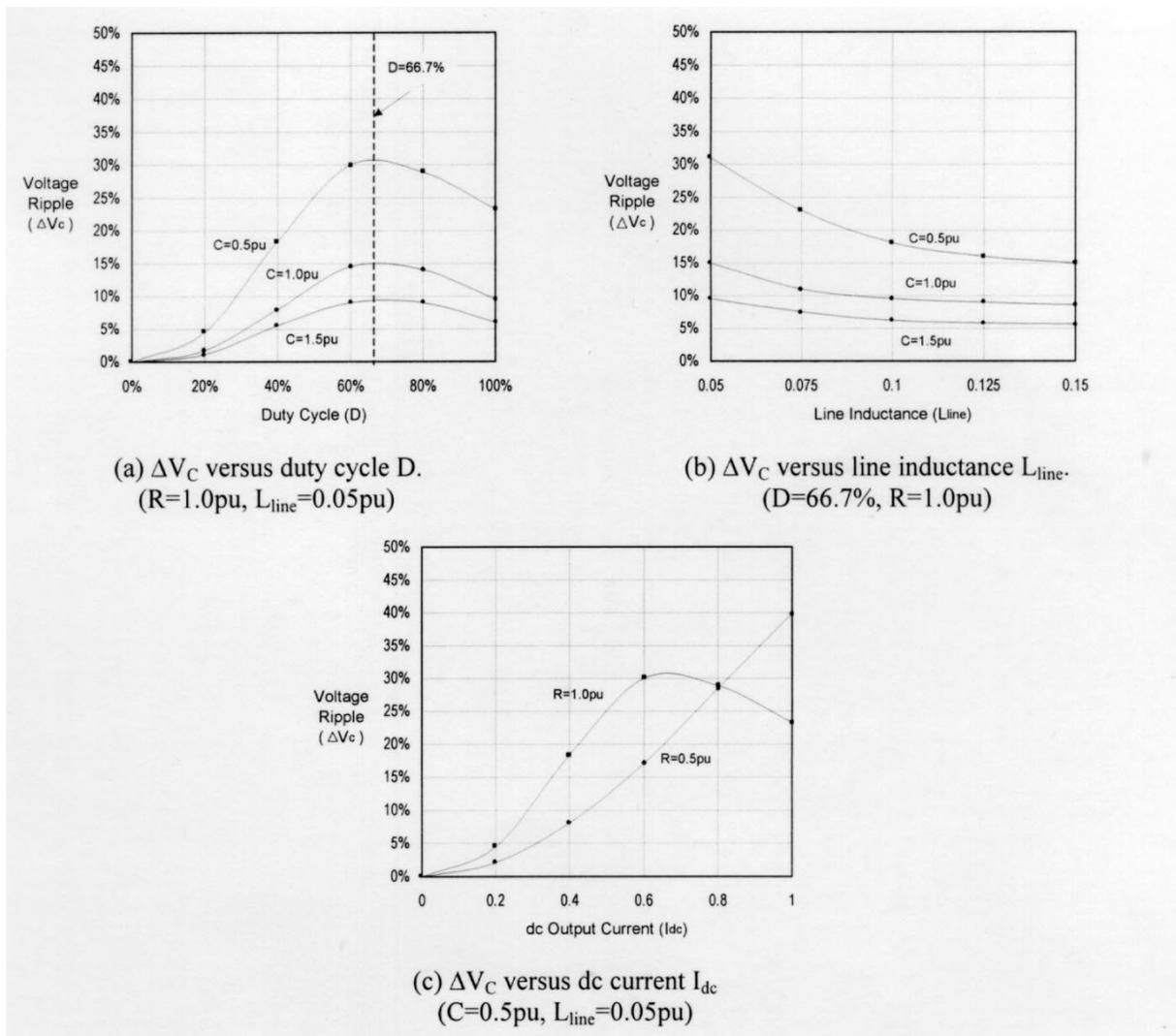


Fig. 10. Relationship between dc voltage ripple and other system parameters.

capacitor on the secondary winding current THD. It can be seen that for a given duty cycle, the smaller the size of the dc capacitor, the higher the THD value. The curves given in Fig. 12 provide a guidance for the transformer design.

D. Effects of Line Inductance Discrepancies

It is well known that the line inductance of the utility supply, to which the proposed rectifier is connected, may be variable and unbalanced. The leakage inductances of the multi-winding transformer may also be unbalanced due to the zigzag winding connection. In this section, the effect of the leakage inductance discrepancies on total harmonic distortion of the line current is investigated.

Fig. 12(a) shows the simulated waveforms of the proposed rectifier where the leakage inductance of Level-1 secondary winding is reduced by 25% while the leakage inductances of the other three secondary windings remain unchanged. The unbalanced leakage inductances make the winding currents (I_{a1} and I_{a2}) as well as their harmonic contents unbalanced. As a result, the low order harmonic currents such as 5th and 7th,

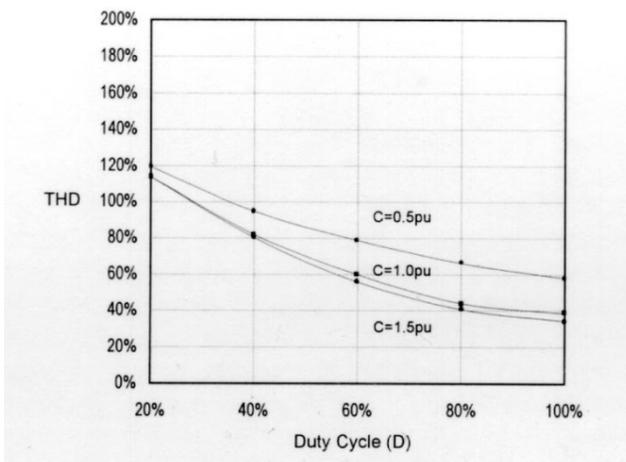


Fig. 11. Transformer secondary winding current THD versus duty cycle D ($R = 1.0 \text{ pu}$, $L_{line} = 0.05 \text{ pu}$).

which should be canceled by a balanced transformer, appear in the line current I_A . Fig. 12(b) shows the simulated waveforms

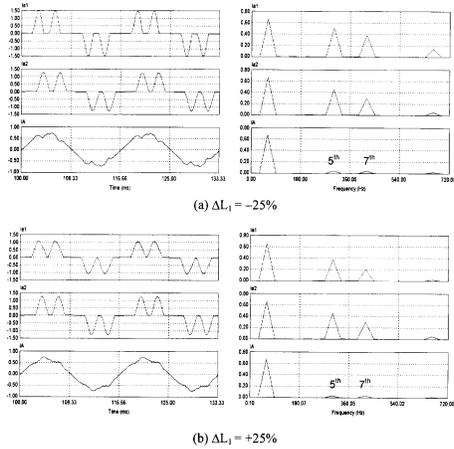


Fig. 12. Effects of line inductance discrepancy on line current I_A ($D = 66.7\%$).

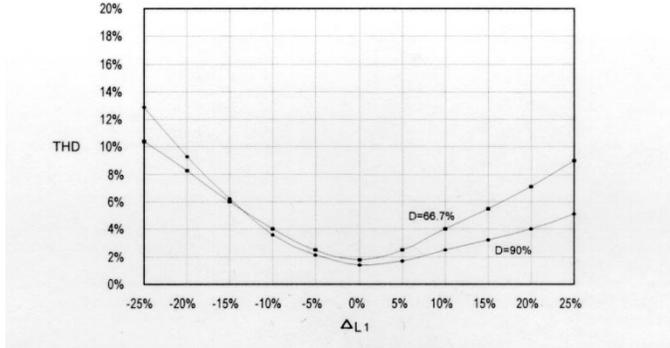


Fig. 13. Relationship between the line current THD and discrepancy of leakage inductance ($C = 0.5$ pu, $R = 1.0$ pu).

when the leakage inductance of Level-1 secondary winding has a 25% increase. Low order harmonics start to appear due to the unbalanced operation.

Fig. 13 shows the relationship between the line current THD and the discrepancy in the leakage inductance. Obviously, the total harmonic distortion reaches the minimum when the transformer leakage inductance is balanced. Therefore, efforts should be made in minimizing the leakage inductance discrepancies when the transformer is designed.

VI. EXPERIMENTAL RESULTS

A 5 kVA/208 V prototype system with a four-secondary-winding ($52\text{ V} \times 4$) transformer is built. The control and the gating pulse generation for the prototype rectifier are implemented by using a TMS320C31 based DSP board. The dc capacitor is 1.0 pu and the load resistance is 1.0 pu. The measured waveforms of the rectifier with the duty cycle of 40% and 90% are shown in Figs. 14 and 15, respectively, where V_A and I_A are the rectifier input phase voltage and line current, V_{a1} and I_{a1} are the voltage and current in the transformer secondary winding. Also included in the figures are the dc capacitor voltage V_{c1} , the GTO device current I_{T1} , the output dc voltage of the multi-level rectifier V_{dc} and the dc voltage of Level-1 buck converter V_{dc1} . The measured waveforms are in a good agreement with the simulated ones given in Fig. 5. In

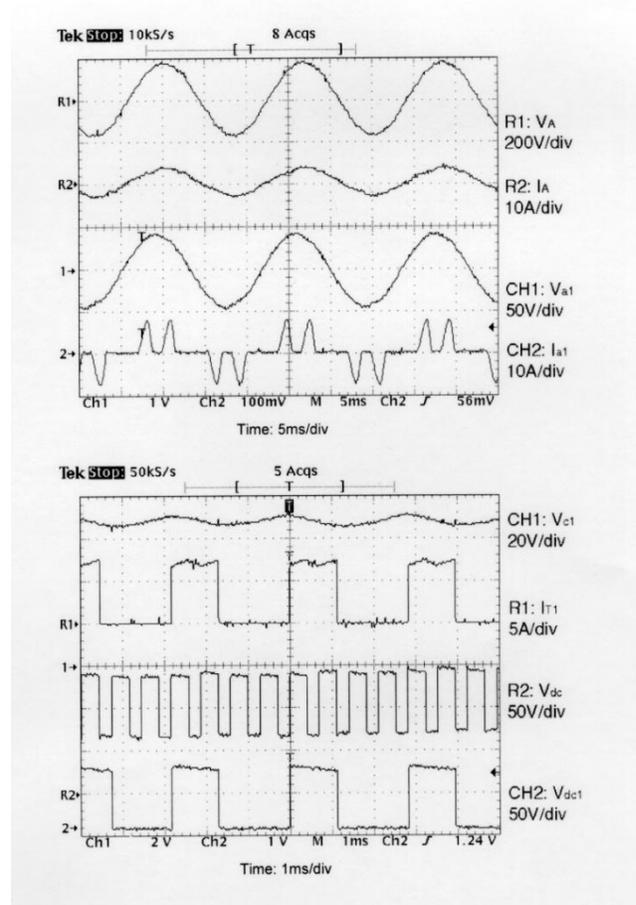


Fig. 14. Experimental results with 40% switching duty cycle.

addition, it can be observed from measured waveforms that the input current is nearly sinusoidal and the power factor is close to unity. The theoretical analysis is verified.

In order to demonstrate the effects of transformer leakage inductance discrepancies, external air-core inductors are connected in series with the transformer secondary windings such that the equivalent leakage inductance of the secondary windings can be increased or decreased. Fig. 16 shows the experimental results when the leakage inductance of Level-1 secondary winding (L_1) is increased and decreased by 25%, while other system parameters remain unchanged. It can be seen that the unbalanced leakage inductances make the secondary winding currents, I_{a1} and I_{a2} , unbalanced. As a result, the harmonic currents in the primary winding cannot be canceled, producing the distorted line current I_A . The experimental waveforms are similar to the simulated ones given in Fig. 12.

VII. CONCLUSIONS

A novel multi-level current source rectifier for medium voltage (4160–7200 V) applications is proposed. Important design issues such as switching pattern, switching frequency, input power factor and line current harmonic distortion are investigated. A number of design considerations including the size of dc capacitor and the effect of unbalanced transformer parameters are discussed. Some of the useful results are plotted for the designer to use. The rectifier has two main

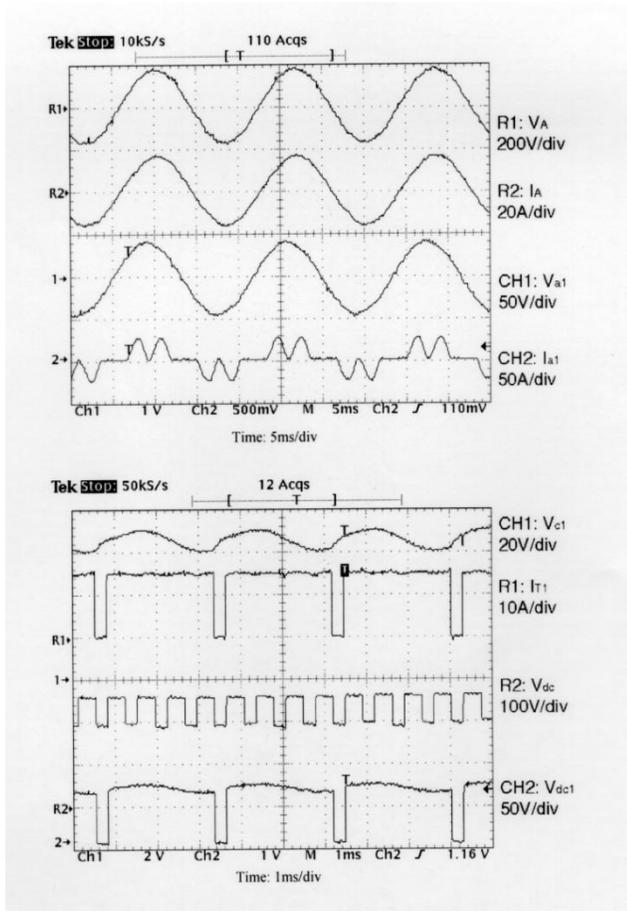


Fig. 15. Experimental results with 90% switching duty cycle.

features: high input power factor and low current harmonic distortion. In addition, the rectifier does not have GTO voltage sharing problems nor line side LC resonant problems. These features make the proposed rectifier very attractive in medium voltage applications. Laboratory experiments on a 5 kVA DSP controlled four-level prototype are carried out to verify the theoretical analysis.

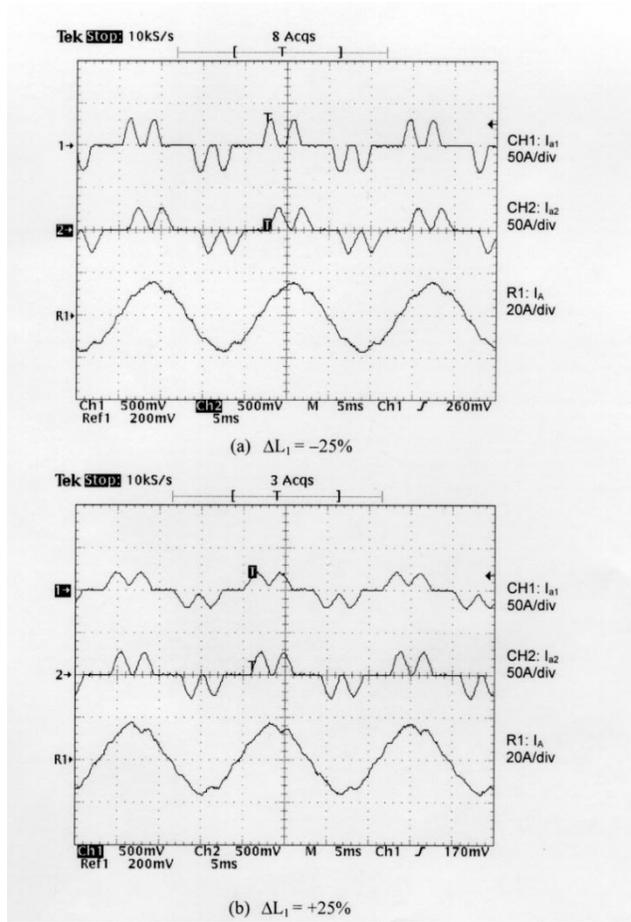
APPENDIX I

PHASE SHIFT OF HARMONIC CURRENTS IN THREE-PHASE TRANSFORMERS

The main purpose of this appendix is to investigate the phase shift of harmonic currents in the transformer primary and secondary windings. It is the phase shift in multi-winding transformers that makes it possible to cancel some harmonic currents produced by the nonlinear load of the transformer.

The circuit diagram of a Δ/Y connected three-phase transformer is shown in Fig. 17. It is assumed that the transformer is ideal and its load is three-phase balanced. The phasor diagram shown in the figure indicates that the secondary line-to-line voltage V_{ab} leads the primary line-to-line voltage V_{AB} by an angle ϕ , which is 30° in this case.

Assuming that a three-phase nonlinear load, such as a diode or SCR rectifier, is connected to the transformer secondary


 Fig. 16. Experimental waveforms with unbalanced transformer leakage inductances ($D = 90\%$).

winding, the secondary currents (i_a , i_b and i_c) will be distorted, but they will not contain even or triplen harmonics, that is,

$$i_a = I_1 \sin \omega t + I_5 \sin 5\omega t + I_7 \sin 7\omega t + I_{11} \sin 11\omega t + I_{13} \sin 13\omega t + \dots \quad (A1)$$

$$i_b = I_1 \sin \omega t + I_5 \sin 5(\omega t - 120^\circ) + I_7 \sin 7(\omega t - 120^\circ) + I_{11} \sin 11(\omega t - 120^\circ) + I_{13} \sin 13(\omega t - 120^\circ) + \dots \quad (A2)$$

$$i_c = I_1 \sin \omega t + I_5 \sin 5(\omega t - 240^\circ) + I_7 \sin 7(\omega t - 240^\circ) + I_{11} \sin 11(\omega t - 240^\circ) + I_{13} \sin 13(\omega t - 240^\circ) + \dots \quad (A3)$$

where I_n is the amplitude of n th harmonic, $n = 1, 3, 5, 7, 11, 13, \dots$

Assuming that the magnitude of the secondary line-to-line voltage V_{ab} is the same as that of the primary line-to-line voltage, the turns ratio of the transformer is $N_1/N_2 = \sqrt{3}$. According to the connection diagram shown in Fig. 17, the line current i_A can be calculated by

$$i_A = i'_a - i'_c \quad (A4)$$

where i'_a and i'_c are the secondary currents i_a and i_c referred to the primary winding, respectively. The referred primary currents

4. Diode rectifier output side base values

$$P_b = \frac{S}{m}$$

$$V_b = \frac{3\sqrt{2}}{\pi} \times \frac{V}{m} = \frac{1.35 \times V}{m}$$

$$I_b = \frac{P_b}{V_b} = \frac{S}{1.35 \times V}$$

$$R_b = \frac{V_b}{I_b} = \frac{1.35^2 \times V^2}{m \times S}$$

$$L_b = \frac{V^2}{m \times S \times 2\pi f}$$

$$C_b = \frac{m \times S}{V^2 \times 2\pi f}$$

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