A Dual GTO Current-Source Converter Topology with Sinusoidal Inputs for High-Power Applications

Yuan Xiao, Bin Wu, *Member, IEEE*, Frank A. DeWinter, *Senior Member, IEEE*, and Reza Sotudeh, *Member, IEEE*

***Abstract*— A dual gate-turn-off thyristor current-source converter topology with sinusoidal inputs is proposed for high-power applications. The sinusoidal input current is realized by using pulsewidth modulation techniques to eliminate 11th and 13th harmonics and a transformer to cancel 5th, 7th, 17th, and 19th harmonics. Three switching patterns are proposed with a switching frequency of 360 or 420 Hz. The combination of these switching patterns provides a full-range control over the dc output current. Resonant modes of the proposed system are identified, and the criterion for the line capacitor design is provided. Simulation and experimental results are given to verify the theoretical analysis.**

***Index Terms*—AC motor drives, gate-turn-off (GTO) thyristor converters, high-power rectifiers, pulsewidth modulation techniques.**

I. Introduction

IN HIGH-POWER (up to 10 000 hp) ac motor drives using gate-turn-off (GTO) thyristor current-source inverter technology, SCR rectifiers are often used as front-end converters [1], [2]. The SCR rectifier has the features of simple structure, reliable operation, and bidirectional power flow. However, it injects harmonic currents into the power systems, and its power factor is poor under light-load conditions. A possible solution to these problems is to replace the SCR rectifier with a GTO pulsewidth modulation (PWM) current-source converter [3]. Fig. 1 shows a simplified circuit diagram of a GTO ac/dc current-source converter which can be used to replace an SCR rectifier in high-power induction motor drivers. Typically, the GTO devices are required to be connected in series in medium-voltage (4160–6900 V) applications.

For the design of a high-power GTO current-source converter, one of the most important issues is the switching frequency, which should be kept as low as possible to minimize GTO switching and snubber power loss. This requirement is also imposed by the switching characteristics of high-power GTO devices [4], [5].

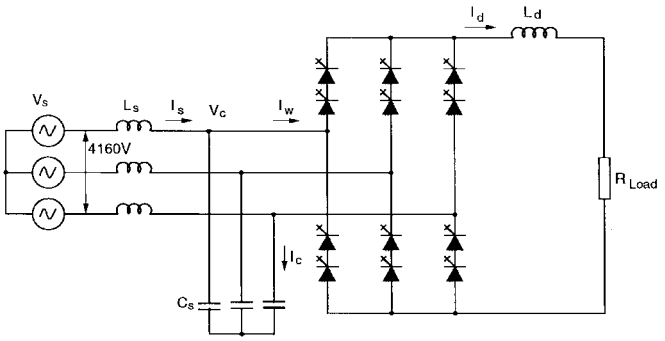

Fig. 1. Circuit diagram of a high-power GTO current-source converter.

In order to minimize the switching frequency, while keeping the input current close to sinusoidal, a novel GTO current-source converter topology, as shown in Fig. 2, is proposed. This topology is composed of two identical converters and an isolation transformer. The transformer is used to cancel certain harmonics produced by the converters. The other low-order harmonics that cannot be cancelled by the transformer are eliminated by PWM switching patterns. Compared with the single converter topology, the proposed dual converter has the following potential features.

- Sinusoidal input current—The transformer is used to cancel 5th, 7th, 17th, and 19th harmonic currents, while the PWM technique is employed to eliminate 11th and 13th harmonics. As a result, the input line current does not contain any harmonics of an order lower than 23rd. The other high-order harmonics can be easily filtered out by the line capacitor.
- Low switching frequency—As mentioned above, only 11th and 13th harmonics are required to be eliminated by the PWM pattern. Therefore, the lowest switching frequency for the proposed topology could be 360 Hz. For the single converter to eliminate all the harmonics with the order lower than 23rd, the minimum switching frequency is 840 Hz, which is too high to be implemented for high-power applications.
- Reliable operation for high-voltage applications—No GTO devices are connected in series in the proposed topology. The dynamic/steady-state voltage-sharing problem for the series devices in a single converter

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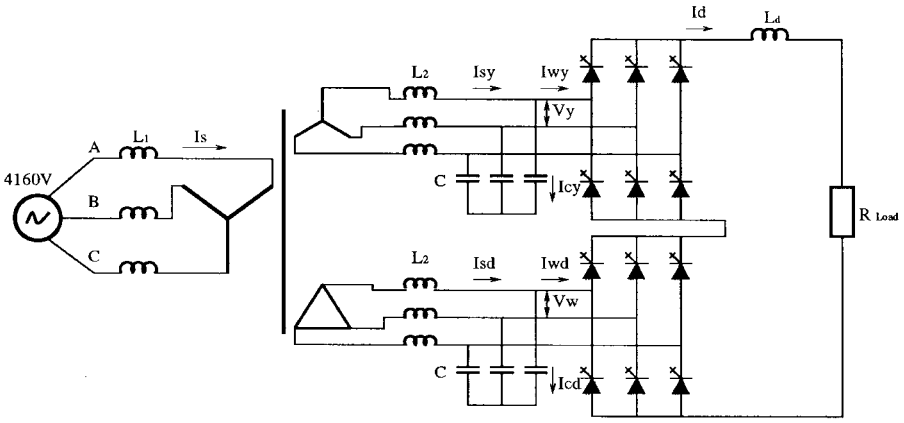


Fig. 2. A dual GTO PWM current-source converter configuration.

topology is completely avoided. The number of GTO devices for the dual converter topology remains the same as that for the single converter topology. For example, in a drive system with a supply voltage of 4160 V, twelve 6000-V GTO devices are required for both single and dual converter topologies. This concept can be easily used to develop a triple converter topology for higher voltage applications.

Compared with a single GTO converter topology, the proposed topology requires a transformer, which may not be considered as a disadvantage in terms of cost and converter size. For example, in retrofit or new applications where a standard (off-the-shelf) ac motor is used, an isolation transformer between the utility supply and front-end converter is indispensable to eliminate excessive line-to-ground and neutral-to-ground motor voltage generated by the current-source drives [6]. The transformer used in the dual converter topology serves the same purpose in addition to the harmonic cancellation. Therefore, the proposed topology is particularly suitable for this type of application. Compared to the single converter with an isolation transformer, the cost increase of the proposed dual converter system is minimal, mainly because the number of GTO devices, snubbers, and gating boards is essentially the same for both topologies.

II. Harmonic Cancellation

It is assumed that two sets of the transformer secondary windings are connected with a 30° phase shift. It can be proved that, regardless of the current waveforms in the secondary windings, the 5th, 7th, 17th, 19th, 27th, and 29th harmonic currents in these windings will be cancelled and do not appear in the primary windings.

III. Switching Patterns

The basic requirements for the design of switching patterns for the proposed topology are as follows:

- to eliminate 11th and 13th harmonics;
- to provide an adjustable dc current over a full range by adjusting modulation index;
- to minimize switching frequency.

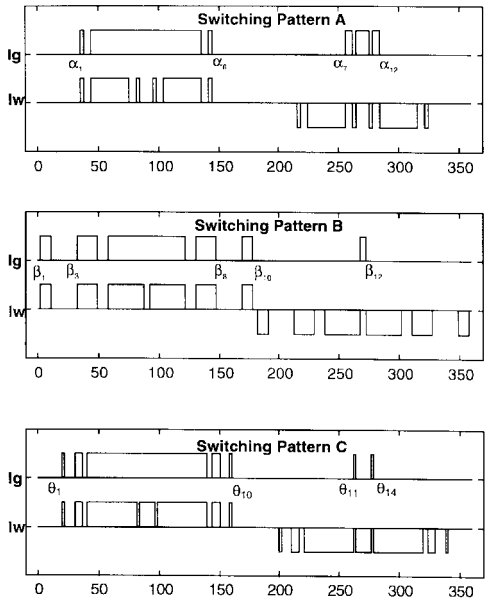


Fig. 3. Three proposed switching patterns. *Pattern A* $M_d = 0.02 \sim 0.857$, $f_{sw} = 360$ Hz. *Pattern B* $M_d = 0.84 \sim 1.086$, $f_{sw} = 360$ Hz. *Pattern C* $M_d = 0.84 \sim 1.086$, $f_{sw} = 420$ Hz.

Besides these requirements, the switching pattern design must satisfy a constraint, that is, only one switching device in the upper legs of the converter and one in the lower legs can be turned on at any time to guarantee a continuous dc output current and a defined converter input current.

Fig. 3 shows three switching patterns developed for the dual converter topology. *Patterns A* and *B* have a switching frequency of 360 Hz, which is the lowest possible frequency to satisfy the first two requirements, while *Pattern C* has a switching frequency of 420 Hz. The modulation index for the converter input current I_w is defined as

$$M_d = \frac{A_1}{I_{\rm dc}} \tag{1}$$

where A_1 is the amplitude of fundamental component in I_w and $I_{\rm dc}$ is the dc current of the converter.

Fig. 4 shows the converter input current waveform produced by *Pattern B* for switching angle calculation. To satisfy the constraint imposed by the current source converter, the switch-

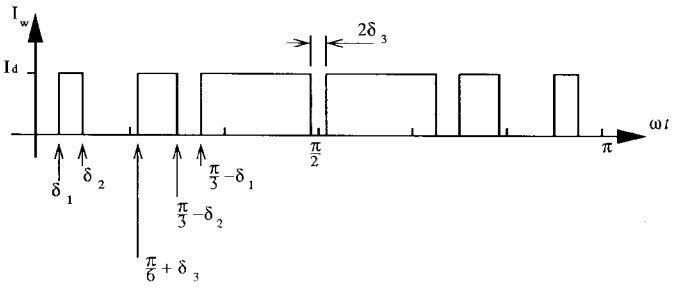


Fig. 4. Definition of independent variables.

ing angles are arranged such that there are only two switches conducting at any given time instant. As a result, only three switching angles, δ_1, δ_2, and δ_3, in Fig. 4 are independent. Once these angles are determined, all other angles in a half cycle can be readily calculated. The converter current I_w can be expressed by a Fourier series

$$I_w(\omega t) = \sum_{n=1}^{\infty} A_n \sin(n\omega t) \tag{2}$$

where A_n is the amplitude of the nth-order harmonic which can be calculated by

$$\begin{aligned} A_n = \frac{4I_{\rm dc}}{\pi}\Big\{ & \cos(n\delta_1) - \cos(n\delta_2) \\ & + \cos\Big[n\Big(\frac{\pi}{6}+\delta_3\Big)\Big] - \cos\Big[n\Big(\frac{\pi}{3}-\delta_2\Big)\Big] \\ & + \cos\Big[n\Big(\frac{\pi}{3}-\delta_1\Big)\Big] - \cos\Big[n\Big(\frac{\pi}{2}-\delta_3\Big)\Big]\Big\}. \end{aligned} \tag{3}$$

To eliminate 11th and 13th harmonics, two equations can be obtained by setting A_{11} and A_{13} to zero.

A third equation is required to obtain a desired modulation index. For a given M_d, the equation can be obtained by setting

$$A_1 - M_d I_{\rm dc} = 0. \tag{4}$$

Thus, three independent variables δ_1, δ_2, and δ_3 can be obtained by solving three nonlinear equations simultaneously.

Fig. 5 illustrates the calculated switching angles for *Patterns A* and *B*. It can be observed that, with the increase of modulation index M_d, the switching angle α_9 increases, while α_{10} decreases. When these two angles are merged at $M_d = 0.857$, the corresponding pulsewidth becomes zero, at which the simultaneous equations given by (3) and (4) have no solution and the 11th and 13th harmonics are no longer eliminated. Therefore, *Pattern A* can be used with the modulation index lower than 0.857.

When the modulation index M_d decreases from its maximum value of 1.085, the angle β_4 of *Pattern B* approaches β_3 and, at the same time, the angle between β_7 and β_8 decreases. These angles are merged at $M_d = 0.84$, which is the lowest modulation index for *Pattern B*. Fortunately, an overlap between *Patterns A* and *B* exists, which allows the converter to operate in a full modulation range. The converter can change its operating mode from *Pattern A* to *Pattern B* at the modulation index of 0.85, which is the mean value of the maximum modulation index of *Pattern A* and the minimum modulation index of *Pattern B*. *Pattern C* has the same range

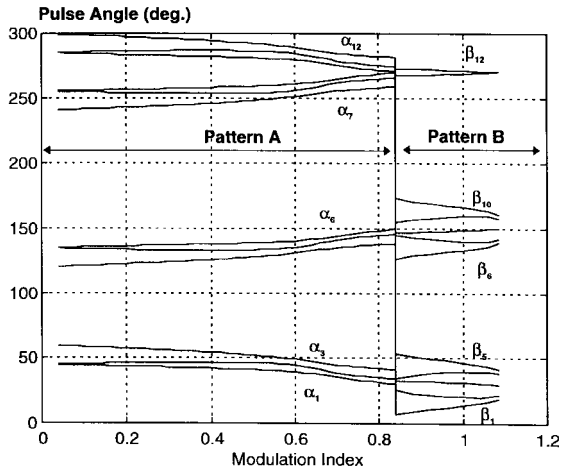


Fig. 5. Switching angle versus modulation index.

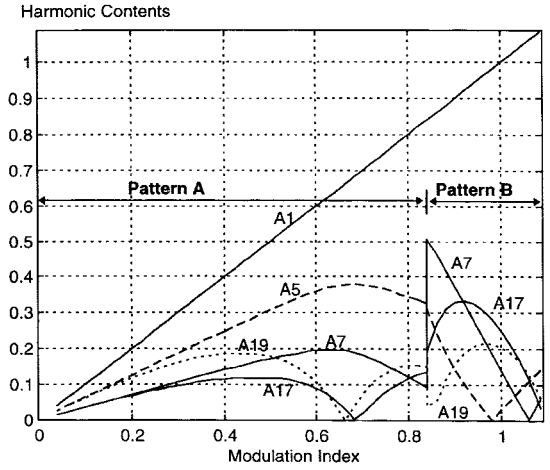


Fig. 6. Harmonic contents of combined PWM *Patterns A* and *B*.

of modulation index as *Pattern B* and, therefore, will not be discussed here.

Fig. 6 shows the harmonic contents in the converter input current generated by these two patterns. Although these switching patterns can satisfy all the requirements, the 7th and 17th harmonic currents produced by *Pattern B* are relatively high, which may increase energy loss in the transformer secondary winding. Fig. 7 illustrates the harmonic content associated with *Patterns A* and *C*. Obviously, a better harmonic profile is achieved for *Pattern C*, at the expense of increased switching frequency. Furthermore, the magnitude of harmonic currents changes with the modulation index smoothly, especially during the transit between the two patterns. Therefore, for high-power converters where a switching frequency of 420 Hz can be implemented, the combination of *Patterns A* and *C* is recommended.

IV. Resonant Modes and Capacitor Design

The filter capacitor and transformer inductances constitute the system resonant modes. Fig. 8 shows the equivalent circuit for resonant mode analysis. The system admittance seen by

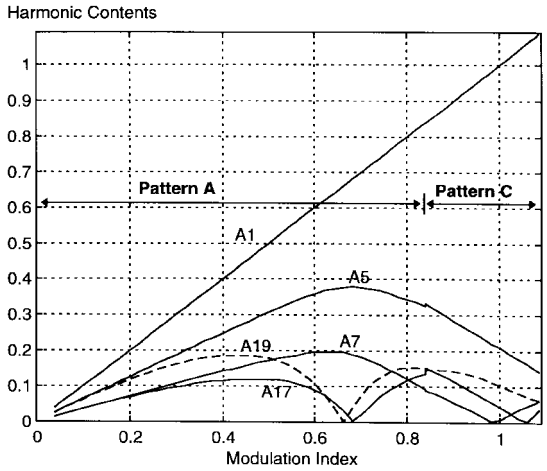


Fig. 7. Harmonic contents of combined PWM *Patterns A* and *C*.

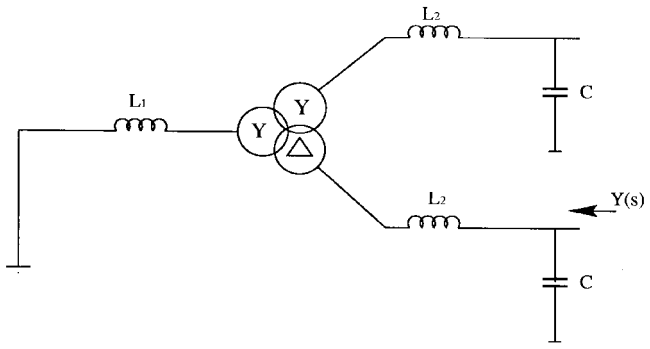


Fig. 8. Equivalent circuit for resonant mode analysis.

the converter can be expressed as

$$Y(s) = \frac{1}{SL_2 + \dfrac{1}{\dfrac{1}{SL_1} + \dfrac{SC}{S^2L_2C+1}}}. \tag{5}$$

The zeros of the admittance $Y(s)$ represent the parallel resonant modes. The frequencies of these resonant modes can be calculated by

$$\omega_1 = \frac{1}{\sqrt{L_2C}} \tag{6}$$

and

$$\omega_2 = \frac{1}{\sqrt{(2L_1 + L_2)C}}. \tag{7}$$

The first resonant mode is associated with the transformer secondary leakage inductance only. This resonance may be excited by the harmonics in the converter input current I_w. Since the 11th and 13th harmonic currents in I_w are eliminated, the frequency of this resonant mode may be set to

$$\omega_1 = 11\text{–}13 \text{ p.u.}$$

Assuming the secondary leakage inductance L_2 is 0.05 per unit, the capacitor size can be determined by

$$C = \frac{1}{\omega_1^2 L_2} = 0.12\text{–}0.17 \text{ p.u.} \tag{8}$$

This equation also indicates that the capacitor size could be reduced by increasing the transformer secondary leakage inductance, which can be achieved by transformer design.

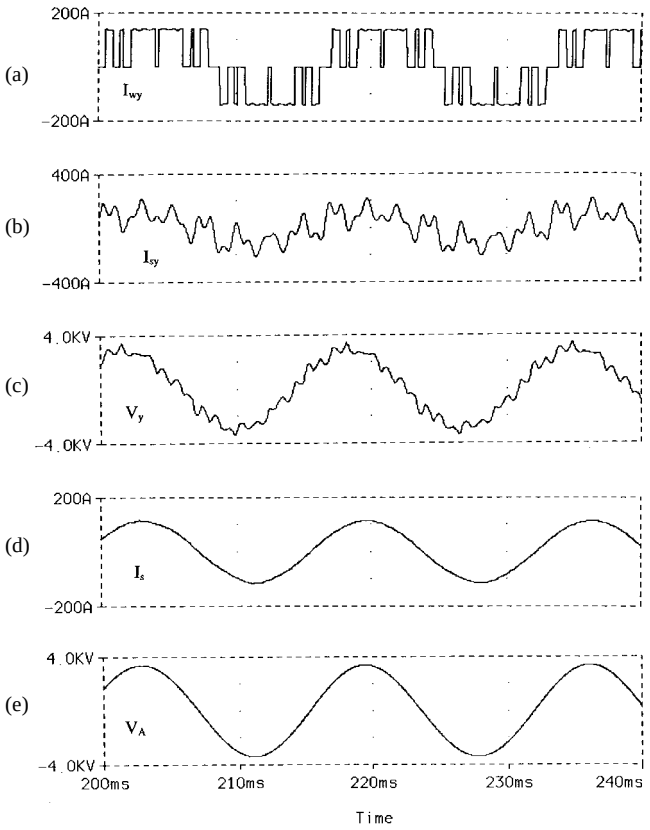


Fig. 9. Simulation results from a 4160-V 1-MVA converter system. *Pattern B* at $M_d = 0.9$ (the worst operating condition).

The transformer winding can be arranged in such a way that some of the primary leakage inductance can be moved to the secondary side without increasing the cost of the transformer.

The second resonant mode is dominated by the total inductance L_1 on the transformer primary side including the inductance of the utility supply. Assuming $L_1 = 0.15$ per unit, the resonant frequency is

$$\omega_2 = \frac{1}{\sqrt{(2L_1 + L_2)C}} = 4.1\text{–}4.9 \text{ pu.} \tag{9}$$

Since the current in the primary winding does not contain any low-order harmonics, this resonance will not be excited.

The resonant frequencies given in (6) and (7) are derived under the assumption that the equivalent Y- and Δ-connected secondary leakage inductances (refer to Fig. 8) have the same value. These inductances can be made equal during the transformer design process. However, in manufacturing, a few percentages of discrepancy may occur. In what follows, the effect of such a discrepancy on the resonant frequency is discussed. Assume that the Y- and Δ-connected secondary leakage inductances can be expressed as

$$L_Y = L_2 \tag{10}$$

and

$$L_\Delta = (1+K)L_2 \tag{11}$$

where K represents the discrepancy in percent.

Following the same procedure discussed at the beginning of this section, the frequencies of the resonant modes can be

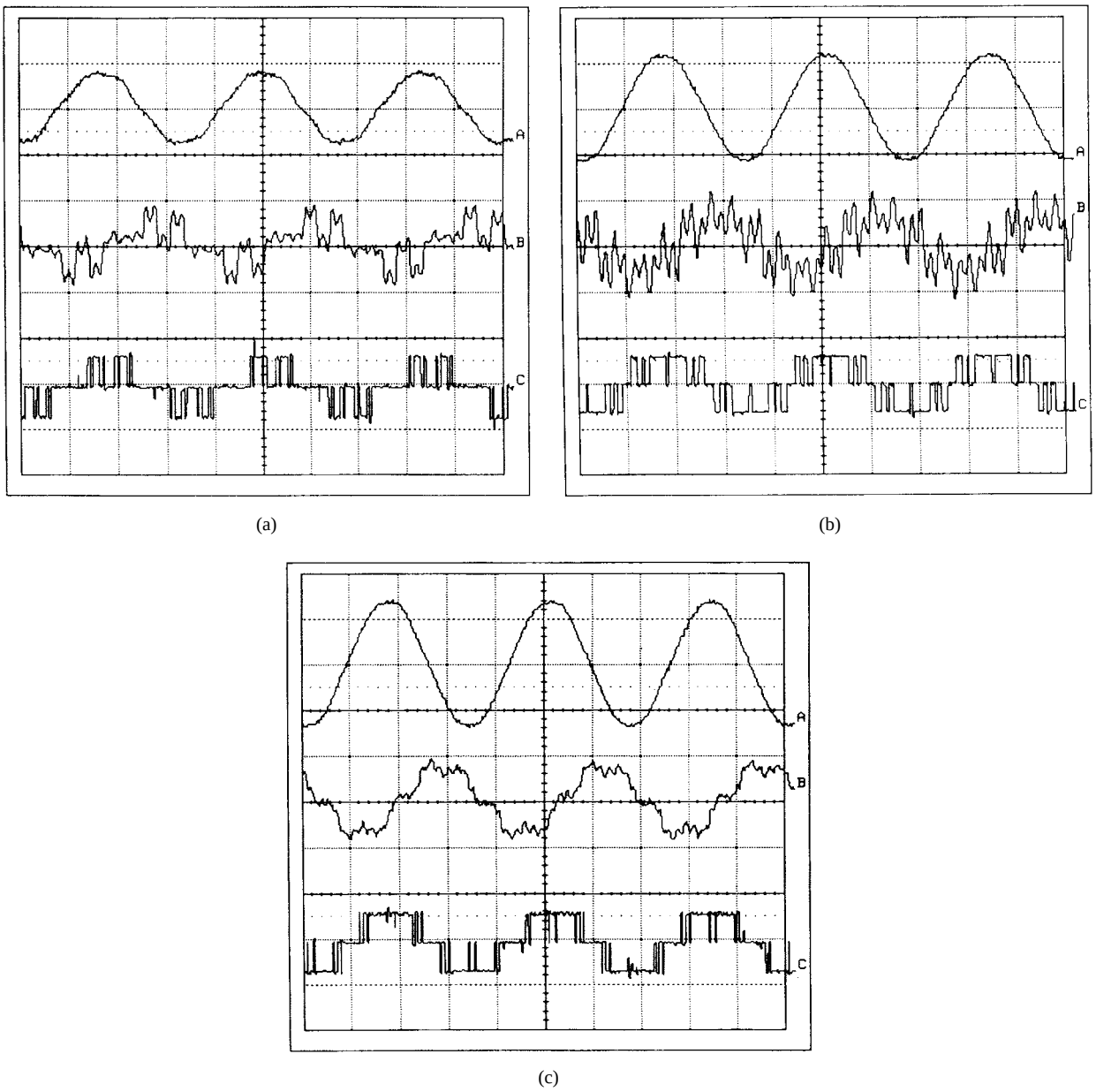


Fig. 10. Experimental results from a 208-V 20-kVA dual converter system. (a) *Pattern A* at $M_d = 0.5$. (b) *Pattern B* at $M_d = 0.9$ and (c) *Pattern C* at $M_d = 1.02$. Trace *A*: line current I_s, 50 A/div, 5 ms/div. Trace *B*: transformer secondary current I_{sd}, 50 A/div, 5 ms/div. Trace *C*: converter input current I_{wd}, 50 A/div, 5 ms/div.

calculated by

$$\omega_1 = \frac{1}{\sqrt{CL_2}} \cdot \frac{1}{\sqrt{1+\dfrac{L_1K}{2L_1+L_2(1+K)}}} \approx \frac{1}{\sqrt{CL_2}} \cdot \frac{1}{\sqrt{1+K/2}} \tag{12}$$

and

$$\omega_2 = \frac{1}{\sqrt{2C\left(L_1+L_2\dfrac{1+K}{2+K}\right)}} \approx \frac{1}{\sqrt{C(2L_1+L_2)}} \cdot \sqrt{\frac{1+K/2}{1+K}}. \tag{13}$$

If the secondary leakage inductances have a 5% discrepancy, ω_1 and ω_2 will approximately change 1.2%. Obviously, this change has little effect on the converter operation.

V. Input Power Factor Control

It is well known that a capacitor bank is required in current-source converters to assist the commutation of switching devices. The use of the capacitor will make the input power factor leading. In the proposed converter system, a relatively small size capacitor can be used, even though the switching frequency is only 360 or 420 Hz. This feature will facilitate the implementation of unity power factor operation. With a typical capacitor value of 0.15 per unit for each converter, the converter system will have a leading input power factor of 0.96 under rated load conditions. To achieve unity power

TABLE I
TOTAL HARMONIC DISTORTION FROM EXPERIMENTAL RESULTS

Switching Pattern	Switching Frequency (Hz)	Modulation Index	THD: I_s
A	360	0.5	5.4%
B	360	0.9	1.8%
C	420	1.02	1.4%

factor, a phase-shift control can be integrated with modulation index control [7]. A small phase shift between the converter input voltage and modulated current will easily make the input power factor unity. A comprehensive analysis of the input power factor control for high-power GTO current-source converters is presented in [8].

VI. SIMULATION AND EXPEIRMENTAL RESULTS

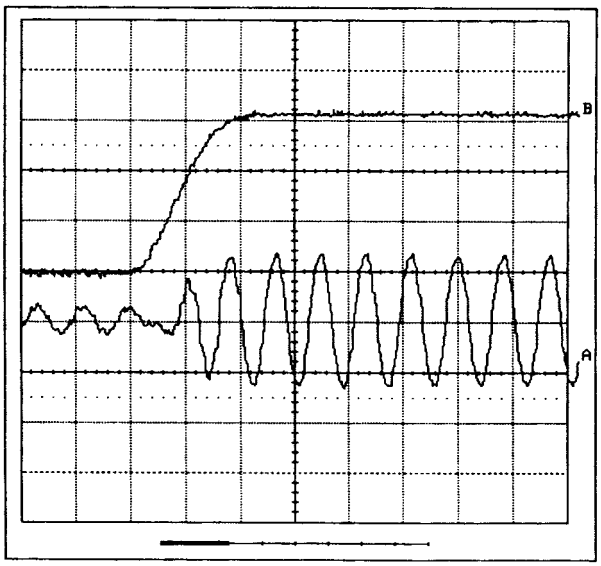
Fig. 9 shows a set of the simulation results. The converter system is rated at 4160 V (line-to-line), 60 Hz, and 1000 kVA. The parameters used in the simulation are $L_1 = 0.15, L_2 = 0.05$, and $C = 0.13$, all in per unit. *Switching Pattern B* is selected with the modulation index set at 0.9, at which both 7th and 17th harmonics have a large magnitude (the worst operating condition). The waveforms of converter input current L_{wy}, transformer secondary current I_{sy}, and secondary line-to-line voltage V_y are shown in Fig. 9(a)–(c), respectively. Although the secondary current I_{sy} contains harmonics, these harmonics can be cancelled by the Δ–Y-connected transformer. Therefore, the line current I_s on the primary side is sinusoidal. The unity power factor is obtained by introducing a small delay angle between the converter input current and voltage.

The experimental results are obtained from a laboratory GTO dual current-source converter system. The control of the laboratory unit, including PWM gate pulse generators, proportional integral (PI) controllers, and a unity power factor controller, is implemented by a TMS320C31–based digital signal processor (DSP) board. All three switching patterns proposed in this paper are included in the PWM generator. The converter system is rated at 208 V, 20 kVA, and 60 Hz with $L_1 = 0.026, L_2 = 0.051$, and $C = 0.15$ per unit. The waveforms of converter input current I_{wy}, transformer secondary current I_{sy}, and line input current I_s when the system is operated at $M_d = 0.5$, 0.9, and 1.02 with *Switching Patterns A, B,* and *C* are shown in Fig. 10. As shown in Table I, the measured total harmonic distortion (THD) of the input line current is 5.4, 1.8, and 1.4%, respectively.

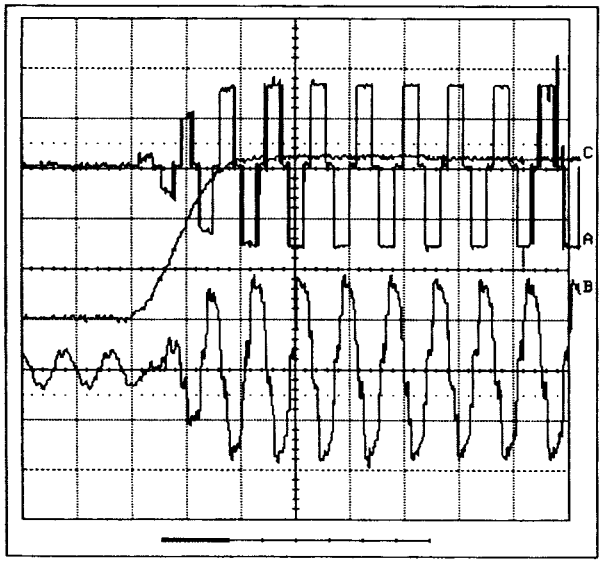
To investigate possible resonances which may be caused by the resonant modes during transient, a step command is applied to the converter system. Fig. 11 shows one set of such experiments. The dc current I_d is increased from zero to 32 A in 40 ms. The transformer primary line current I_s, secondary line current I_{sd}, and converter input current I_{wd} do not exhibit any resonant phenomenon during transient. Many experiments were performed under various loading conditions with a step increase or step decrease command. No resonant phenomena were ever observed during the experiments.

VII. CONCLUSIONS

A dual GTO current-source converter topology with sinusoidal inputs has been proposed for high-power applications. The sinusoidal input current is realized by using PWM techniques to eliminate 11th and 13th harmonics and a transformer which is connected to two identical current-source converters. Three switching patterns are developed with switching frequencies of 360 and 420 Hz. The combination of these switching patterns provides a full-range control over the dc output current. Resonant modes of the proposed system are identified, and the criterion for the line capacitor design is provided. A unity power factor control scheme for the proposed topology is briefly discussed. A 20-kVA dual current-source converter system has been constructed to verify the theoretical analysis. The proposed topology is particular suitable for high-power applications, due to its low switching frequency, sinusoidal inputs, and unity power factor operation.



(a)



(b)

Fig. 11. Step response of laboratory dual converter system for the investigation of resonant modes, *Pattern B* at $M_d = 1.075$. Trace *A*: converter input current I_{wd}, 50 A/div, 20 ms/div. Trace *B*: transformer secondary current I_{sd}, 50 A/div, 20 ms/div. Trace *C*: dc current $I_{\rm dc}$, 10 A/div, 20 ms/div.

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