High Power GTO AC/DC Current Source Converter with Minimum Switching Frequency and Maximum Power Factor

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Abstract - This paper presents a unique PWM switching pattern and a novel power factor control scheme for high power GTO ac/dc converters. This switching pattern has a switching frequency of 360Hz, which is the lowest possible frequency to achieve 5th and 7th harmonic elimination and an adjustable dc output current simultaneously. Using both feedback and feedforward control techniques, the proposed power factor control scheme can keep the converter input power factor at unity or a maximum achievable value. Simulation and experimental results are given to confirm the proposed PWM pattern and power factor control scheme.

I. Introduction

Figure 1 shows a simplified circuit diagram of a GTO ac/dc current source converter (CSC) which can be used to replace SCR rectifier in high power (up to 10,000hp) induction motor drives. In order to reduce GTO and snubber loss, which accounts for approximately 80% of total loss in a drive system without power transformers, the switching frequency of the converter must be minimized[1-2]. In the literature, the lowest switching frequency for 5th and 7th harmonic elimination used in current source converters is 420Hz[3].

A novel PWM switching pattern with a single-bypass pulse for high power current source converter is proposed. Using this switching pattern together with a power factor control scheme discussed in this paper, the current source converter has the following features:

- The switching frequency is only 360Hz, which is the lowest possible switching frequency to eliminate 5th and 7th harmonics and at the same time to provide an adjustable dc output current;
- Input power factor of the converter can be kept at unity or a maximum possible value; and
- The line current is nearly sinusoidal.

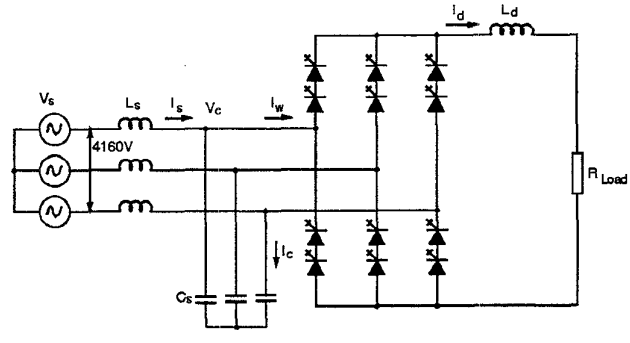

Fig. 1 A typical circuit diagram of PWM ac/dc current source converter

II Switching Pattern

Two proposed PWM gating patterns are illustrated in Figure 2, where g_1 to g_6 are gating signals and I_w is converter input current. Both switching patterns use only five pules to eliminate 5th and 7th harmonics and one bypass pulse, defined by θ_{11} and θ_{12}, to obtain an adjustable dc current. Therefore, the switching frequency of the converter is only 360Hz, which is the lowest possible one to achieve the above purpose.

It can be seen from the current waveform I_w that pattern A can be applied when modulation index M_d is high, which is defined as

$$M_d = \frac{A_1}{I_{dc}} \qquad (1)$$

where A_1 is the amplitude of fundamental component in I_w and I_{dc} is the dc current of the converter. When the modulation index is low, Pattern B is suitable, since the converter bypasses the dc current three times per cycle to reduce the fundamental component A_1. Of these three

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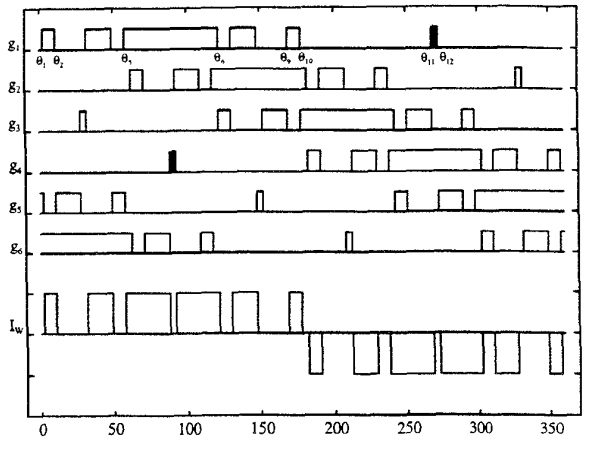
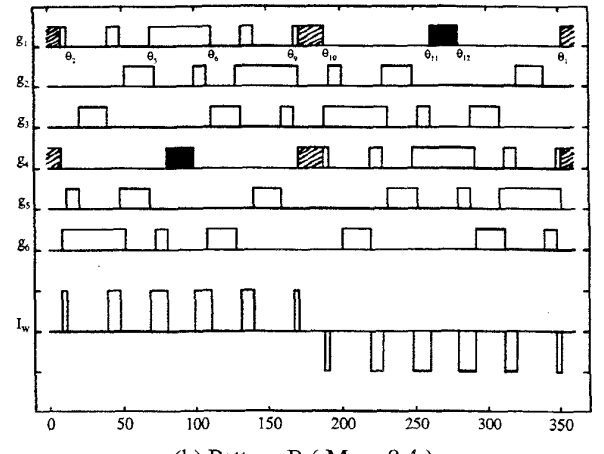
bypasses, only one is produced by the bypass pulse, and the other two are achieved by overlapping gating signals (see shaded pulses in Fig. 2.b). This is a unique arrangement which minimizes the number of bypass pulses. As a results, a minimum switching frequency of 360Hz is obtained. For other switching patterns proposed in [3], two bypass pulses were used to achieve the same objective.



(a) Pattern A ($M_d = 0.9$)



(b) Pattern B ($M_d = 0.4$)

Fig. 2 PWM gating patterns and converter input current I_W

To satisfy the criterion imposed by current source converter that only two switches conduct at any time, the 12 switching angles from θ_1 to θ_{12} are decided by only three independent variables α_1, α_2 and α_3, as shown in Fig. 3. The converter input current I_W can be expressed by a Fourier series:

$$i_w(\omega t) = \sum_{n=1}^{\infty} A_n \sin(n\omega t) \qquad (2)$$

where A_n is the n_{th}-order harmonic which can be calculated by

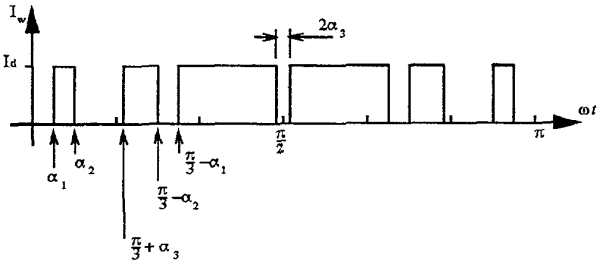


Fig.3 Definition of independent variables α_1, α_2 and α_3

$$A_n = \frac{4I_{dc}}{\pi}\{\cos(n\alpha_1)-\cos(n\alpha_2) + \cos[n(\frac{\pi}{6}+\alpha_3)]-\cos[n(\frac{\pi}{3}-\alpha_2)] + \cos[n(\frac{\pi}{3}\pm\alpha_1)]-\cos[n(\frac{\pi}{2}-\alpha_3)]\} \qquad (3)$$

To eliminate 5th and 7th harmonics, two equations can be obtained by setting A_5 and A_7 to be zero.

A third equation is required to obtain a desired modulation index. For a given M_d, an equation can be obtained by setting

$$A_1 - M_d I_{dc} = 0 \qquad (4)$$

Thus, three independent variables α_1, α_2 and α_3 are obtained by solving three nonlinear equations simultaneously.

Figure 4 shows the switching angles versus modulation index M_d. It should be noted that the transition from pattern A to B is smooth. Also, the switching angle θ_1 becomes negative and θ_{10} is larger than 180° when the modulation index M_d is lower than 0.826 at which the transition between Patterns A and B takes place. The harmonic contents in the converter input current I_W are evaluated and shown in Fig 5, where it is indicated that the 5th and 7th harmonic components are eliminated.

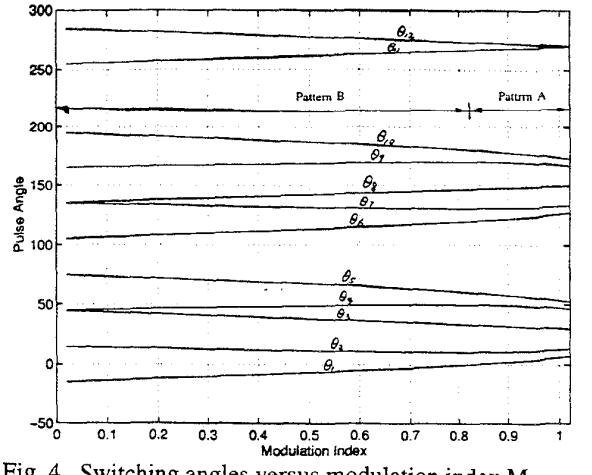


Fig. 4 Switching angles versus modulation index M_d

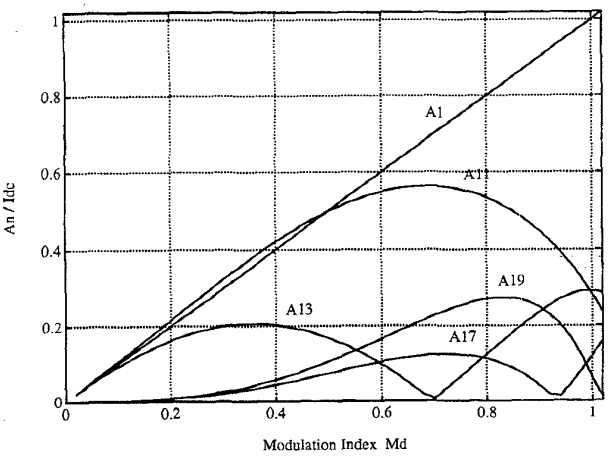


Fig. 5 Harmonic contents in converter input current I_W

III Power Factor Control

Figure 6 shows a phasor diagram of a current source converter. The input power factor can be controlled by introducing a delay angle between the converter input current I_W and voltage V_C [4]. When a unity power factor is achievable, the delay angle for obtaining a unity power factor can be calculated by

$$\alpha = \sin^{-1}\frac{\omega_s C_s V_s}{M_d I_d} \qquad (5)$$

However, a unity power factor is not always achievable for the high power CSC because of the line filter capacitor C_S which is in a range of 0.4 to 0.7 per unit for a converter with a switching frequency of 360Hz. For example, under light load conditions, the converter input current I_W is low, and its lagging component produced by delay angle α cannot compensate the leading capacitor current I_C(typically, I_C=0.4~0.7 per unit). Under this operating condition, Eq. (5) is not valid. Unity power factor cannot be achieved either when a high dc voltage is required. Since the dc voltage is given by

$$V_{dc} = \sqrt{1.5}\, M_d\, V_{L\text{-}L} \cos\alpha \qquad (6)$$

both modulation index M_d and cosα should be close to their maximum value to provide required dc voltage. There is no room available for α to be adjusted for unity power factor control.

To overcome the problems mentioned above, a novel power factor control scheme for the high power GTO ac/dc current source converter is proposed and illustrated in Fig. 7. Using both feedforward and feedback control techniques, the proposed scheme guarantees that the input power factor of the converter can be kept at its maximum possible value. When the converter operates under certain operating conditions where a unity power factor is achievable, this control scheme will automatically adjust delay angle α and modulation index M_d such that Eq. (5) will be satisfied. On the other hand, if a unity power factor is not achievable, the modulation index M_d will be saturated and delay angle α will be adjusted by the PI controller to produce a highest achievable power factor.

Another feature of this scheme is parameter insensitive, that is, variations in the line and load impedance or changes in the filter capacitor size will not affect the process of tracking the maximum input power factor. No parameters in the control scheme should be adjusted to accommodate such variations or changes.

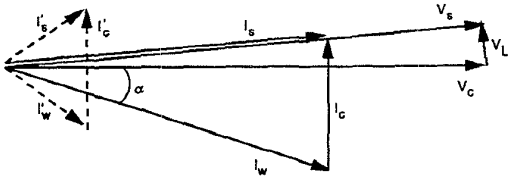


Fig. 6 Phasor diagram of a converter system

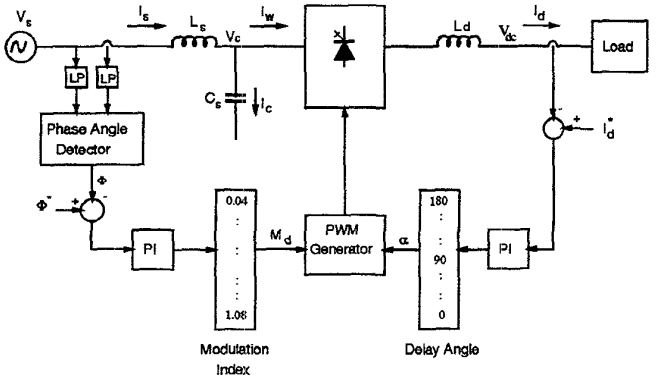


Fig. 7 Proposed power factor control scheme

IV Simulation and Experimental Results

One of the experimental results obtained from a laboratory GTO current source converter is shown in Fig. 8.The converter is rated at 208V, 10kVA and 60Hz with L_s = 0.1 and C_s = 0.66 per unit. It can be seen that the line current I_S is nearly sinusoidal due to the use of PWM technique and filter capacitor C_S. Figure 9 shows a set of simulated transient and steady-state waveforms of the converter system under different operating conditions. The converter is rated at 4160V; 60Hz, and 1MVA with L_s = 0.1 and C_s = 0.66 per unit. At t = 1.0 second, the converter reaches a steady state operating point where $I_d = I_d^* = 1.0$, V_d = 0.5, and R_L = 0.5, all in per unit. As shown in Fig. 9(d) and (e), the input power factor is unity with M_d = 0.819 and α = 55.17°. At t > 1.0 second, the current reference I_d^* is reduced to 0.4 per unit and at the same time the load resistance R_L is

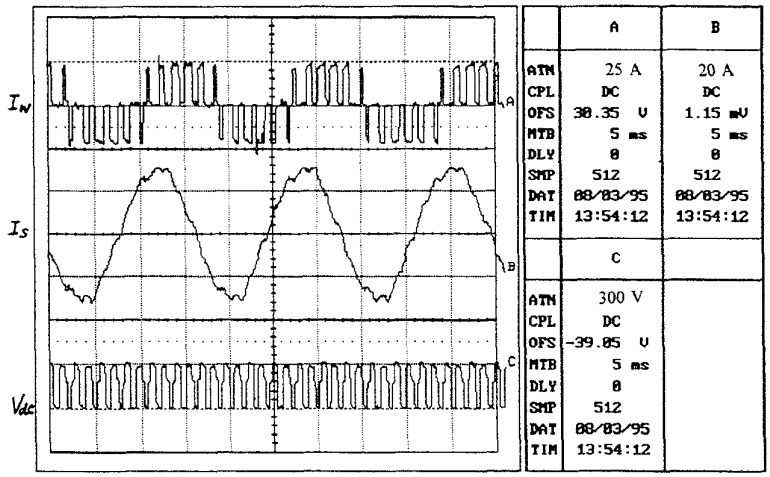


Fig. 8 Experimental results

increased to 1.25 per unit to keep the dc voltage at 0.5 per unit. At t = 2.0 second when the system reaches a new steady state, the modulation index M_d is saturated and the delay angle α is 62.99° at which a maximum possible power factor is obtained. In this case, the phase angle Φ between V_s and I_s is 60.48° as indicated in Fig. 9(f) and (g), and the power factor reaches a value of 0.49.

V Conclusions

A unique PWM switching pattern and a novel power factor control scheme for high power GTO ac/dc converters are proposed in this paper. This switching pattern has a switching frequency of 360Hz, which is the lowest possible frequency to achieve 5th and 7th harmonic elimination and an adjustable dc output current simultaneously. The proposed power factor control scheme using both feedback and feedforward control techniques can keep the converter input power factor at unity or a maximum achievable value. The proposed PWM pattern and power factor control scheme are verified by simulation and experiment.

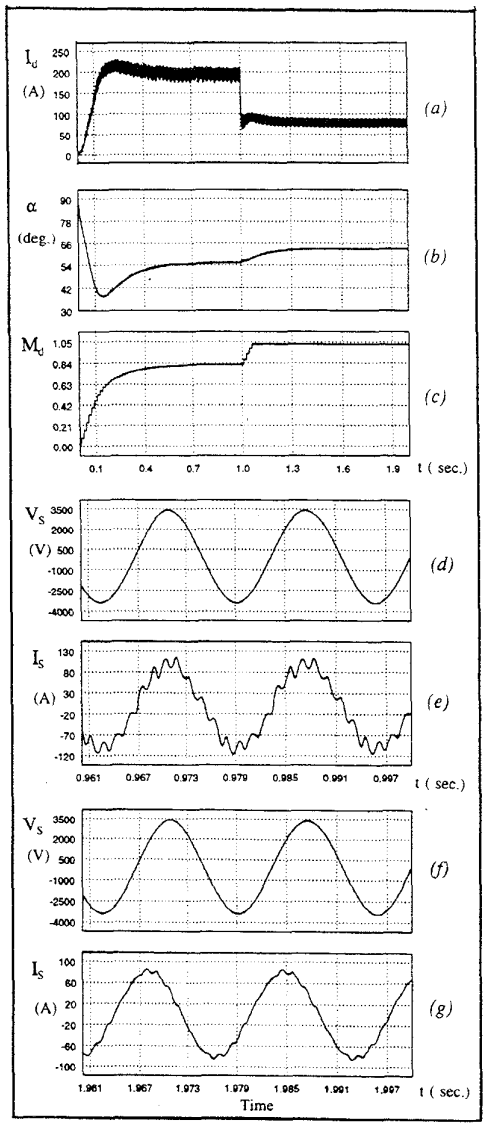


Fig. 9 Simulation results

Reference

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