IEEE Transactions on Circuits and Systems-II

Guest Editorial of Special Issue on Software Defined Radio Transceivers and Circuits for 5G Wireless Communications

Wireless communications is one of the fastest growing technologies, which has a huge impact on our daily life, society and economy. A plethora of wireless communication standards have been developed to date and more new standards are also emerging. For universal global communications anytime and anywhere, one smart mobile phone should ideally support 2G/2.5G (GSM, GPRS, EDGE), 3G (UMTS, WCDMA, CDMA2000, TD-SCDMA), and 4G (LTE, LTE-A). As research has already started to define 5G communications, more standards will be developed, for example to include new wireless and mobile technologies such as massive MIMO, millimetre waves, cognitive radio, etc. 5G mobile systems have already been placed on the development agenda in many countries worldwide. Compared with existing generations, 5G will provide much higher data rate, operational flexibility and environmental adaptability.

Integration and interoperation of such different systems and standards requires full reconfigurability in 5G transceiver architecture and constituent circuits to accommodate different operation frequency, signal bandwidth and power requirement, which can only be fulfilled by advanced software defined radio techniques. The most challenging part of the dynamically reconfigurable transceiver is the RF, analog and mixed-signal circuits and systems, as the digital baseband can easily be programmable by FPGA and DSP technologies. A software-defined transceiver on a single chip would also be desired for reducing phone size and cost.

The aim of this special issue is to publish, in a single source, technical papers reflecting the most recent research and application results in software defined radio architectures, circuits and systems for wireless and mobile communications, and identify new challenges in software defined radio research for 5G communications.

The response to our call for papers is remarkable, with some 110 submissions having been received. After rigorous review, 23 papers have been selected for publication in the special issue. These papers cover a very wide range of software defined radio systems and techniques, which are summarised succinctly as below.

- The papers *All-digital Transmitter with Mixed-domain Combination Filter, A Configurable Transmitter Architecture for IEEE 802.11ac and 802.11ad Standards, 2-D Cartesian Memory Polynomial Model for Nonlinearity and I/Q imperfections Compensation in Concurrent Dual-Band Transmitters, Low-complexity pipelined architecture for FBMC/OQAM transmitter, Wideband TV White Space Transceiver Design and Implementation, Digitally Enhanced Wideband I/Q Downconversion Receiver with 2-channel Time-Interleaved ADCs,* and *Finding the Initial Estimate for the Diode Bias Point in Multi-Port Receivers* are concerned with various advanced wireless transmitters and receivers with novel digital or digitally-assisted architectures and techniques.
- *Cooperative Wideband Spectrum Sensing Based on Sub-Nyquist Sparse Fast Fourier Transform* presents work in the hot area of cognitive radio.
- The contributions *A PAPR-Aware Dual-Mode Sub-GHz CMOS Power Amplifier for Short Range Wireless Communication, Analysis and Design of Ultra-broadband Stacked Power Amplifier in CMOS Technology,* and *A Methodology for Implementation of High Efficiency Broadband Power Amplifiers with Second Harmonic Manipulation* focus on challenging multi-mode and broadband power amplifiers.
- A significant number of papers describe different types of filters for software defined transceivers, which include digital filters, analog filters, RF and microwave filters. Their titles are *Design and Realization of Variable Digital Filters for Software Defined Radio Channelizers using Improved Coefficient Decimation Method, Efficient Halfband FIR Filter Structures for RF and IF Data Converters, A Digitally Assisted Non-Linearity Mitigation System for Tunable Channel Select Filters, Frequency-Domain Analysis of N-path Filters Using Conversion Matrices, High-Q Bandstop Filters Exploiting Acoustic-Wave-Lumped-Element Resonators (AWLRs), A Reconfigurable Microwave Combline Filter, A Tunable Metamaterial Resonator using Varactor Diodes to Facilitate the Design of Reconfigurable Microwave Circuits,* and *Passive and Active Electrical Balance Duplexers.*

- The papers *All-Digital Calibration of Timing Skews for TIADCs Using the Polyphase Decomposition* and *A 65nm CMOS DAC Based on a Differentiating Arbitrary Waveform Generator Architecture for 5G Handset Transmitter* highlight some interesting design and calibration techniques for data converters (ADC and DAC).
- Finally, the contributions *A 0.05-to-10GHz, 19-to-22GHz, and 38-to-44GHz Frequency Synthesizer for Software-Defined Radios in 0.13-μm CMOS Process* and *Open Loop Fractional Division using Voltage Comparator based Digital-to-Time Converter* present new research on frequency synthesisers.

We are very grateful to all authors of the papers for their high quality contribution to the special issue. We would also like to thank all reviewers of the papers for their generous and valuable help. Assistance from the TCAS-II Editorial Staff is much appreciated. Finally, great support from the TCAS-II Editors, Prof. J. Silva-Martinez and Prof. A. Demosthenous is highly acknowledged.

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Yichuang Sun (M'90-SM'99) received the B.Sc. and M.Sc. degrees from Dalian Maritime University, Dalian, China, in 1982 and 1985, respectively, and the Ph.D. degree from the University of York, York, U.K., in 1996, all in communications and electronics engineering. He is currently a Professor in the School of Engineering and Technology of the University of Hertfordshire, UK.

His research interests are in the areas of RF, analog and mixed-signal circuits, software defined radio transceivers, and wireless and mobile communication systems. He has published over 280 papers and 4 books: Continuous-time Active Filter Design, CRC Press, USA, Design of High frequency Integrated Analogue Filters, IEE/IET Press, UK, Wireless Communication Circuits and Systems, IET Press, and Test and Diagnosis of Analogue, Mixed-signal and RF Integrated Circuits - the Systems on Chip Approach, IET Press.

He was a Series Editor of IEE Circuits, Devices and Systems Book Series from 2003 to 2008. He was Associate Editor of IEEE Transactions on Circuits and Systems-I in 2010-2011 and will serve the journal as Associate Editor again in 2016-2017. He has been Editor of ETRI Journal since 2006. He was Lead Guest Editor of seven IEEE and IET journal special issues. He has also been widely involved in various IEEE technical committee and international conference activities.

Baoyong Chi received the B.S. degree in microelectronics from Peking University, Beijing, China, in 1998 and the Ph.D. degrees in 2003 from Tsinghua University, Beijing. During 2006 to 2007, he was a Visiting Assistant Professor at Stanford University, Stanford, CA, USA. He is currently a Professor in Institute of Microelectronics, Tsinghua University. He has been a TPC member of A-SSCC since 2005 and VLSI-DAT since 2009. He served as Guest Editor for a special issue of the IEEE Transactions on Circuits and Systems-II and as MOOP Member of the Science China Information Science. In his 12 years of academic experience, he has published over 140 academic papers and 2 books, and has been issued more than 15 patents. His research interests include RF/MM-wave integrated circuit design, analog integrated circuit design and monolithic wireless transceiver analog front-end.

Heng Zhang received the B.S. degree in electrical engineering from Peking University, Beijing, China, in 2004, and the Ph.D. degree in electrical engineering from Texas A&M University, College Station, USA, in 2010. In the summer and fall of 2006, she was an Analog IC Design Engineer with Texas Instrument, Dallas, TX, where she designed a low power ADC for hard disk applications. In summer 2007, she was with the RF and Analog Technologies Department, UMC, Sunnyvale, CA, where she researched digital calibration techniques for ADCs. Since August 2010, she has been a Senior Staff Scientist with Broadcom Corporation, Irvine, CA, working on high-speed transceivers for Enterprise, Storage, Wireless and Telecom Networking applications.

Dr. Zhang's research interests include high-speed serial links, data converters, and RF circuits. She has published peer-reviewed journal/conference papers with 420+ citations. Her papers have been listed as Top 100 most accessed papers in IEEE publications overall; Top 10 most accessed papers in IEEE Journal of Solid-State Circuits; Top 10 most accessed papers in IEEE Transactions on Circuits and Systems I; and Top 10 most accessed papers in IEE Electronic Letters, for multiple months. She served as Guest Editor and Associate Editor for IEEE Transactions on Circuits and System-II in 2014-2015. Dr. Zhang was the recipient of 2010 Chinese Government National Award for Outstanding Self-financed Students Abroad.

Appendix

Order of Papers to Appear in the Special Issue

Transmitters and Receivers

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2. **14168** A Configurable Transmitter Architecture for IEEE 802.11ac and 802.11ad Standards
3. **14396** 2-D Cartesian Memory Polynomial Model for Nonlinearity and I/Q imperfections Compensation in Concurrent Dual-Band Transmitters
4. **14241** Low-complexity pipelined architecture for FBMC/OQAM transmitter
5. **14076** Wideband TV White Space Transceiver Design and Implementation
6. **14217** Digitally Enhanced Wideband I/Q Downconversion Receiver with 2-channel Time-Interleaved ADCs
7. **14442** Finding the Initial Estimate for the Diode Bias Point in Multi-Port Receivers

Cognitive Radio

8. **14532** Cooperative Wideband Spectrum Sensing Based on Sub-Nyquist Sparse Fast Fourier Transform

Power Amplifiers

9. **14415** A PAPR-Aware Dual-Mode Sub-GHz CMOS Power Amplifier for Short Range Wireless Communication
10. **14430** Analysis and Design of Ultra-broadband Stacked Power Amplifier in CMOS Technology
11. **14190** A Methodology for Implementation of High Efficiency Broadband Power Amplifiers with Second Harmonic Manipulation

Filters

12. **14260** Design and Realization of Variable Digital Filters for Software Defined Radio Channelizers using Improved Coefficient Decimation Method
13. **14066** Efficient Halfband FIR Filter Structures for RF and IF Data Converters
14. **14553** A Digitally Assisted Non-Linearity Mitigation System for Tunable Channel Select Filters
15. **14150** Frequency-Domain Analysis of N-path Filters Using Conversion Matrices
16. **14349** High-Q Bandstop Filters Exploiting Acoustic-Wave-Lumped-Element Resonators (AWLRs)
17. **14523** A Reconfigurable Microwave Combline Filter
18. **14526** A Tunable Metamaterial Resonator using Varactor Diodes to Facilitate the Design of Reconfigurable Microwave Circuits
19. **14405** Passive and Active Electrical Balance Duplexers

Data Converters

20. **14335** All-Digital Calibration of Timing Skews for TIADCs Using The Polyphase Decomposition
21. **14480** A 65 nm CMOS DAC Based on a Differentiating Arbitrary Waveform Generator Architecture for 5G Handset Transmitter

Frequency Synthesisers

22. **14330** A 0.05-to-10GHz, 19-to-22GHz, and 38-to-44GHz Frequency Synthesizer for Software-Defined Radios in 0.13-μm CMOS Process
23. **14302** Open Loop Fractional Division using Voltage Comparator based Digital-to-Time Converter