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Design of Reconfigurable dB-Linear Variable-Gain Amplifier and Switchable-Order Gm-C Filter in 65-nm CMOS Technology

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***Abstract*— A system approach for a power-scalable analog baseband (ABB) design is presented in this paper. Using this approach, the energy efficiency of an ABB can be maximized without compromising any other important specifications. To fulfill the feasibility study, a switchable-order g_m-C lowpass filter (LPF) along with a voltage-controlled programmable-gain amplifier (VC-PGA) are designed. The selectivity of the LPF can be linearly scaled with power consumption. In addition, the power consumption of the VC-PGA has a binary-weighted manner. In contrast to conventional PGAs, the gain step of the designed PGA can be continuously tuned by a control voltage. To prove the concept, the ABB is implemented in 65 nm CMOS technology. The measurements show that the frequency responses of the ABB can be configured as either 5th or 7th order with 16 gain steps. The bandwidth is approximately 50 MHz for all cases and the gain step can be continuously tuned between 0 and 3 dB. At the high-gain mode, the output 3rd-order intercept point (OIP3) and the input-referred noise (IRN) of the LPF and PGA are approximately to be 8 dBm and 5 nV/sqrt Hz, respectively. The maximum power consumption of the ABB, excluding the output buffer, is approximately 19.8 mW with a 1.2 V supply voltage. The die area, excluding the pads, is only 0.18 mm^2.**

***Index Terms*— CMOS, g_m-C filter, multiple-loop feedback, programmable-gain amplifier, reconfigurable baseband circuits.**

I. Introduction

EXISTING in any wireless system, analog baseband (ABB) circuits, including lowpass filters (LPFs) and programmable-gain amplifiers (PGAs), play a crucial role [1]-[26]. They are required to not only pass, but also amplify wanted signals with minimal degradation or distortion at given channels, while dramatically reject unwanted signals, such as noise, and spurious responses. It would otherwise harm signal integrity of the system. Many important parameters of a wireless system are strongly dependent on the performance of the ABB, and so ABB is a major topic for design of wireless systems [27], [28]. As the development of 5G communications, which provides higher data rate, operational flexibility, and environmental adaptability, full configurability in the transceiver architecture and constituent circuits is required to accommodate the large range of operation frequency, signal bandwidth, and power requirements. The design of dynamically reconfigurable analog, and mixed-signal circuits and systems is important yet challenging. Recently, there has been tremendous demand for reconfigurable ABB design, since it can be used for many applications, ranging from a cellular network, such as a software-defined radio [1]-[4], [6], to a recent automotive radar system [5]. All of these designs are targeted for data-constraint applications, where achieving high-speed data transfer is the primary requirement.

Coping with the carbon footprint of wireless communications makes us more concerned with the energy efficiency of wireless circuits. This is particularly true for many emerging applications, such as the Internet-of-things (IoTs) and wireless sensor networks (WSNs), where the energy efficiency and implementation cost are extremely constraint. Therefore, an initial generic system approach for power-scalable ABB designs with special emphasis on energy efficiency improvement was presented in [26]. Beyond the one initially presented, not only a voltage-controlled PGA (VC-PGA), but also the required switchable-order filtering solution at ABB is presented in this work. Moreover, the detailed design formulas are derived and summarized for filter implementation. Then, using the formulas, a filter design example that can switch the order between 5th and 7th is given along with the designed VC-PGA in [26] to provide a complete solution for reconfigurable ABB. Note that the presented approach is not designed for any specific application, but rather targets on a general scenario, in which energy efficiency and cost are critical. In addition, as a system approach, many previously presented circuit design techniques can be directly reused in a sub-circuit for this approach [8], [9]. The strong motivation of this work is to demonstrate how to linearly scale the power consumption with the selectivity of the LPF and the gain of the PGA, which has never been reported in the literature before, to the best of our knowledge. To verify the concept, a 5th-/7th-order LPF along with a voltage-controlled PGA is implemented in 65 nm CMOS technology.

The remainder of this paper is organized as follows. The concept of a power-scalable ABB will be firstly introduced in Section II. In Section III, the design of a switchable-order LPF

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based on a multiple-loop feedback (MLF) structure will be investigated. The design of a voltage-controlled PGA will be presented in Section IV. In Section V, the measurements will be given, followed by the conclusions in Section VI.

II. Design Considerations of the Proposed Power-Scalable Analog Baseband Circuits

The block diagram of the designed ABB is shown in Fig. 1. The primary function of the LPF is to provide sufficient selectivity to attenuate out-of-band interference to a level that does not adversely impact subsequent analog-to-digital conversion and demodulation processes [26]. Following the LPF, another important building block at ABB is the programmable-gain amplifier (PGA). The PGA is mainly used to improve the dynamic range of receiver [10]-[17]. Note that, if a relatively high swing is required for the system, a buffer will be applied along with the PGA.

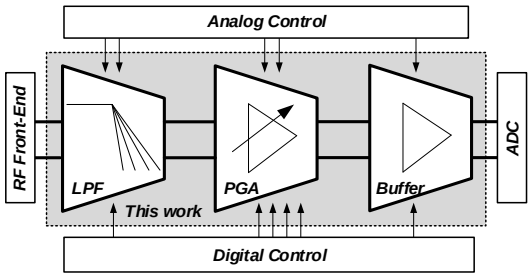

Fig. 1. The block diagram of the designed analog baseband circuits

A. Switchable-Order Gm-C Filter

Design of a switchable-order g_m-C filter using the LC-ladder simulation method is presented in [22]. The order of the LPF can only be reconfigured as either 5^{th} or 3^{rd} due to the inflexibility of the LC-ladder based method. The advantage of using a power-scalable approach over the conventional design is illustrated in Fig. 2(a). The LPF presented in [22] is used as a benchmark. The normalized power consumption of a LPF is plotted as a function of selectivity. As shown, the energy efficiency of the LPF can be improved by using the proposed approach, and this is particularly true if lower-order filtering is required. Moreover, in conventional PGA design, multiple fixed-gain stages are required to enlarge the overall gain range [3]. Although this approach is simple, the energy efficiency of this approach can also be further improved. To demonstrate the advantage of the power-scalable approach for PGA design over the conventional approach, the normalized power consumption of these two approaches as a function of gain is given in Fig. 2(b). As can be seen, using the proposed approach the power consumption of the PGA can be much more linearly scaled with gain than its counterpart that uses the conventional approach.

B. Voltage-Controlled PGA with Fine Gain Tuning

Besides the improved energy efficiency, a novel concept named voltage-controlled PGA (VC-PGA) is also presented in this work, which has a capability to fine-tune the gain step by a control voltage. In general, a PGA has a drawback that the total number of gain steps will be fixed, if the number of control bits is fixed. Therefore, the design decision has to be made to trade-off the gain range and the gain step. It is desirable to design a PGA with a capability to configure its gain step, which not only enables the PGA to be used for many different applications but also gives a flexibility to adjust the performance even after fabrication. Consequently, the design constraint between gain range and gain step can be dramatically reduced; otherwise, it would normally result in an overdesign.

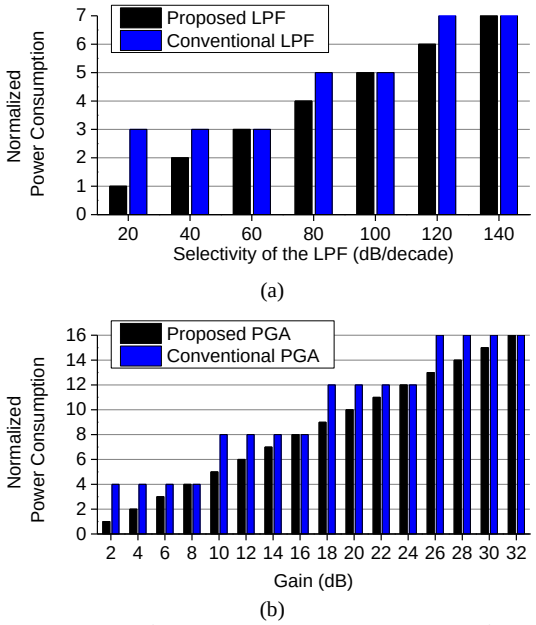

Fig. 2. Comparisons of the normalized power consumption of the proposed approach and the conventional one, (a) LPF, (b) PGA.

III. Design of Switchable-Order LPF Using MLF-Based Approach

Although extensive research has been done in the field of switchable-order LPF design, most published work is based on an active-RC structure [1], [3], [7], [21], [23]-[24], and only a few [4], [22], [25] use a g_m-C structure. Thus, in this work, we are only concerned with a g_m-C based design. To the best of our knowledge, using a system approach for a switchable-order g_m-C LPF design has only been explored to some extent in the literature [26]. Most of the previously published work is primarily focused on a circuit approach, such as transistor-level operational transconductance amplifier (OTA) design [4]. The benefit of further exploring a system approach for switchable-order filter design could be enormous, because it can offer not only flexibility of implementation from a filter-structure-selection point of view, but also the possibility of reusing any existing circuit approach to satisfy the requirements of linearity [8] and power consumption [4]. As a result, using an appropriate system approach for g_m-C LPF design, the overall performance of an LPF can be optimized in a relatively straightforward way.

A. Selection of Filter Order

The order of a filter should be chosen first of all to satisfy system requirements in terms of filtering performance. Based on this consideration, the order needs to be as low as possible. The main benefit for doing so is to reduce, not only the overall

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power consumption, but also the die area by means of using fewer components. In addition, design of lower-order filters is less complex. In the literature, the order of an analog filter at baseband ranges from 3rd to 8th order, with most using 4th/5th order to best trade-off circuit complexity and performance [1]-[3], [6]-[8], [21]-[24].

B. Selection of Filter Approximation

Design of a filter for analog signal processing at baseband is an iterative process, and system-level simulations may be required to investigate the impact of different filter approximations on the overall system performance. There are a variety of filter approximations that can be considered for design, such as Butterworth, Chebyshev, elliptic, linear-phase functions etc. The selection of an appropriate approximation is a complicated task, which needs to trade-off many factors, including stopband attenuation, power consumption, design complexity and cost [18]. Butterworth [1]-[4], Chebyshev [2], [9], [19], and elliptic [8] approximations have all been widely used for design. Among them, the Butterworth type is used more often due to the simplicity and ease of design in structure. In this paper, the Butterworth approximation is selected because, not only is the Butterworth response maximally flat and simplest, but also the Butterworth is the least selective, so often requires a higher order, such as 6th or 7th order. We believe that the higher the filter's order required, the more important that the filter's order needs to be switchable, so that the overall power consumption can be effectively controlled according to the system requirements.

C. Selection of System Approaches

Another important concern for switchable-order LPF design at baseband is to select an appropriate system approach, known as filter structure [25]. Among the various system approaches, the LC-ladder simulation [4], [8], [22], biquad cascade [9], [25], and multiple-loop feedback (MLF) approaches [19] and [26], are the most popularly used.

The LC-ladder simulation method is to use active circuits to replace the inductors in passive-ladder filter prototypes. Most known frequency responses can be realized using this approach. Also, the resulting active filters share the low sensitivity of the passive prototypes. However, the types of frequency response that can be implemented using this approach are constrained by those that can be realized as a passive-ladder filter, and some filter functions (e.g. linear-phase responses) may not be realizable using this approach. As far as switchable-order LPF design is concerned, the LC-ladder-based approach may be the least flexible due to its non-modular-based nature [4], [22]. It may require designing several filters with different orders and then merging them by reusing some components.

The biquad cascade consists of a series of independent second-order sections. Each of them provides a pair of complex conjugate poles to the overall frequency response. Although this approach yields a simple and modular circuit structure that is suitable for switchable-order design, it has a main drawback that the filter response is relatively sensitive to variations of component values [25]-[28].

MLF is a very general approach of active filter deign, of which biquad cascades and LC-ladders could be treated as a subset. An all-pole MLF filter consists of a cascade of g_m cells and grounded capacitors with multiple feedback paths between them [26]. If each g_m cell is designed to be identical, then any order of filter can be easily reconfigured by switching on/off the corresponding g_m cells, capacitors and feedback loops. Due to this modular-based nature, MLF-based approaches are particularly suitable for switchable-order LPF designs. In addition, they also offer minimum-component designs with low sensitivity. For these reasons, an MLF-based approach will be adopted for a switchable-order LPF design in this paper.

D. Motivation of Filter Design Using MLF Structure

It is noted that the theoretical works of using MLF structure for gm-C filter design has been explored to some extent in the literature since early 90s, it never caught on. One might even suspect that some flaws might have been uncovered that kept MLF-based approach out of the mainstream. Although there is no fatal flaw, synthesis of filter using MLF structure seems to be more complicated than the ones using of classical LC-ladder simulation and biquad cascade. In addition, the performance of the most of previously published works using MLF structures is only verified in simulation. To fully address these two concerns, synthesis of switchable-order gm-C filter using MLF IFLF structure will be derived in detail in the next Section. The performance of the designed LPF will be fully verified through on-wafer measurement.

E. Synthesis of a Switchable-Order Filter

As a starting point, the structure of an nth-order LPF using MLF inverse-follow-the-leader-feedback (IFLF) structure is given in Fig. 3(a). To implement this LPF, a 4-input g_m cell is required, as shown in Fig. 3(b). As illustrated, a classical single-stage differential amplifier is used with a cross-coupled load. This cross-coupled load acts as a negative resistance. By carefully selecting the device size of $M_{6,7}$, the open-loop DC gain of the g_m cell can be significantly boosted. To implement a 4-input cell, two identical 2-input cells are used and their outputs are connected together in parallel. Note that only a simple g_m cell is selected, because the motivation of this work is to demonstrate the feasibility of the presented approach rather than optimize a LPF for any specific application.

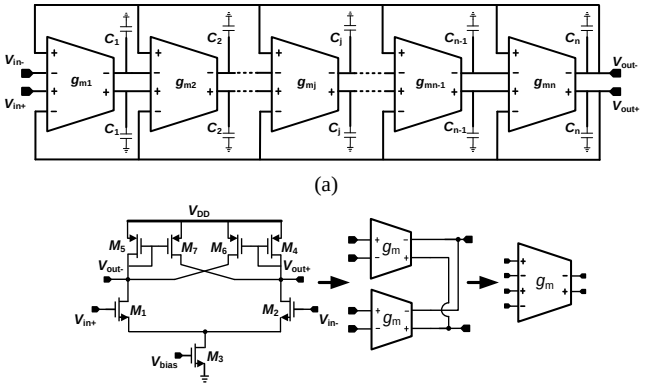

Fig. 3. MLF IFLF LPF structures and implementation of g_m cell. (a) All-pole MLF IFLF LPF structure. (b) Circuit implementation of g_m cell.

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The overall transfer function of an n[th]-order LPF can be written as

$$H(s) = \frac{1}{D(s)_{n^{th}}} = \frac{1}{B_n s^n + \cdots + B_2 s^2 + B_1 s + 1}. \quad (1)$$

In practice, the filter's order is likely to be configured from 3[rd] to 7[th] order. The transfer function of the LPF from 3[rd] to 7[th] orders [19]:

$$\begin{aligned}
D(s)_{3rd} &= \tau_1\tau_2\tau_3 s^3 + \tau_1\tau_2 s^2 + \tau_1 s + 1 \\
D(s)_{4th} &= \tau_1\tau_2\tau_3\tau_4 s^4 + \tau_1\tau_2\tau_3 s^3 + \tau_1\tau_2 s^2 + \tau_1 s + 1 \\
D(s)_{5th} &= \tau_1\tau_2\tau_3\tau_4\tau_5 s^5 + \tau_1\tau_2\tau_3\tau_4 s^4 + \tau_1\tau_2\tau_3 s^3 + \tau_1\tau_2 s^2 \\
&\quad + \tau_1 s + 1 \\
D(s)_{6th} &= \tau_1\tau_2\tau_3\tau_4\tau_5\tau_6 s^6 + \tau_1\tau_2\tau_3\tau_4\tau_5 s^5 + \tau_1\tau_2\tau_3\tau_4 s^4 \\
&\quad + \tau_1\tau_2\tau_3 s^3 + \tau_1\tau_2 s^2 + \tau_1 s + 1 \\
D(s)_{7th} &= \tau_1\tau_2\tau_3\tau_4\tau_5\tau_6\tau_7 s^7 + \tau_1\tau_2\tau_3\tau_4\tau_5\tau_6 s^6 \\
&\quad + \tau_1\tau_2\tau_3\tau_4\tau_5 s^5 + \tau_1\tau_2\tau_3\tau_4 s^4 + \tau_1\tau_2\tau_3 s^3 \\
&\quad + \tau_1\tau_2 s^2 + \tau_1 s + 1. \quad (2)
\end{aligned}$$

From (1) and (2), we find that

$$\tau_1 = B_1, \tau_2 = \frac{B_2}{B_1}, \tau_3 = \frac{B_3}{B_2}, \quad \cdots \quad \tau_n = \frac{B_n}{B_{n-1}}. \quad (3)$$

To implement a switchable-order Butterworth LPF using the structure presented in Fig. 3, the normalized characteristics of 3[rd]-, 4[th]-, 5[th]-, 6[th]- and 7[th]-order Butterworth LPFs at the cut-off frequency are given by:

$$H(s) = \frac{1}{D(s)} \quad (4)$$

with

$$\begin{aligned}
D(s)_{3rd} &= s^3 + 2s^2 + 2s + 1 \\
D(s)_{4th} &= s^4 + 2.613126s^3 + 3.414214s^2 + 2.613126s \\
&\quad + 1 \\
D(s)_{5th} &= s^5 + 3.236068s^4 + 5.236068s^3 + 5.236068s^2 \\
&\quad + 3.236068s + 1 \\
D(s)_{6th} &= s^6 + 3.863703s^5 + 7.464102s^4 + 9.141620s^3 \\
&\quad + 7.464102s^2 + 3.863703s + 1 \\
D(s)_{7th} &= s^7 + 4.493959s^6 + 10.097835s^5 \\
&\quad + 14.591794s^4 + 14.591794s^3 + 10.097835s^2 \\
&\quad + 4.493959s + 1. \quad (5)
\end{aligned}$$

By matching the coefficients between (2) and (5), the corresponding time constants τ_n are calculated and are summarized in Table I. The variables *n* and *j* are the maximum and minimum allowed filter orders that can be configured, respectively. Since $\tau_n = C_n/g_{mn}$, if identical transconductances are used, the corresponding capacitance values can be calculated accordingly. To minimize the die area of a reconfigurable LPF, it is necessary to share as much capacitance as possible. In doing so, the proposed switchable-order LPF structure is shown in Fig. 4. As shown, except for the last stage, two types of capacitors are used in the structure, the fixed capacitors and the switched capacitors. Note that the term ΔC_{x_y} refers to the required additional capacitors that are used for implementing different filter orders, and are controlled by switches denoted as S_2 to S_n. The variable *x* is the number of the stage to which the capacitors are connected. The variable *y* indicates the filter's order that the capacitors correspond to. For example, ΔC_{3_6} indicates that the capacitor is located at the third stage of a 6[th]-order LPF. As the filter's order is reconfigured, not only τ_n but also $\Delta\tau_n$ needs to be calculated for each switched order of a LPF. $\Delta\tau_n$ is the difference between corresponding time constants. To implement a Butterworth LPF with its order to be switched from 3[rd] to 7[th], $\Delta\tau_n$ is calculated and summarized in Table II.

TABLE I
CALCULATED TIME CONSTANTS OF 3[RD]- TO 7[TH]-ORDER BUTTERWORTH LPF, RESPECTIVELY.

	τ_1	τ_2	τ_3	τ_4	τ_5	τ_6	τ_7
3[rd]	2	1	0.5				
4[th]	2.61	1.31	0.77	0.38			
5[th]	3.24	1.62	1	0.62	0.31		
6[th]	3.86	1.93	1.23	0.82	0.52	0.26	
7[th]	4.49	2.25	1.45	1	0.7	0.45	0.22

TABLE II
SUMMARIZED TIME CONSTANTS FOR A BUTTERWORTH LPF WITH ITS ORDER SWITCHED FROM 3[RD] TO 7[TH].

	$\Delta\tau_1$	$\Delta\tau_2$	$\Delta\tau_3$	$\Delta\tau_4$	$\Delta\tau_5$	$\Delta\tau_6$	$\Delta\tau_7$
4[th]	0.61	0.31	0.27	0.38			
5[th]	0.62	0.31	0.24	0.24	0.31		
6[th]	0.63	0.31	0.23	0.2	0.21	0.26	
7[th]	0.63	0.32	0.22	0.18	0.17	0.19	0.22

The filter is designed with identical transconductance, using the g_m cell in Fig. 3(b), with a selected value of 1 mS. If the cut-off frequency of the filter is chosen as 50 MHz and a balanced structure is used, the capacitance values for a 3[rd]-order LPF can be firstly calculated as:

$$C_{1\_3} = 12.8 \text{ pF}, \quad C_{2\_3} = 6.4 \text{ pF}, \quad C_{3\_3} = 3.2 \text{ pF}. \quad (6)$$

Since $\Delta\tau_n = \Delta C_n/g_{mn}$, using the values presented in Table II the corresponding capacitance values can be calculated for implementation of 4[th]-, 5[th]-, 6[th]- and 7[th]-order LPFs, respectively.

4[th]-order:

$$\begin{aligned}
C_{1_4} &= C_{1_3} + \Delta C_{1_4} = 16.6 \text{ pF} \\
C_{2_4} &= C_{2_3} + \Delta C_{2_4} = 8.4 \text{ pF} \\
C_{3_4} &= C_{3_3} + \Delta C_{3_4} = 5 \text{ pF} \\
C_{4_4} &= \Delta C_{4_4} = 2.4 \text{ pF}. \quad (7)
\end{aligned}$$

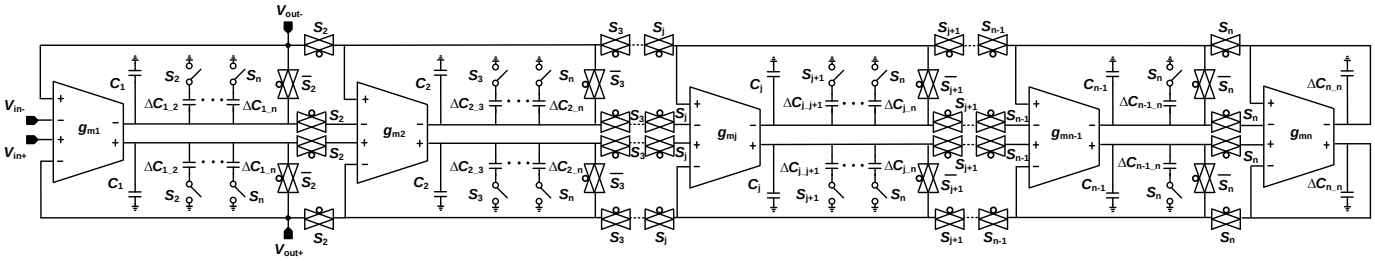

Fig. 4. Proposed reconfigurable MLF IFLF LPF structure.

5^{th}-order:

$$\begin{aligned} C_{1\_5} &= C_{1\_4} + \Delta C_{1\_5} = 20.6\ \text{pF} \\ C_{2\_5} &= C_{2\_4} + \Delta C_{2\_5} = 10.4\ \text{pF} \\ C_{3\_5} &= C_{3\_4} + \Delta C_{3\_5} = 6.4\ \text{pF} \\ C_{4\_5} &= C_{4\_4} + \Delta C_{4\_5} = 4\ \text{pF} \\ C_{5\_5} &= \Delta C_{5\_5} = 2\ \text{pF}. \end{aligned} \tag{8}$$

6^{th}-order:

$$\begin{aligned} C_{1\_6} &= C_{1\_5} + \Delta C_{1\_6} = 24.6\ \text{pF} \\ C_{2\_6} &= C_{2\_5} + \Delta C_{2\_6} = 12.2\ \text{pF} \\ C_{3\_6} &= C_{3\_5} + \Delta C_{3\_6} = 7.8\ \text{pF} \\ C_{4\_6} &= C_{4\_5} + \Delta C_{4\_6} = 6.4\ \text{pF} \\ C_{5\_6} &= C_{5\_5} + \Delta C_{5\_6} = 3.4\ \text{pF} \\ C_{6\_6} &= \Delta C_{6\_6} = 1.6\ \text{pF}. \end{aligned} \tag{9}$$

7^{th}-order:

$$\begin{aligned} C_{1\_7} &= C_{1\_6} + \Delta C_{1\_7} = 28.6\ \text{pF} \\ C_{2\_7} &= C_{2\_6} + \Delta C_{2\_7} = 14.4\ \text{pF} \\ C_{3\_7} &= C_{3\_6} + \Delta C_{3\_7} = 9.2\ \text{pF} \\ C_{4\_7} &= C_{4\_6} + \Delta C_{4\_7} = 6.4\ \text{pF} \\ C_{5\_7} &= C_{5\_6} + \Delta C_{5\_7} = 4.4\ \text{pF} \\ C_{6\_7} &= C_{6\_6} + \Delta C_{6\_7} = 2.8\ \text{pF} \\ C_{7\_7} &= \Delta C_{7\_7} = 1.4\ \text{pF}. \end{aligned} \tag{10}$$

Using the calculated values, a switchable-order LPF based on the MLF IFLF structure is implemented in 65 nm CMOS technology. The simulated frequency responses of the LPF are shown in Fig. 5. As illustrated, the LPF's order can be switched from 4^{th} to 7^{th} order.

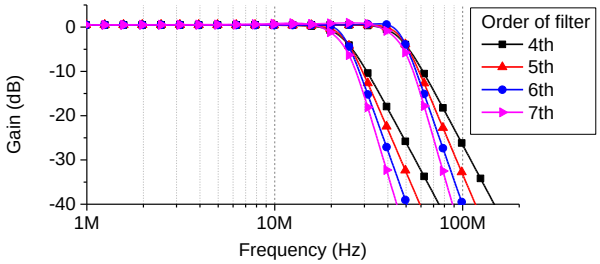

Fig. 5. Simulated frequency responses of the designed switchable-order filter.

F. Design of a 5^{th}-/7^{th}-order LPF

Although the presented MLF structure can be used to design a filter with any order, for this paper we only fabricated a 5^{th}-/7^{th}-order LPF due to the limited space (the space is mainly limited by the measurement pads, as shown in the die photo). The simplified LPF schematic is given in Fig. 6. As shown, only one bit is provided, which is S_7. As S_7 is enabled, the LPF will be configured as a 7^{th}-order LPF, which provides better roll-off; otherwise, the LPF will be configured as 5^{th} order, in which approximately 30% of the power can be saved for the LPF. Following with the previously presented design procedure, the capacitance values of the LPF corresponding to 7^{th} order can be calculated as

$$\begin{aligned} &\Delta C_{1\_7} = 8\ \text{pF}, \quad \Delta C_{2\_7} = 4\ \text{pF}, \quad \Delta C_{3\_7} = 2.8\ \text{pF}, \\ &\Delta C_{4\_7} = 2.4\ \text{pF}, \quad \Delta C_{5\_7} = 2.4\ \text{pF}, \quad \Delta C_{6\_7} = 2.8\ \text{pF}, \\ &\Delta C_{7\_7} = 1.4\ \text{pF}. \end{aligned} \tag{11}$$

where the fixed capacitance values are based on the 5^{th}-order LPF, which have been calculated in (6).

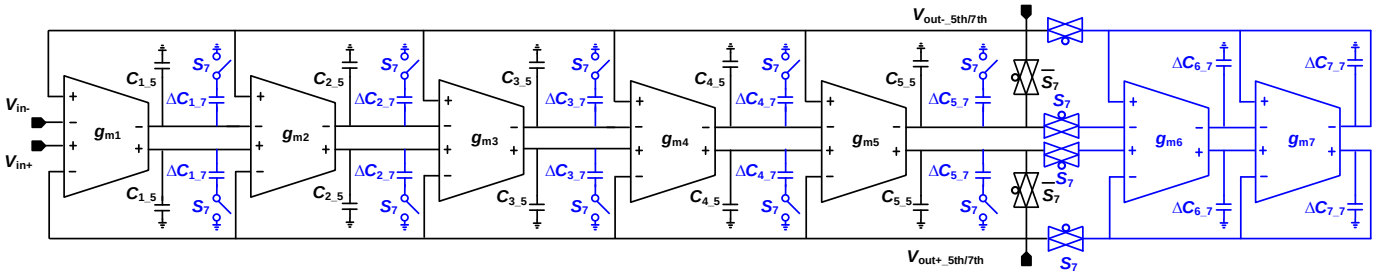

Fig. 6. Implementation of a 5^{th}-/7^{th}-order filter based on the structure presented in Fig. 4.

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G. *Discussion of Switch Implementation*

So far, the design is mainly focused on filter synthesis. As the filter's order becomes higher, impact on filter's response due to non-idealities of switches should be taken into consideration. There are two types of switch used in this design. One is the grounded switch, which is used to control the capacitor bank, while another one is the series switch, which is used to construct the feedback loop. The performance of these series connected switches is critical for the frequency response of the filter, as there can be as many as n-1 of them placed along the signal feedback path. In order to minimize the insertion loss of the switch, a classical transmission gate structure with p-MOS to n-MOS ratio of 2.5 is implemented. As indicated in Fig. 7, an n-MOS width of 5 μm is sufficiently large to minimize the unwanted loss.

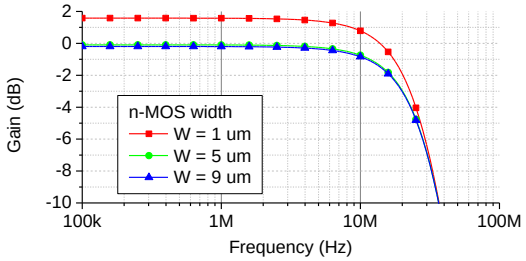

Fig. 7. The impact on filter behavior due to different transistor's widths for feedback control.

On the other hand, the width of transistor used to implement the grounded switch also needs to be carefully selected. As the switch is turned on, the on-resistance will be connected with the capacitor in series. Thus, the quality-factor (Q) of the capacitor could be affected. The impact on frequency response of the filter due to loading with capacitors with different Q is illustrated in Fig. 8. As shown, the value of Q needs to be maintained beyond 150 in order not to severely affecting the filter's performance. With a 1 pF capacitor at 50 MHz, the corresponding resistance is 21 Ω. The simulation results show that an n-MOS with size of 30 μm / 0.06 μm (Ron ≈ 19 Ω) is appropriate in this design. For both types of switches, the extra parasitic capacitance introduced by the switch is absorbed by the capacitor.

IV. Design of Voltage-Controlled Programmable-Gain Amplifier with Binary-Weighted Power Consumption

A. *Design Considerations of Voltage-Controlled PGA*

The conventional PGA uses a combination of fine and coarse gain tuning stages to achieve the required gain step, as shown in Fig. 9(a). However, there is an issue related to this approach. If only a single control bit is used for fine tuning, then the gain step of the PGA cannot be reconfigured at all. Using multiple control bits to provide re-configurability for a PGA not only increases the die area, but also makes the digital control more complicated. For example, using the PGA shown in Fig. 9(a), if the gain step of the PGA is reconfigured from 3 dB to 2 dB, the gain of the fixed-gain amplifier also needs to be changed to 6 dB to suit this gain change.

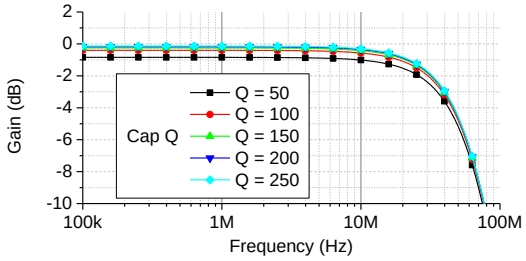

Fig. 8. The impact on filter behavior with various Q of capacitor.

In contrast, the proposed PGA in Fig. 9(b) utilizes a "cell based" approach [15]. In this approach, the gain setting of each stage is related to the gain of the unit cell. In other words, using the proposed approach for a PGA design, the gain step of the PGA is the gain of the unit cell. Thus, by changing the gain of the unit cell, the gain step of the PGA can be effectively reconfigured. Design of a unit cell that has such a capability to be reconfigured becomes the key to this approach. Two criteria need to be taken into account to implement the unit cell. Firstly, the power consumption of a state-of-the-art low-power VGA/PGA is only a few mW [10]-[17]. Thus the expected power consumption of the unit cell needs to be in the range of a few of hundred μW, which indicates that the power consumption of the unit cell needs to be aggressively reduced. Secondly, the size of the unit cell needs to be minimized. As shown in Fig. 9(b), several unit cells are cascaded; if the size of each cell is not minimized, the final PGA will lead to a relatively large die area. In addition, the gain control of a PGA is desirable to have a dB-linear characteristic, so that it would be easier to configure the PGA with required gain step. For this reason, the dB-linear gain error of the unit cell needs to be extremely small; otherwise, the gain error of the cell can accumulate and thus cause an excessive gain error of the PGA.

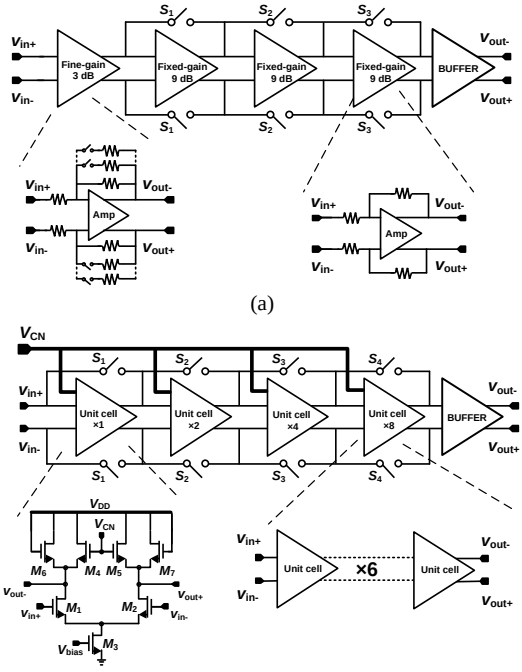

Fig. 9. Block diagrams and simplified schematics of (a) conventional op-amp based PGA and (b) proposed PGA with adjustable gain steps.

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B. *Implementation of PGA*

To design such a unit cell, a solution based on current steering between p-MOS and n-MOS was presented in [15]. One of the most critical issues related to the VGA design using this structure is that the accurate dB-linear gain characteristic might not be properly maintained, especially under some extreme conditions, such as SF and FS corners. To solve this issue to some extent, a one-time calibration is recommended to setup the correct bias voltage in [15]. There is no doubt that this calibration procedure brings another degree of complexity into the design. Unlike that work, to fundamentally solve this issue, the designed unit cell in this work uses n-MOS only, which helps to minimize the effects caused by process, voltage and temperature (PVT) variations.

As illustrated, $M_{1,\,2}$ are the input differential pair. M_3 acts as the tail current source that controls the bias current. To achieve a dB-linear characteristic, a pair of transistors $M_{4,\,5}$ are used as load and biased in the sub-threshold region, while another pair of transistors M_6 and M_7 are biased in the saturation region. By inspection, the gain is derived as:

$$A_v = \frac{v_{out}}{v_{in}} = \frac{g_{m,1,2}}{g_{m,4,5} + g_{m,6,7}} \tag{12}$$

where g_m is the transconductance of the relevant transistor. Equation (12) can be rewritten to include the changes in g_m as:

$$A_v = \frac{g_{m,1,2}}{g_{m,4,5} + g_{m,6,7} + \Delta g_{m,4,5} + \Delta g_{m,6,7}}. \tag{13}$$

The bias conditions of the input differential-pair transistors M_1 and M_2 are fixed at all times, thus the current relationship between $I_{DS,4,5}$ and $I_{DS,6,7}$ can be expressed as:

$$I_{DS,1,2} = I_{DS,4,5} + I_{DS,6,7} \tag{14}$$

and thus:

$$\Delta I_{DS,4,5} = -\Delta I_{DS,6,7} = \Delta I_{DS}. \tag{15}$$

As the transistors M_4 and M_5 are biased in the sub-threshold region, while the other transistors M_6 and M_7 are biased in the saturation region, $g_{m4,5}$ and $g_{m6,7}$ can be expressed as:

$$g_{m,4,5} = \frac{2I_{DS,4,5}}{nV_T}, g_{m,6,7} = \sqrt{2\mu_N C_{ox}\left(\frac{W}{L}\right)_{6,7}} \cdot \sqrt{I_{DS,6,7}}. \tag{16}$$

Differentiating $g_{m,4,5}$ w.r.t. $I_{DS,4,5}$ and $g_{m,6,7}$ w.r.t. $I_{DS,6,7}$ gives:

$$\Delta g_{m,4,5} = \frac{2}{nV_T}\Delta I_{DS}, \Delta g_{m,6,7} = \frac{\mu_N C_{ox}\left(\frac{W}{L}\right)_{6,7}}{g_{m,6,7}}\Delta I_{DS}. \tag{17}$$

Substituting (16) and (17) into (13) leads to

$$A_v = \frac{g_{m,1,2}}{Y + X} \tag{18}$$

where

$$X = \left(\frac{2}{nV_T} - \frac{\mu_N C_{ox}\left(\frac{W}{L}\right)_{6,7}}{g_{m,6,7}}\right)\Delta I_{DS} \tag{19}$$

$$Y = g_{m,4,5} + g_{m,6,7}. \tag{20}$$

As demonstrated in (17), the gain of the unit cell can be varied by changing ΔI_{DS}. If the term X is designed to be much smaller than Y, the impact of changing ΔI_{DS} on gain will be small. Thus, a small gain range with a good dB-linear characteristic can be expected. On the other hand, if X is not much smaller than Y, the relatively large gain range can only be achieved by compromising the dB-linear gain error. Since the transistors M_4 and M_5 are biased in the sub-threshold region, ΔI_{DS} can be easily changed by varying the gate voltage of M_4 and M_5. To further elaborate this viewpoint, in Fig. 10(a) and 10(b), the gain of the unit cell is plotted as a function of V_{CN} with different widths of $M_{6,\,7}$ and $M_{4,\,5}$, respectively. By carefully selecting the sizes of the devices, $M_{4,\,5,\,6,\,7}$, the gain range and gain error of the unit cell can be optimized. Although there is a discrepancy between the simulated and predicted results, the tendencies of the gain characteristic for both cases are similar. The discrepancy is likely to be caused by the limited output resistance of the devices, which is ignored for the sake of a simplified analysis. The following procedure can be used to design the unit cell with an accurate dB-linear characteristic. First of all, the sizes of the input transistors M_1 and M_2 can be chosen based on the required power consumption. Secondly, given the required gain of the unit cell, a selection of the sizes of M_4 and M_5 can be chosen. Finally, to achieve an accurate dB-linear characteristic, the sizes of M_6 and M_7 can be optimized accordingly.

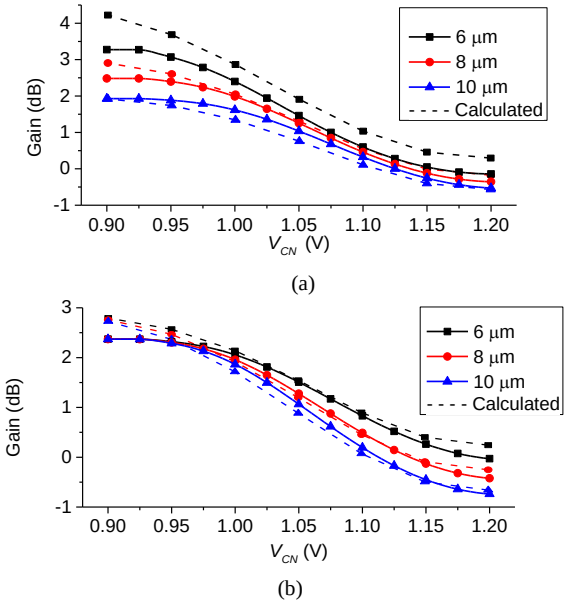

Fig. 10. Simulated gain characteristic of the designed cell, (a) different width of $M_{6,\,7}$ (b) different width of $M_{4,\,5}$.

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V. Measurement Results

To verify the functionality of the designed ABB, both the LPF and PGA are fabricated in standard 65 nm CMOS technology. The chip microphotograph is shown in Fig. 11. The core of the ABB occupies 600 × 300 μm^2. Note that the bottom-row pads are used for other test structures, which are not used for the designed ABB circuits. The on-wafer measurement was performed using an Agilent E8364B vector network analyser (VNA) connected to the SGS pads at the sides. Baluns are added at both input and output of the proposed ABB circuits for measurement of differential signal. The insertion loss of the output buffer of 9 dB is de-embedded from all figures and tables. A 100-Ω resistor is placed between the differential inputs, so that a standard 50-Ω input impedance matching can be realized for stand-alone ABB measurements.

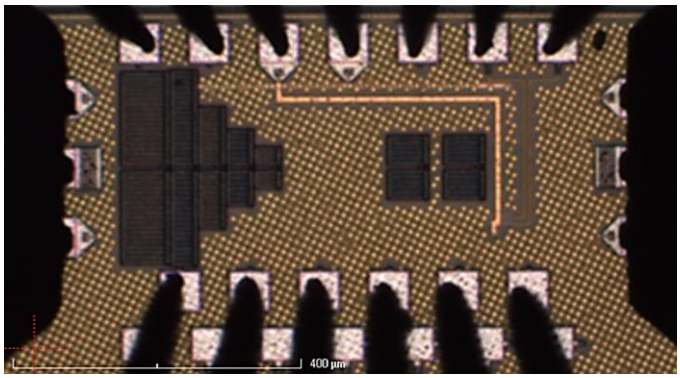
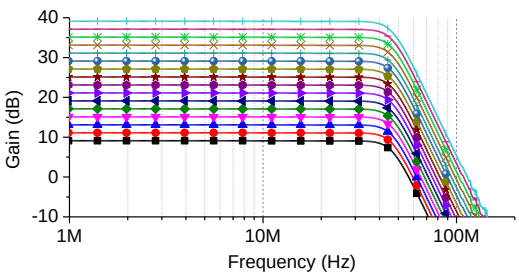


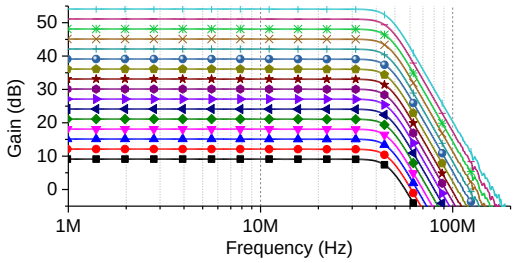
Fig. 11. Microphotograph of the designed ABB circuit.

The 5th- and 7th-order frequency responses of the designed ABB are shown in Fig. 12 and Fig. 13, respectively. As illustrated in both figures, regardless of the order of the frequency response and gain step, a bandwidth of 50 MHz can always be achieved. In addition, switching the order of the LPF does not affect the gain characteristic of the PGA. To demonstrate the robustness of the design, the simulated frequency responses of the ABB are not only compared with the measured results, as shown in Fig. 14, but also with the Monte Carlo simulation results of 100 runs as shown in Fig. 15.

In Fig. 16, the gain characteristics of the ABB with different gain steps are plotted against the control word. Since a 4-bit control word is used to control the gain, the control word can be varied from 0 (0000 in binary) to 15 (1111 in binary). The gain step of the ABB can be reconfigured from 2 to 3 dB, which results in a gain range variation from 30 to 45 dB. Moreover, in both cases, a good dB-linear characteristic can be achieved.

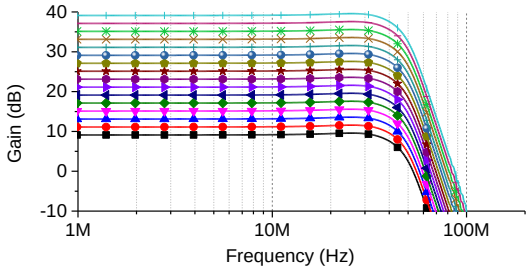


(a)

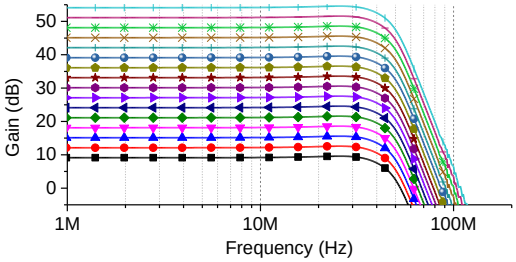


(b)

Fig. 12. Measured 5th-order frequency responses of the ABB. (a) 2 dB gain step. (b) 3 dB gain step.



(a)



(b)

Fig. 13. Measured 7th-order frequency responses of the ABB. (a) 2 dB gain step. (b) 3 dB gain step.

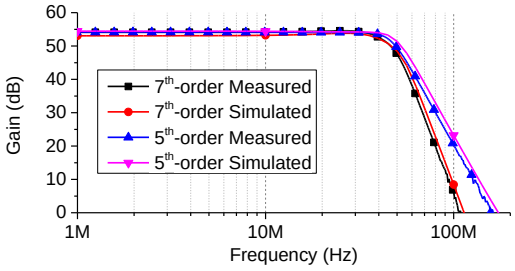


Fig. 14. Measured and simulated frequency responses of the designed ABB.

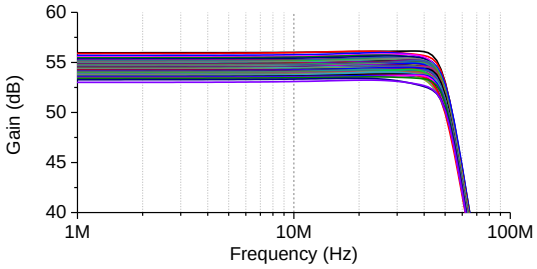


Fig. 15. The frequency responses of the designed ABB with Monte Carlo simulation results of 100 runs.

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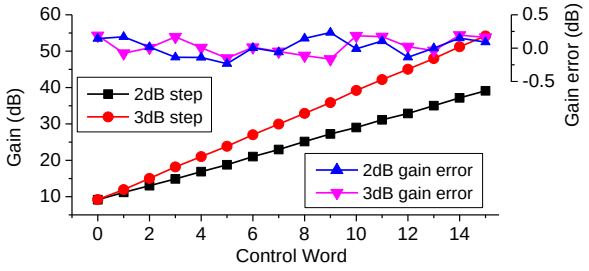

Fig. 16. Measured gain characteristics of the ABB with different gain steps.

Within the above-mentioned gain range, the measured in-band output 3rd-order intercept point IP3 (OIP3) and the noise figure (NF) of the ABB are shown in Fig. 17. For the OIP3 measurement, two-tone signals (10 and 11 MHz) are used at the input. Measurements also show that the dc power consumption of the LPF and PGA can be varied from 5.3 mW (5th-order LPF with low-gain mode PGA) to 19.8 mW (7th-order LPF with high-gain mode) from a 1.2 V power supply. The detailed power breakdown is shown in Fig. 18.

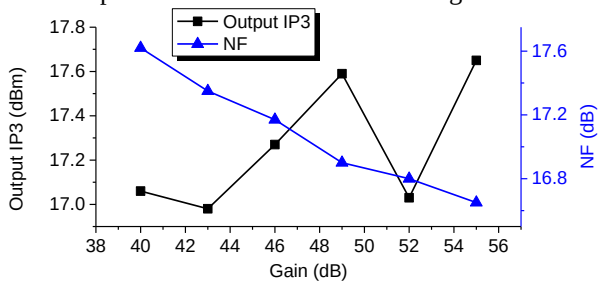

Fig. 17. Measured OIP3 and NF of the ABB as a function of gain.

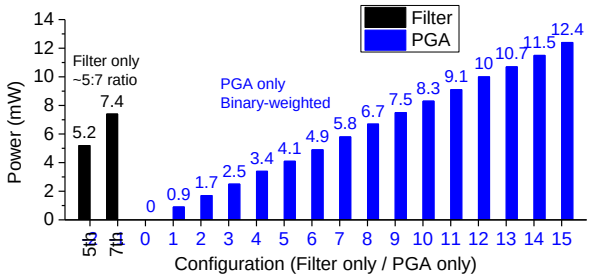

Fig. 18. Measured power vs selectivity for filter and power vs gain for PGA.

A performance summary of the designed ABB circuits and its comparisons with other state-of-the-art designs are given in Table III. Due to the fact that open-loop structures are used for both g_m-C filter and PGA, our designed ABB has the smallest die area, which would result in a dramatically reduced fabrication cost. Since different designs have different bandwidths and power consumption, only the energy efficiency (ratio of bandwidth over maximum power consumption) is compared in the Table. As can be seen, the presented design has a good energy efficiency compared to other designs. Although closed-loop-based design could achieve better OIP3, a penalty has to be paid on not only power consumption but also chip area. The linearity, which is sufficient for many applications, can always be traded-off to a certain extent with power consumption. Last but not least, the presented ABB is the only one that has the capability to continuously tune the gain step, which could significantly relax the trade-off between a large gain range and a small gain step.

TABLE III
PERFORMANCE SUMMARY OF THE DESIGNED ABB CIRCUITS AND ITS COMPARISONS WITH OTHER STATE-OF-THE-ART DESIGNS

Ref	Topology	f_{-3dB} (MHz)	Energy efficiency (MHz/mW)	OIP3 (dBm)	IRN (nV/sqrt Hz)	Gain range (dB)	Gain step (dB)	Area (mm^2)	Note
[1]	Active-Gm-RC filter + resistive feedback PGA	24	1.1	27	33	0-39	3	1.56	Biquad cascade
[2]	Gm-C filter + resistive feedback PGA	30	2.3	16	n/a	0-48	0.5	0.57	Ladder simulation
[3]	Active-RC filter + resistive feedback PGA	20	2	18	87	0-72	6	0.8	Biquad cascade
[6]	Gm-C filter + PGA	30	1.9	8	n/a	0-71	1	1.1	Ladder simulation
[7]	Active RC filter	18	0.9	12.5	35	-	-	0.97	Biquad cascade
[21]	Active RC filter	20	-	26	52	-	-	-	Biquad cascade
[22]	Gm-C filter	2.75	0.83	27	40	-	-	0.57	Ladder simulation
[23]	Active-Gm-RC filter	11	0.77	17	-	-	-	0.9	Biquad cascade
This work	Gm-C filter + voltage-controlled PGA	50	2.5	8	5	9-54	2/3	0.18	Multiple-loop Feedback

VI. CONCLUSION

A novel system approach for power-scalable ABB circuits design in CMOS technology has been presented in this paper, including a switchable-order g_m-C LPF using an MLF IFLF structure and a VC-PGA with binary-weighted power consumption. Both circuits are designed and fabricated in a standard 65 nm CMOS technology. As demonstrated, the

presented approach is particularly suitable for a reconfigurable ABB design with improved energy efficiency. It therefore can be concluded that the presented system approach not only has the potential to be used for software-defined radios, but also can be considered as a solution for many applications which require low cost and high energy efficiency, such as 5G communication, WSNs and IoTs. In addition, the proposed design technique of a PGA may be used to enhance the circuit's yield, as the gain step of the PGA can be fine-tuned after fabrication, which is not the case for conventional op-amp based designs.

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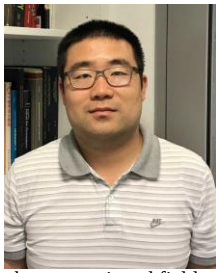

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