### G. *Discussion of Switch Implementation*

So far, the design is mainly focused on filter synthesis. As the filter's order becomes higher, impact on filter's response due to non-idealities of switches should be taken into consideration. There are two types of switch used in this design. One is the grounded switch, which is used to control the capacitor bank, while another one is the series switch, which is used to construct the feedback loop. The performance of these series connected switches is critical for the frequency response of the filter, as there can be as many as n-1 of them placed along the signal feedback path. In order to minimize the insertion loss of the switch, a classical transmission gate structure with p-MOS to n-MOS ratio of 2.5 is implemented. As indicated in Fig. 7, an n-MOS width of 5 μm is sufficiently large to minimize the unwanted loss.

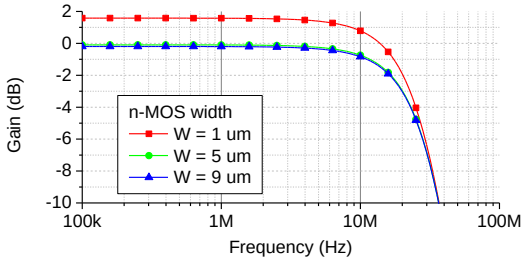



Fig. 7. The impact on filter behavior due to different transistor's widths for feedback control.

On the other hand, the width of transistor used to implement the grounded switch also needs to be carefully selected. As the switch is turned on, the on-resistance will be connected with the capacitor in series. Thus, the quality-factor (Q) of the capacitor could be affected. The impact on frequency response of the filter due to loading with capacitors with different Q is illustrated in Fig. 8. As shown, the value of Q needs to be maintained beyond 150 in order not to severely affecting the filter's performance. With a 1 pF capacitor at 50 MHz, the corresponding resistance is 21 Ω. The simulation results show that an n-MOS with size of 30 μm / 0.06 μm (Ron ≈ 19 Ω) is appropriate in this design. For both types of switches, the extra parasitic capacitance introduced by the switch is absorbed by the capacitor.

## IV. Design of Voltage-Controlled Programmable-Gain Amplifier with Binary-Weighted Power Consumption

### A. *Design Considerations of Voltage-Controlled PGA*

The conventional PGA uses a combination of fine and coarse gain tuning stages to achieve the required gain step, as shown in Fig. 9(a). However, there is an issue related to this approach. If only a single control bit is used for fine tuning, then the gain step of the PGA cannot be reconfigured at all. Using multiple control bits to provide re-configurability for a PGA not only increases the die area, but also makes the digital control more complicated. For example, using the PGA shown in Fig. 9(a), if the gain step of the PGA is reconfigured from 3 dB to 2 dB, the gain of the fixed-gain amplifier also needs to be changed to 6 dB to suit this gain change.

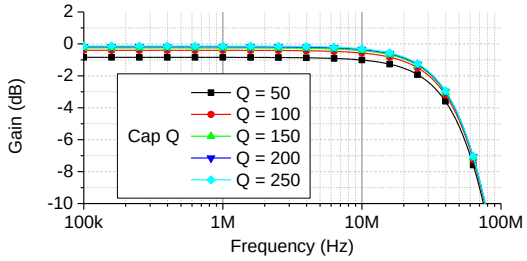



Fig. 8. The impact on filter behavior with various Q of capacitor.

In contrast, the proposed PGA in Fig. 9(b) utilizes a "cell based" approach [15]. In this approach, the gain setting of each stage is related to the gain of the unit cell. In other words, using the proposed approach for a PGA design, the gain step of the PGA is the gain of the unit cell. Thus, by changing the gain of the unit cell, the gain step of the PGA can be effectively reconfigured. Design of a unit cell that has such a capability to be reconfigured becomes the key to this approach. Two criteria need to be taken into account to implement the unit cell. Firstly, the power consumption of a state-of-the-art low-power VGA/PGA is only a few mW [10]-[17]. Thus the expected power consumption of the unit cell needs to be in the range of a few of hundred μW, which indicates that the power consumption of the unit cell needs to be aggressively reduced. Secondly, the size of the unit cell needs to be minimized. As shown in Fig. 9(b), several unit cells are cascaded; if the size of each cell is not minimized, the final PGA will lead to a relatively large die area. In addition, the gain control of a PGA is desirable to have a dB-linear characteristic, so that it would be easier to configure the PGA with required gain step. For this reason, the dB-linear gain error of the unit cell needs to be extremely small; otherwise, the gain error of the cell can accumulate and thus cause an excessive gain error of the PGA.

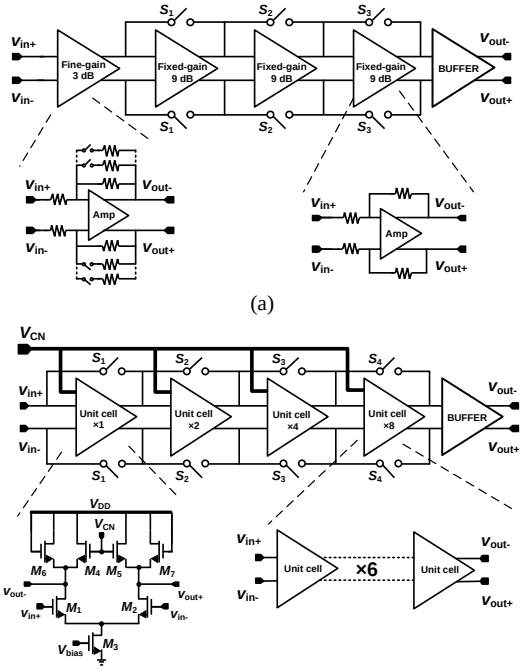



Fig. 9. Block diagrams and simplified schematics of (a) conventional op-amp based PGA and (b) proposed PGA with adjustable gain steps.

### B. *Implementation of PGA*

To design such a unit cell, a solution based on current steering between p-MOS and n-MOS was presented in [15]. One of the most critical issues related to the VGA design using this structure is that the accurate dB-linear gain characteristic might not be properly maintained, especially under some extreme conditions, such as SF and FS corners. To solve this issue to some extent, a one-time calibration is recommended to setup the correct bias voltage in [15]. There is no doubt that this calibration procedure brings another degree of complexity into the design. Unlike that work, to fundamentally solve this issue, the designed unit cell in this work uses n-MOS only, which helps to minimize the effects caused by process, voltage and temperature (PVT) variations.

As illustrated, $M_{1,\ 2}$ are the input differential pair. $M_3$ acts as the tail current source that controls the bias current. To achieve a dB-linear characteristic, a pair of transistors $M_{4,\ 5}$ are used as load and biased in the sub-threshold region, while another pair of transistors $M_6$ and $M_7$ are biased in the saturation region. By inspection, the gain is derived as:

$$A_v = \frac{v_{out}}{v_{in}} = \frac{g_{m,1,2}}{g_{m,4,5} + g_{m,6,7}} \tag{12}$$

where $g_m$ is the transconductance of the relevant transistor. Equation (12) can be rewritten to include the changes in $g_m$ as:

$$A_v = \frac{g_{m,1,2}}{g_{m,4,5} + g_{m,6,7} + \Delta g_{m,4,5} + \Delta g_{m,6,7}}. \tag{13}$$

The bias conditions of the input differential-pair transistors $M_1$ and $M_2$ are fixed at all times, thus the current relationship between $I_{DS,4,5}$ and $I_{DS,6,7}$ can be expressed as:

$$I_{DS,1,2} = I_{DS,4,5} + I_{DS,6,7} \tag{14}$$

and thus:

$$\Delta I_{DS,4,5} = -\Delta I_{DS,6,7} = \Delta I_{DS}. \tag{15}$$

As the transistors $M_4$ and $M_5$ are biased in the sub-threshold region, while the other transistors $M_6$ and $M_7$ are biased in the saturation region, $g_{m4,5}$ and $g_{m6,7}$ can be expressed as:

$$g_{m,4,5} = \frac{2I_{DS,4,5}}{nV_T}, g_{m,6,7} = \sqrt{2\mu_N C_{ox}\left(\frac{W}{L}\right)_{6,7}} \cdot \sqrt{I_{DS,6,7}}. \tag{16}$$

Differentiating $g_{m,4,5}$ w.r.t. $I_{DS,4,5}$ and $g_{m,6,7}$ w.r.t. $I_{DS,6,7}$ gives:

$$\Delta g_{m,4,5} = \frac{2}{nV_T}\Delta I_{DS}, \Delta g_{m,6,7} = \frac{\mu_N C_{ox}\left(\frac{W}{L}\right)_{6,7}}{g_{m,6,7}}\Delta I_{DS}. \tag{17}$$

Substituting (16) and (17) into (13) leads to

$$A_v = \frac{g_{m,1,2}}{Y + X} \tag{18}$$

where

$$X = \left(\frac{2}{nV_T} - \frac{\mu_N C_{ox}\left(\frac{W}{L}\right)_{6,7}}{g_{m,6,7}}\right)\Delta I_{DS} \tag{19}$$

$$Y = g_{m,4,5} + g_{m,6,7}. \tag{20}$$

As demonstrated in (17), the gain of the unit cell can be varied by changing $\Delta I_{DS}$. If the term $X$ is designed to be much smaller than $Y$, the impact of changing $\Delta I_{DS}$ on gain will be small. Thus, a small gain range with a good dB-linear characteristic can be expected. On the other hand, if $X$ is not much smaller than $Y$, the relatively large gain range can only be achieved by compromising the dB-linear gain error. Since the transistors $M_4$ and $M_5$ are biased in the sub-threshold region, $\Delta I_{DS}$ can be easily changed by varying the gate voltage of $M_4$ and $M_5$. To further elaborate this viewpoint, in Fig. 10(a) and 10(b), the gain of the unit cell is plotted as a function of $V_{CN}$ with different widths of $M_{6,\ 7}$ and $M_{4,\ 5}$, respectively. By carefully selecting the sizes of the devices, $M_{4,\ 5,\ 6,\ 7}$, the gain range and gain error of the unit cell can be optimized. Although there is a discrepancy between the simulated and predicted results, the tendencies of the gain characteristic for both cases are similar. The discrepancy is likely to be caused by the limited output resistance of the devices, which is ignored for the sake of a simplified analysis. The following procedure can be used to design the unit cell with an accurate dB-linear characteristic. First of all, the sizes of the input transistors $M_1$ and $M_2$ can be chosen based on the required power consumption. Secondly, given the required gain of the unit cell, a selection of the sizes of $M_4$ and $M_5$ can be chosen. Finally, to achieve an accurate dB-linear characteristic, the sizes of $M_6$ and $M_7$ can be optimized accordingly.

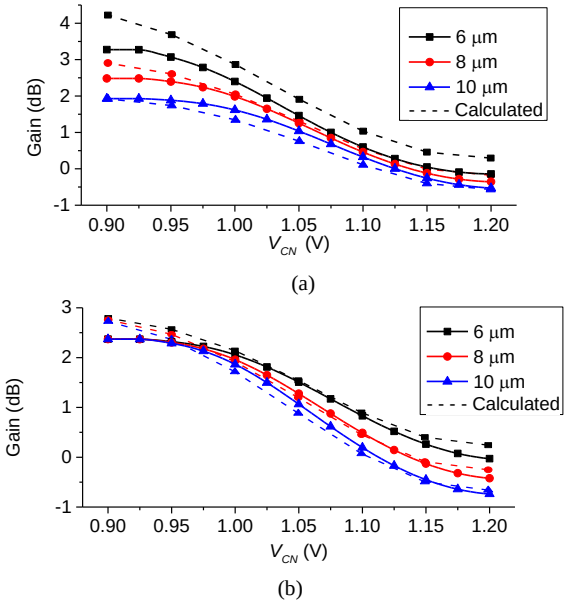



Fig. 10. Simulated gain characteristic of the designed cell, (a) different width of $M_{6,\ 7}$ (b) different width of $M_{4,\ 5}$.

## V. Measurement Results

To verify the functionality of the designed ABB, both the LPF and PGA are fabricated in standard 65 nm CMOS technology. The chip microphotograph is shown in Fig. 11. The core of the ABB occupies 600 × 300 $\mu m^2$. Note that the bottom-row pads are used for other test structures, which are not used for the designed ABB circuits. The on-wafer measurement was performed using an Agilent E8364B vector network analyser (VNA) connected to the SGS pads at the sides. Baluns are added at both input and output of the proposed ABB circuits for measurement of differential signal. The insertion loss of the output buffer of 9 dB is de-embedded from all figures and tables. A 100-Ω resistor is placed between the differential inputs, so that a standard 50-Ω input impedance matching can be realized for stand-alone ABB measurements.

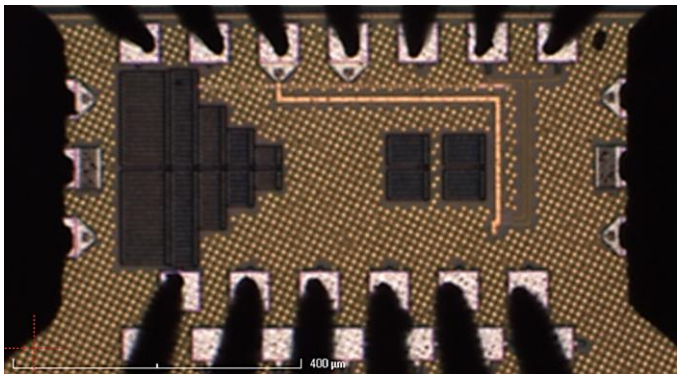
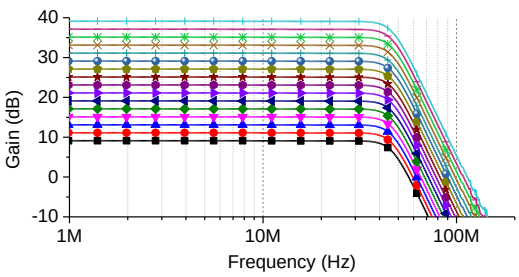


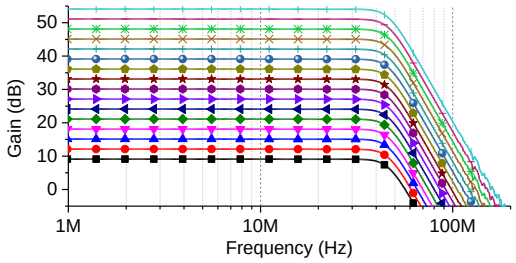

Fig. 11. Microphotograph of the designed ABB circuit.

The 5th- and 7th-order frequency responses of the designed ABB are shown in Fig. 12 and Fig. 13, respectively. As illustrated in both figures, regardless of the order of the frequency response and gain step, a bandwidth of 50 MHz can always be achieved. In addition, switching the order of the LPF does not affect the gain characteristic of the PGA. To demonstrate the robustness of the design, the simulated frequency responses of the ABB are not only compared with the measured results, as shown in Fig. 14, but also with the Monte Carlo simulation results of 100 runs as shown in Fig. 15.

In Fig. 16, the gain characteristics of the ABB with different gain steps are plotted against the control word. Since a 4-bit control word is used to control the gain, the control word can be varied from 0 (0000 in binary) to 15 (1111 in binary). The gain step of the ABB can be reconfigured from 2 to 3 dB, which results in a gain range variation from 30 to 45 dB. Moreover, in both cases, a good dB-linear characteristic can be achieved.

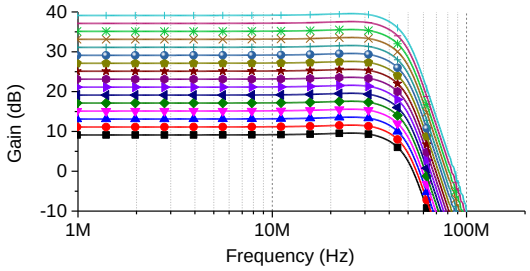



(a)

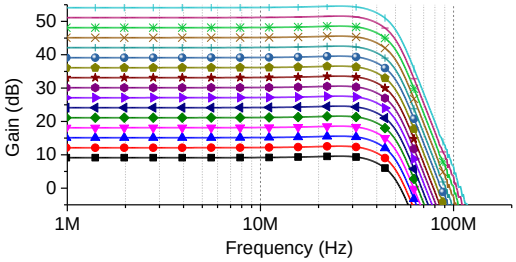



(b)

Fig. 12. Measured 5th-order frequency responses of the ABB. (a) 2 dB gain step. (b) 3 dB gain step.




(a)




(b)

Fig. 13. Measured 7th-order frequency responses of the ABB. (a) 2 dB gain step. (b) 3 dB gain step.

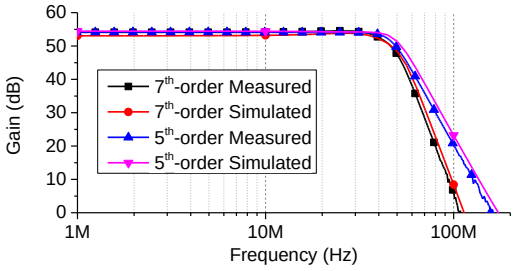



Fig. 14. Measured and simulated frequency responses of the designed ABB.

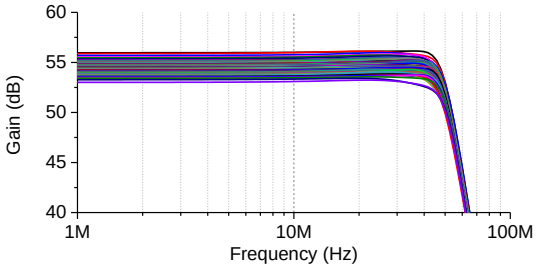



Fig. 15. The frequency responses of the designed ABB with Monte Carlo simulation results of 100 runs.

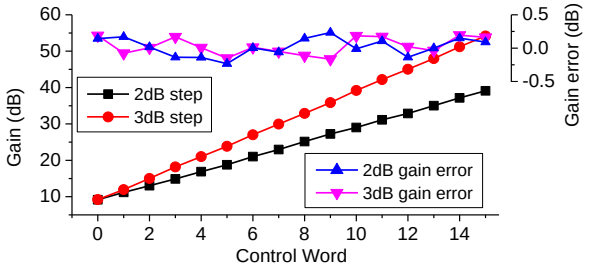



Fig. 16. Measured gain characteristics of the ABB with different gain steps.

Within the above-mentioned gain range, the measured in-band output 3rd-order intercept point IP3 (OIP3) and the noise figure (NF) of the ABB are shown in Fig. 17. For the OIP3 measurement, two-tone signals (10 and 11 MHz) are used at the input. Measurements also show that the dc power consumption of the LPF and PGA can be varied from 5.3 mW (5th-order LPF with low-gain mode PGA) to 19.8 mW ($7^{th}$-order LPF with high-gain mode) from a 1.2 V power supply. The detailed power breakdown is shown in Fig. 18.

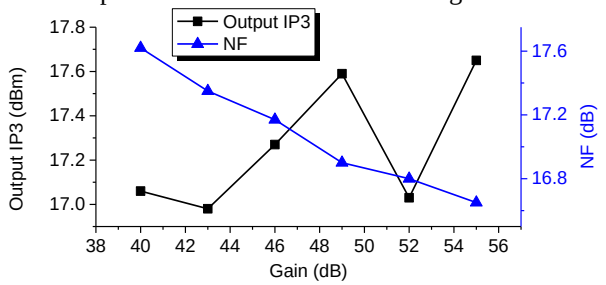



Fig. 17. Measured OIP3 and NF of the ABB as a function of gain.

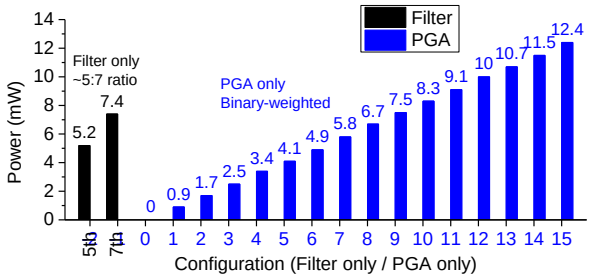



Fig. 18. Measured power vs selectivity for filter and power vs gain for PGA.

A performance summary of the designed ABB circuits and its comparisons with other state-of-the-art designs are given in Table III. Due to the fact that open-loop structures are used for both $g_m$-C filter and PGA, our designed ABB has the smallest die area, which would result in a dramatically reduced fabrication cost. Since different designs have different bandwidths and power consumption, only the energy efficiency (ratio of bandwidth over maximum power consumption) is compared in the Table. As can be seen, the presented design has a good energy efficiency compared to other designs. Although closed-loop-based design could achieve better OIP3, a penalty has to be paid on not only power consumption but also chip area. The linearity, which is sufficient for many applications, can always be traded-off to a certain extent with power consumption. Last but not least, the presented ABB is the only one that has the capability to continuously tune the gain step, which could significantly relax the trade-off between a large gain range and a small gain step.

TABLE III
PERFORMANCE SUMMARY OF THE DESIGNED ABB CIRCUITS AND ITS COMPARISONS WITH OTHER STATE-OF-THE-ART DESIGNS

| Ref | Topology | $f_{-3dB}$ (MHz) | Energy efficiency (MHz/mW) | OIP3 (dBm) | IRN (nV/sqrt Hz) | Gain range (dB) | Gain step (dB) | Area ($mm^2$) | Note |
|---|---|---|---|---|---|---|---|---|---|
| [1] | Active-Gm-RC filter + resistive feedback PGA | 24 | 1.1 | 27 | 33 | 0-39 | 3 | 1.56 | Biquad cascade |
| [2] | Gm-C filter + resistive feedback PGA | 30 | 2.3 | 16 | n/a | 0-48 | 0.5 | 0.57 | Ladder simulation |
| [3] | Active-RC filter + resistive feedback PGA | 20 | 2 | 18 | 87 | 0-72 | 6 | 0.8 | Biquad cascade |
| [6] | Gm-C filter + PGA | 30 | 1.9 | 8 | n/a | 0-71 | 1 | 1.1 | Ladder simulation |
| [7] | Active RC filter | 18 | 0.9 | 12.5 | 35 | - | - | 0.97 | Biquad cascade |
| [21] | Active RC filter | 20 | - | 26 | 52 | - | - | - | Biquad cascade |
| [22] | Gm-C filter | 2.75 | 0.83 | 27 | 40 | - | - | 0.57 | Ladder simulation |
| [23] | Active-Gm-RC filter | 11 | 0.77 | 17 | - | - | - | 0.9 | Biquad cascade |
| This work | Gm-C filter + voltage-controlled PGA | 50 | 2.5 | 8 | 5 | 9-54 | 2/3 | 0.18 | Multiple-loop Feedback |

## VI. CONCLUSION

A novel system approach for power-scalable ABB circuits design in CMOS technology has been presented in this paper, including a switchable-order $g_m$-C LPF using an MLF IFLF structure and a VC-PGA with binary-weighted power consumption. Both circuits are designed and fabricated in a standard 65 nm CMOS technology. As demonstrated, the

presented approach is particularly suitable for a reconfigurable ABB design with improved energy efficiency. It therefore can be concluded that the presented system approach not only has the potential to be used for software-defined radios, but also can be considered as a solution for many applications which require low cost and high energy efficiency, such as 5G communication, WSNs and IoTs. In addition, the proposed design technique of a PGA may be used to enhance the circuit's yield, as the gain step of the PGA can be fine-tuned after fabrication, which is not the case for conventional op-amp based designs.

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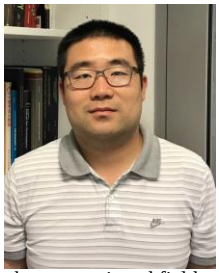

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He has secured over S$30M of research funding from various funding agencies and the industry in the past 5 years. He is a Series Editor of 5 books on "Emerging Technologies in Circuits and Systems", author of 9 books, 7 book chapters and has over 600 top-tier refereed journal and conference papers in his area of research and holds 38 patents. Professor Yeo is a Member of Board of Advisors of the Singapore Semiconductor Industry Association and a world-renowned authority on low-power RF/mm-wave IC design and a recognized expert in CMOS technology. He is an IEEE fellow for his contributions to low-power integrated circuit design.

Prof Yeo has supervised or trained more than 100 researchers and postgraduate students, many of whom are successful leaders in the industry and academia. He gave several keynotes and invited talks at various scientific conferences, meetings, workshops and seminars. Furthermore, he served in the editorial board of IEEE Transactions on Microwave Theory and Techniques and was one of the Guest Editors of Journal of Circuits, Systems and Computers on Green Integrated Circuits and Systems from 2008 to 2010 and on Energy and Variability Aware Circuits and Systems from 2011 to 2013. He also holds/held key positions in many international conferences as Advisor, General Chair, Co-General Chair and Technical Chair. In 2009, he was conferred the Public Administration Medal (Bronze) on National Day by the President of the Republic of Singapore and the Distinguished Nanyang Alumni Award by NTU for his outstanding contributions to the university and society.