Design and Implementation of a Re-configurable Wideband Radio Frequency Spectrum Analyser with Image Rejection in the Digital Domain

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***Abstract*— Most existing radio frequency (RF) spectrum analysers use conventional super-heterodyne architecture to remove images associated with the down conversion of RF input frequency to some intermediate frequency (IF) for further processing, and their complexity increases as the frequency range of interest is extended. This paper describes a novel digital system architecture for spectrum analysers based on quadrature down conversion. Quadrature down conversion architectures where image responses are inherently rejected are normally used to analyse a single frequency or a very narrow frequency spectrum. This paper proposes using quadrature architecture in an ultra-wideband spectrum analysis application. A wideband spectrum analyser receiver with compensation for gain and phase imbalances in the RF input range, as well as compensation for gain and phase imbalances within the IF passband complete with resolution bandwidth (RBW) filtering, video bandwidth (VBW) filtering and amplitude detection is implemented in a low-cost field programmable gate arrays (FPGA). The proposed method still achieves the desired image rejection performance specification, is power-efficient and significantly simplifies the RF front-end hardware in comparison to state of the art methods.**

***Index Terms*— Spectrum Analyser; Re-configurable; wideband; resolution bandwidth; FPGA**

I. Introduction

Radio frequency (RF) spectrum analyser is one of the most important instruments used in test and measurement applications. It measures the magnitude of a signal of any frequency within the full frequency range of the instrument. The continued high demand of portable spectrum analysers with decent RF performance for applications such as testing in cellular systems, radar installations, analysis in satellite stations and even for general research and development makes it a topic of high interest. The architectures of most existing spectrum analysers are entirely analogue up to and including the detectors [1, 2]. Recent efforts to extend the frequency range of interest, especially of portable spectrum analysers have found it to be overly complex in analogue terms [3, 4]. With the existing super-heterodyne architectures, it requires the Local Oscillators (LOs) to generate frequencies much higher than the frequency range of interest and involves designing remarkably complex, high frequency transistor-based Voltage Controlled Oscillators (VCOs) [5]. Additionally, power consumption increases with complexity in the hardware architecture which is not desirable in a hand-held instrument. Therefore, the possibility of using alternate architectures using digital techniques is considered in this paper.

The main challenge presented in the development of the spectrum analyser is to remove images associated with the down conversion of RF input frequency to some intermediate frequency for further processing [6]. In a super-heterodyne architecture, the first intermediate frequency (IF) is chosen to be higher than the frequency range of interest [7]. This ensures that the image is also greater than the frequency range and greater than the chosen IF as well. A fixed low-pass filter is then placed in front of the mixer to remove this image. This filter also rejects the effect of any harmonics of the LO frequency. But this architecture becomes unfeasible as the frequency range of interest is extended. To ease the LO requirement for an extended frequency range, the first IF is chosen to fall in the frequency range of interest. Removing image responses in this case is extremely difficult using analogue tuneable low pass filters. The problem of IF feedthrough when the IF falls in the frequency range of interest also needs to be accounted for.

Quadrature down-conversion architectures where image responses are inherently rejected are normally used to analyse a single frequency or a very narrow frequency spectrum [7]. However, gain and phase imbalances in the I (In-phase) and Q (Quadrature) channels means that the image rejection is severely limited [8]. This is improved by applying compensation which is tailored for the narrow frequency band. Most literature reviewed were found to be in the context of receivers for signals with digital modulation such as digital mobile communications, wireless applications, and digital television. In all these applications, a long time is spent on a single frequency, unlike in a spectrum analyser. Although design considerations have been made in the past to enhance the image rejection over a wide bandwidth, the image rejection ratio achieved was well below than what is required for spectrum analysis [9]. This paper proposes using quadrature architecture in an ultra-wideband spectrum analysis application. For a spectrum analyser, the ultra-wide frequency range is

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divided into thousands of sub-bands of unequal widths. Each sub-band has its own parameters for gain and phase mismatch. These parameters are stored in a Random-Access Memory (RAM) in the field programmable gate arrays (FPGA) and periodically updated to account for variations in the gain and phase imbalances due to temperature.

Several algorithms exist for the compensation of gain and phase imbalances in a quadrature architecture. In [10] an estimated correlation method carried out to compensate for gain and phase imbalances was proposed. However, their method only works if the errors are small in the first place and will not converge if they are large.

Instead of estimating the imbalances, the imbalances could be computed directly. This paper proposes a correlation method of calculating the compensation parameters directly. For this novel approach to work, the input waveform must be periodic over the number of samples over which correlations are performed. This is achievable in a system where gain and phase correction parameters are calculated using a test signal whereby the frequency of the test signal could be adjusted to suit the calculation method. The test signal or the internal calibration signal source is introduced in the RF chain close to the input and this signal is switched in instead of the real input when imbalance calculation is performed. The calibration signal source is a fractional *N* frequency synthesizer where the frequency of the generated signal is precisely defined in the synthesizer. System noise also has a significant effect on the accuracy of the calculated results. However, simulation results show that the accuracy of the results could be maintained if noise in the system is controlled and by increasing the number of samples used for the calculation to account for the noise present in the system. The noise in the system can be controlled by providing a clean, adequately filtered supply to power the amplifiers, designing the amplifiers such that they have very high-power supply rejection ratio, planning the gain of the amplifiers to achieve minimum noise injection, choosing a calibration signal source and the local oscillator signal sources with decent phase noise performances, and providing a clean jitter-free clock input to the analogue to digital converter. This paper also proposes gain and phase imbalance computation using Weaver baseband [11] architecture in a wideband spectrum analyser application. The proposed solution is different from the approaches in [12-14] where the signal is mixed down to low IF instead of baseband. The proposed solution is also different from [15] where only two low-pass filters are used instead of four to save hardware resources. However, this means that their solution only works if the errors are small in the first place.

Finally, this paper proposes novel solution for compensation of gain and phase imbalances within the IF passband and therefore presents a complete solution for swept spectrum analysis. It should be declared that this paper reuses some content from thesis [6] with permission.

Section II of this paper provides the system model and methodology of the proposed scheme. The section briefly explains the low IF based digital spectrum analyser architectures, IQ image reject receiver architecture, IQ imbalance compensation using digital techniques and IQ imbalance compensation within the IF passband. Section III presents the simulation of direct imbalance computation method, gain and phase imbalance correction, demonstration of the effect of noise on the correlation method of imbalance compensation, simulation of direct imbalance computation using Weaver base-band architecture and simulation of gain and phase imbalance variations and corrections within the IF passband. Section IV details the new design analysis of digital spectrum analyser architecture with image rejection using Weaver base-band architecture and FPGA design, simulation, and synthesis of the new method. Section V concludes the research and possible future work is discussed.

II. Digital Signal Processing Based Radio Frequency Spectrum Analysis

The system model of the proposed analogue input section is shown in Figure 1. For the lower frequency range, the frequency is mixed to a higher first IF, followed by quadrature down conversion to a low final IF. This means that image spurious associated with the high IF can be easily removed using a fixed low-pass filter in front of the first mixer. For the higher range, quadrature down conversion is directly used. Images associated with quadrature down conversion is removed in the digital domain. This division of frequencies ensures that IF feed through is avoided. Although, the front-end is designed for an input frequency range spanning from 10 MHz to 6 GHz, the design is modular and could be scaled up appropriately to cover a wider frequency span.

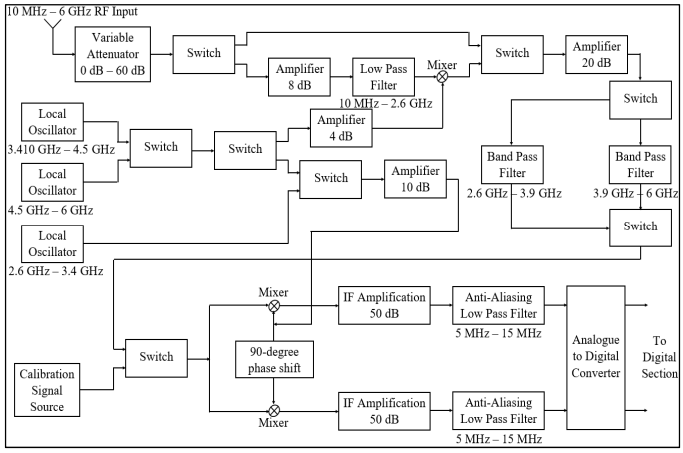


Figure 1. Analogue section of the RF architecture.

A. IQ imbalance and compensation

In a conventional quadrature receiver shown in Figure 2, the RF input is multiplied by two sinusoidal LO input signals with equal amplitude and with a 90-degree phase difference.

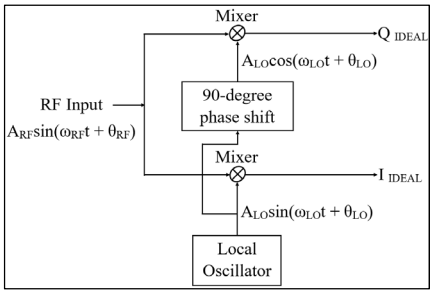


Figure 2. Quadrature frequency down conversion model.

Let the RF input be defined as $A_{RF}sin(\omega_{RF}t+\theta_{RF})$, where A is the amplitude, ω is the frequency and θ is the initial phase. Similarly, the two sinusoidal LO input signals can be defined as $A_{LO}sin(\omega_{LO}t+\theta_{LO})$ and $A_{LO}cos(\omega_{LO}t+\theta_{LO})$, respectively. This is only true in ideal situation, there always exist an imbalance in the amplitudes and phase of the two LO input signals. Let the outputs of the mixers be defined as I_{IDEAL} and Q_{IDEAL} respectively. Therefore,

$$I_{IDEAL} = A_{RF}sin(\omega_{RF}t+\theta_{RF})\times A_{LO}sin(\omega_{LO}t+\theta_{LO}) \quad (1)$$

$$Q_{IDEAL} = A_{RF}sin(\omega_{RF}t+\theta_{RF})\times A_{LO}cos(\omega_{LO}t+\theta_{LO}) \quad (2)$$

Let α be the amplitude imbalance and ξ be the phase imbalance in the LO input signals. Therefore, one of the LO signals will now be $A_{LO}(1+\alpha)cos(\omega_{LO}t+\theta_{LO}+\xi)$. The Q channel output will change to

$$Q_{REAL} = A_{RF}sin(\omega_{RF}t+\theta_{RF})\times A_{LO}(1+\alpha)cos(\omega_{LO}t+\theta_{LO}+\xi) \quad (3)$$

In this model, imbalances are placed in the Q channel as shown in Figure 3. Any compensation applied to this model will try to match the gain and phase of Q channel to that of the I channel.

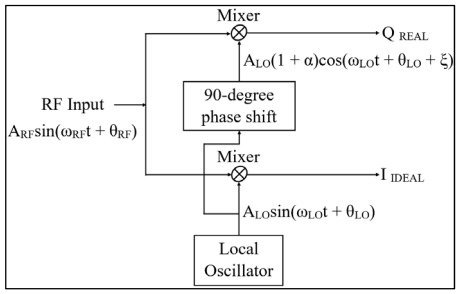


Figure 3. Quadrature frequency down conversion model with all gain/phase imbalances placed in the Q channel.

As shown in Figure 4, gain and phase imbalances in the Q channel could be compensated by multiplying Q channel with $1/cos(\xi)(1+\alpha)$ and I channel with $sin(\xi)/cos(\xi)$ respectively and adding them together.

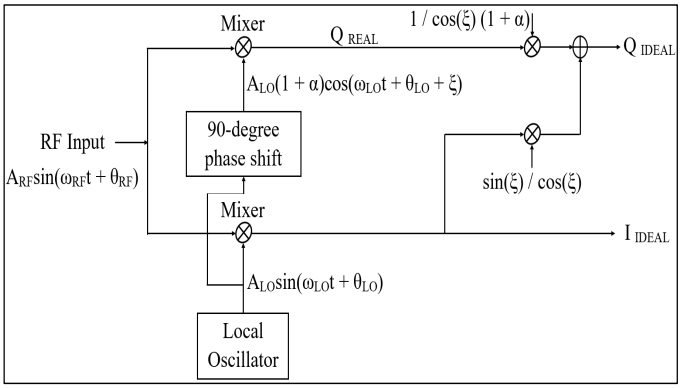


Figure 4. Compensation model for gain and phase imbalances.

B. Image rejection

Once the errors in the I and Q channels are compensated, image rejection is achieved by shifting one of the channels by 90 degrees and adding them together. This is in effect the Hartley architecture [16]. The 90-degree phase shift would need to be perfectly accurate and frequency independent. This is quite difficult to achieve in the digital domain. Another possible solution is to use a second mixing stage to achieve the 90-degree phase shift. The intermediate frequency is further down converted to a lower IF (or down to baseband). This is described as Weaver architecture [11], shown in Figure 5. There are several advantages of using Weaver architecture over Hartley in a FPGA implementation. The down conversion is achieved by using multipliers which are readily available in FPGAs. The digital filters would also make use of the embedded multipliers and additions in the filters could be performed using logic resources.

The wanted I and Q signal outputs from the Weaver architecture could be converted down to base-band using a Digital Down Conversion (DDC) architecture for further processing [17]. Resolution band width filters can then be implemented using low-pass filters. However, it is also possible to convert the I and Q signals directly down to baseband in the Weaver architecture itself. Doing this has several advantages. The two low-pass filters before the mixers are no longer required as there is no second image. The four low-pass filters after the mixers also functions as RBW filters and therefore there is no need for any additional filtering thereby reducing design complexity. Weaver base-band architecture is shown in Figure 6.

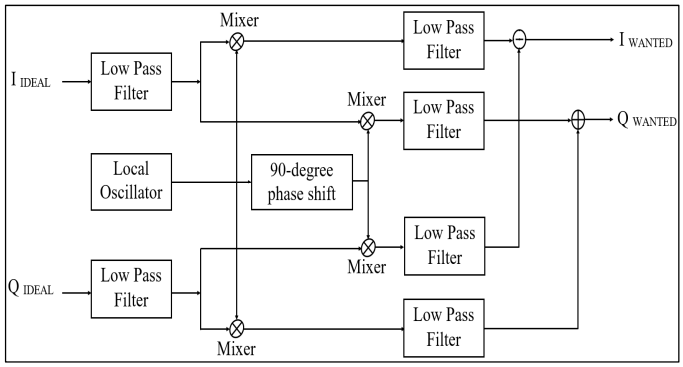


Figure 5. Block diagram of the Weaver architecture.

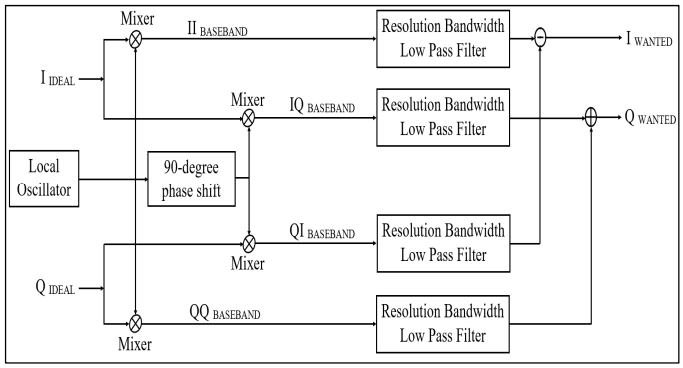


Figure 6. Block diagram of the Weaver base-band architecture.

C. Imbalance computation by correlation method

In this method, the compensation parameters, $1/cos(\xi)(1+\alpha)$ and $sin(\xi)/cos(\xi)$ would be calculated exploring the correlation properties in the I and Q channels.

From equation (3), it is known that Q_{REAL} is equal to $(1+\alpha)(Q_{IDEAL}cos(\xi) - I_{IDEAL}sin(\xi))$. If autocorrelation is performed on both sides of the equation, the equation changes to:

$$corr(\overrightarrow{Q_{REAL}},\overrightarrow{Q_{REAL}}) = corr(\overrightarrow{(1+\alpha)(Q_{IDEAL}cos(\xi) - I_{IDEAL}sin(\xi))}, \overrightarrow{(1+\alpha)(Q_{IDEAL}cos(\xi) - I_{IDEAL}sin(\xi))}) \quad (4)$$

$$corr(\overrightarrow{Q_{REAL}},\overrightarrow{Q_{REAL}}) = (1+\alpha)^2(corr(\overrightarrow{Q_{IDEAL}},\overrightarrow{Q_{IDEAL}})cos^2(\xi) + corr(\overrightarrow{I_{IDEAL}},\overrightarrow{I_{IDEAL}})\sin^2(\xi) - 2corr(\overrightarrow{I_{IDEAL}},\overrightarrow{Q_{IDEAL}})sin(\xi)\cos(\xi)) \quad (5)$$

I and Q are equal and orthogonal signals. Therefore, cross-correlation of I_{IDEAL} and Q_{IDEAL} is equal to zero and autocorrelation of I_{IDEAL} is equal to the autocorrelation of Q_{IDEAL} and is equal to the total power in each of the channel. $corr(\overrightarrow{Q_{IDEAL}},\overrightarrow{Q_{IDEAL}})$ is replaced by $corr(\overrightarrow{I_{IDEAL}},\overrightarrow{I_{IDEAL}})$ and $corr(\overrightarrow{I_{IDEAL}},\overrightarrow{Q_{IDEAL}})$ is replaced by 0.

$$corr(\overrightarrow{Q_{REAL}},\overrightarrow{Q_{REAL}}) = (1+\alpha)^2(corr(\overrightarrow{I_{IDEAL}},\overrightarrow{I_{IDEAL}})(cos^2(\xi)+\sin^2(\xi))) \quad (6)$$

From trigonometric identities, it is known that

$$cos^2(\xi) + sin^2(\xi) = 1 \quad (7)$$

Therefore,

$$corr(\overrightarrow{Q_{REAL}},\overrightarrow{Q_{REAL}}) = (1+\alpha)^2 corr(\overrightarrow{I_{IDEAL}},\overrightarrow{I_{IDEAL}}) \quad (8)$$

$$(1+\alpha) = \sqrt{\frac{corr(\overrightarrow{Q_{REAL}},\overrightarrow{Q_{REAL}})}{corr(\overrightarrow{I_{IDEAL}},\overrightarrow{I_{IDEAL}})}} \quad (9)$$

If both sides of equation (3) are cross correlated with I_{IDEAL}, the equation changes to:

$$corr(\overrightarrow{I_{IDEAL}},\overrightarrow{Q_{REAL}}) = corr(\overrightarrow{I_{IDEAL}},\overrightarrow{(1+\alpha)\{Q_{IDEAL}cos(\xi) - I_{IDEAL}sin(\xi)\}}) \quad (10)$$

$$corr(\overrightarrow{I_{IDEAL}},\overrightarrow{Q_{REAL}}) = (1+\alpha)cos(\xi)corr(\overrightarrow{I_{IDEAL}},\overrightarrow{Q_{IDEAL}}) - (1+\alpha)\sin(\xi)corr(\overrightarrow{I_{IDEAL}},\overrightarrow{I_{IDEAL}}) \quad (11)$$

Cross-correlation of I_{IDEAL} and Q_{IDEAL} is equal to zero. Therefore,

$$corr(\overrightarrow{I_{IDEAL}},\overrightarrow{Q_{REAL}}) = -(1+\alpha)\sin(\xi)corr(\overrightarrow{I_{IDEAL}},\overrightarrow{I_{IDEAL}}) \quad (12)$$

$$(1+\alpha)\sin(\xi) = \frac{-corr(\overrightarrow{I_{IDEAL}},\overrightarrow{Q_{REAL}})}{corr(\overrightarrow{I_{IDEAL}},\overrightarrow{I_{IDEAL}})} \quad (13)$$

Hence, equation (14) and (15) are proofed from equations (9) and (13).

D. Imbalance computation using Weaver base-band architecture

System noise has a significant effect on the accuracy of the calculated results using the correlation method of direct computation of gain and phase imbalances. The effect of noise can be minimised by averaging process. However, the number of samples that is needed would have to increase exponentially as the signal to noise ratio deteriorates. An alternative solution to calculate imbalances using Weaver base-band architecture is presented in this sub-section.

Using trigonometric identities, equations (1) and (3) can be written as follows:

$$I_{IDEAL} = \left(\frac{A_{RF}A_{LO}}{2}\right)(cos(\omega_{RF}t + \theta_{RF} - \omega_{LO}t - \theta_{LO}) - cos(\omega_{RF}t + \theta_{RF} + \omega_{LO}t + \theta_{LO})) \quad (16)$$

$$Q_{REAL} = \left(\frac{A_{RF}A_{LO}(1+\alpha)}{2}\right)(sin(\omega_{RF}t + \theta_{RF} + \omega_{LO}t + \theta_{LO} + \xi) + sin(\omega_{RF}t + \theta_{RF} - \omega_{LO}t - \theta_{LO} - \xi)) \quad (17)$$

The anti-alias filters before the Analogue to Digital Converter (ADC) in Figure 1 removes the sum frequency components. Therefore, the IQ signals in the digital domain are presented as:

$$I_{IDEAL} = \left(\frac{A_{RF}A_{LO}}{2}\right)cos(\omega_{RF}t + \theta_{RF} - \omega_{LO}t - \theta_{LO}) \quad (18)$$

$$Q_{REAL} = \left(\frac{A_{RF}A_{LO}(1+\alpha)}{2}\right)sin(\omega_{RF}t + \theta_{RF} - \omega_{LO}t - \theta_{LO} - \xi) \quad (19)$$

$$\frac{1}{cos(\xi)(1+\alpha)} = \frac{corr(\overrightarrow{Q_{REAL}},\overrightarrow{Q_{REAL}})}{\sqrt{corr(\overrightarrow{I_{IDEAL}},\overrightarrow{I_{IDEAL}})\times \mathrm{co}\,rr(\overrightarrow{Q_{REAL}},\overrightarrow{Q_{REAL}}) - \mathrm{corr}(\overrightarrow{I_{IDEAL}},\overrightarrow{Q_{REAL}})\times corr(\overrightarrow{I_{IDEAL}},\overrightarrow{Q_{REAL}})}} \quad (14)$$

$$\frac{\sin(\xi)}{cos(\xi)} = \frac{corr(\overrightarrow{I_{IDEAL}},\overrightarrow{Q_{REAL}})}{\sqrt{corr(\overrightarrow{I_{IDEAL}},\overrightarrow{I_{IDEAL}})\times \mathrm{co}\,rr(\overrightarrow{Q_{REAL}},\overrightarrow{Q_{REAL}}) - \mathrm{corr}(\overrightarrow{I_{IDEAL}},\overrightarrow{Q_{REAL}})\times corr(\overrightarrow{I_{IDEAL}},\overrightarrow{Q_{REAL}})}} \quad (15)$$

Let us define $(\omega_{RF} - \omega_{LO})$ as ω_{IF}, $(\theta_{RF} - \theta_{LO})$ as θ_{IF}, and $\left(\frac{A_{RF}A_{LO}}{2}\right)$ as A_{IF} respectively. Therefore, equations (18) and (19) can be written as:

$$I_{IDEAL} = A_{IF}cos(\omega_{IF}t + \theta_{IF}) \tag{20}$$

$$Q_{REAL} = A_{IF}(1+\alpha)sin(\omega_{IF}t + \theta_{IF} - \xi) \tag{21}$$

These input signals are mixed down to baseband in the four mixers shown in Figure 6 by multiplying them with internally generated orthogonal signals. These signals are generated using Direct Digital Synthesis (DDS) methods in the digital domain [18]. The outputs from the four mixers /multipliers are:

$$II = A_{IF}cos(\omega_{IF}t + \theta_{IF}) \times sin(\omega_{IF}t) \tag{22}$$

$$IQ = A_{IF}cos(\omega_{IF}t + \theta_{IF}) \times cos(\omega_{IF}t) \tag{23}$$

$$QI = A_{IF}(1+\alpha)sin(\omega_{IF}t + \theta_{IF} - \xi) \times sin(\omega_{IF}t) \tag{24}$$

$$QQ = A_{IF}(1+\alpha)sin(\omega_{IF}t + \theta_{IF} - \xi) \times cos(\omega_{IF}t) \tag{25}$$

Using trigonometric identities, equations (22), (23), (24) and (25) can be written as follows:

$$II = \frac{A_{IF}}{2}(sin(\omega_{IF}t + \theta_{IF} + \omega_{IF}t) + sin(\omega_{IF}t - \omega_{IF}t - \theta_{IF})) \tag{26}$$

$$IQ = \frac{A_{IF}}{2}(cos(\omega_{IF}t + \theta_{IF} + \omega_{IF}t) + cos(\omega_{IF}t + \theta_{IF} - \omega_{IF}t)) \tag{27}$$

$$QI = \frac{A_{IF}(1+\alpha)}{2}(cos(\omega_{IF}t + \theta_{IF} - \xi - \omega_{IF}t) - cos(\omega_{IF}t + \theta_{IF} - \xi + \omega_{IF}t)) \tag{28}$$

$$QQ = \frac{A_{IF}(1+\alpha)}{2}(sin(\omega_{IF}t + \theta_{IF} - \xi + \omega_{IF}t) + sin(\omega_{IF}t + \theta_{IF} - \xi - \omega_{IF}t)) \tag{29}$$

The low pass filters at the output of the multipliers removes the sum frequency components.

$$II_{LPF} = \frac{-A_{IF}}{2}sin(\theta_{IF}) \tag{30}$$

$$IQ_{LPF} = \frac{A_{IF}}{2}cos(\theta_{IF}) \tag{31}$$

$$QI_{LPF} = \frac{A_{IF}(1+\alpha)}{2}cos(\theta_{IF} - \xi) \tag{32}$$

$$QQ_{LPF} = \frac{A_{IF}(1+\alpha)}{2}sin(\theta_{IF} - \xi) \tag{33}$$

The amplitude and phase imbalance information are still retained in these four outputs. The aim is to calculate $1/cos(\xi)(1+\alpha)$ and $sin(\xi)/cos(\xi)$. Solving equations (30-33), it can be proved that:

$$\frac{1}{cos(\xi)(1+\alpha)} = \frac{-\left(\left(II_{LPF} \times II_{LPF}\right) + \left(IQ_{LPF} \times IQ_{LPF}\right)\right)}{\left(\left(IQ_{LPF} \times QI_{LPF}\right) - \left(II_{LPF} \times QQ_{LPF}\right)\right)} \tag{34}$$

and

$$\frac{sin(\xi)}{cos(\xi)} = \frac{\left(\left(II_{LPF} \times QI_{LPF}\right) + \left(IQ_{LPF} \times QQ_{LPF}\right)\right)}{\left(\left(IQ_{LPF} \times QI_{LPF}\right) - \left(II_{LPF} \times QQ_{LPF}\right)\right)} \tag{35}$$

The main advantage of using this algorithm is that the four mixer outputs are base-band signals and hence the low-pass filters can be implemented as very narrow filters. Therefore, noise can be filtered out and the compensation parameters can be calculated with great accuracy. Figure 7 is a block diagram representation of imbalance computation and correction in Weaver base-band architecture.

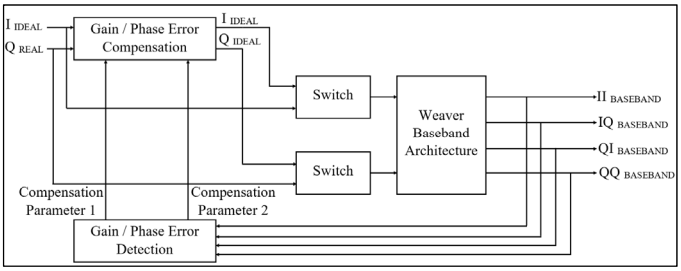


Figure 7. Imbalance computation method using Weaver base-band architecture.

E. IQ imbalance compensation within the IF passband

Any compensation method assumes that the differential phase error and / or differential gain error of the two anti-alias filters before the ADC is constant with frequency across the passband of the filters and well into the stopband. In practice it varies with IF frequency and compensation only achieve maximum image rejection at one point in the IF filter passband. Hence some type of algorithm is required to compensate for the variation of gain and phase error in the IF passband.

The use of digital Finite Impulse Response (FIR) filters to compensate for minor I/Q mismatch in direct-conversion receivers was proposed in [19]. A similar structure could be applied in a spectrum analyser application. The variation of gain and phase errors variation within the IF passband is only of concern for wider resolution bandwidths where the noise floor is quite high (the image only needs to be rejected down to the noise floor). A first order FIR filter compensation should be adequate.

The aim is to make the gain and phase imbalance at all frequencies across the IF passband to be equal to the gain and phase imbalance at IF. The gain and phase imbalance are measured at equally spaced frequencies across the IF passband. This is then normalised with respect to the gain and phase imbalance at IF and then used to compute inverse Fast Fourier Transform (FFT) which provides the coefficients of the FIR filter.

Using this method, the frequency response over the entire IF passband is deliberated by performing interpolation of the sampled frequency response. The ripple error in between the

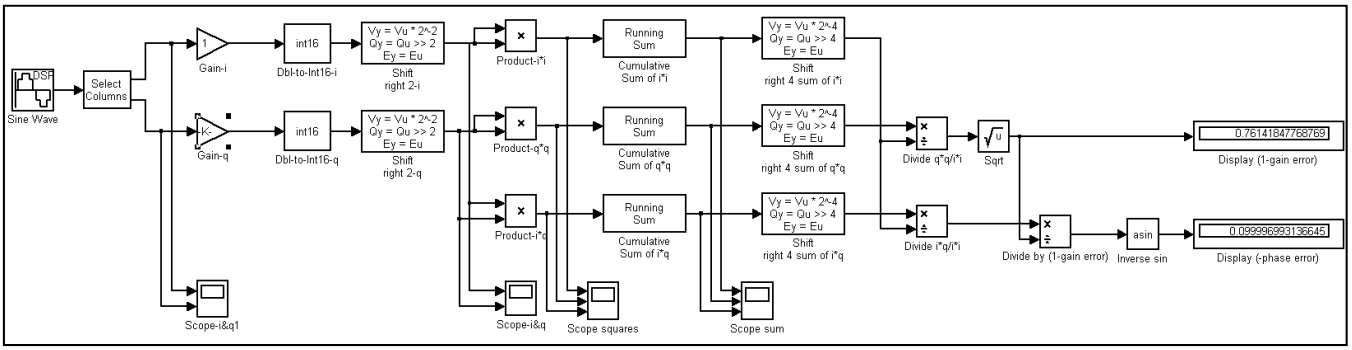


Figure 8. Simulation of imbalance computation by correlation method.

sampled frequencies is smoothed out by using window functions.

III. Simulation and Performance Analysis of the Proposed Methods

A. Simulation of imbalance computation by correlation method

The auto correlation of I is equal to $\left(I_1 \times I_1 + I_2 \times I_2 + ...I_N \times I_N\right)/N$ and the cross-correlation of I and Q is equal to $\left(I_1 \times Q_1 + I_2 \times Q_2 + ...I_N \times Q_N\right)/N$ where N is the number of samples. For the equations derived in the previous section to be true, the cross correlation of the ideal I and Q channels should be equal to zero (orthogonal property of I and Q) and the auto correlation of the ideal I channel should be equal to the auto correlation of the ideal Q channel (and should be equal to the total power in each channel). These conditions are only satisfied when the numbers of samples used to calculate the correlations represent exact number of complete waveform cycles of I and Q.

The error detection block modelled in Matlab Simulink is shown in Figure 8. The sampling rate is 100 MSa/s and the frequency of the calibration signal used for error calculation is equal to 18.75 MHz. The 'Sine wave' block provides the two calibration signals, which are separated by the 'Select Columns' block. A phase error of 0.1 radians and a gain error of 23.87 % were introduced between the two signals. The 'Dbl to Int16' and 'Shift right-2' blocks simulate the effects of ADC truncation to 14 bits. The 'Product', 'Cumulative sum' and 'Shift right-4' blocks calculate the correlations.

The outputs of the two 'Divider' blocks are equal to $(1+\alpha)^2$ and $-((1+\alpha)\times sin(\xi))$ respectively. The display blocks display (1-gain error) and (–phase error) in radians, respectively.

The calculated gain and phase errors as shown in Figure 8 were 23.858 % and -0.0999969 radians, respectively. A range of gain and phase errors were introduced in the I and Q signals. The accuracy of the computed errors was always better than 0.001 % gain and 0.000001 radians. This is 100 times better than what is required to achieve 60 dB of image rejection.

Obviously, this is only true if the calibration signal is ideal. The calibration signal will have some phase noise, harmonics of 18.75 MHz frequency and uncorrelated noise added to it. All this will introduce errors.

The calibration signal source used in this design was MAX2870 [20], an ultra-wideband, phase-locked loop (PLL)

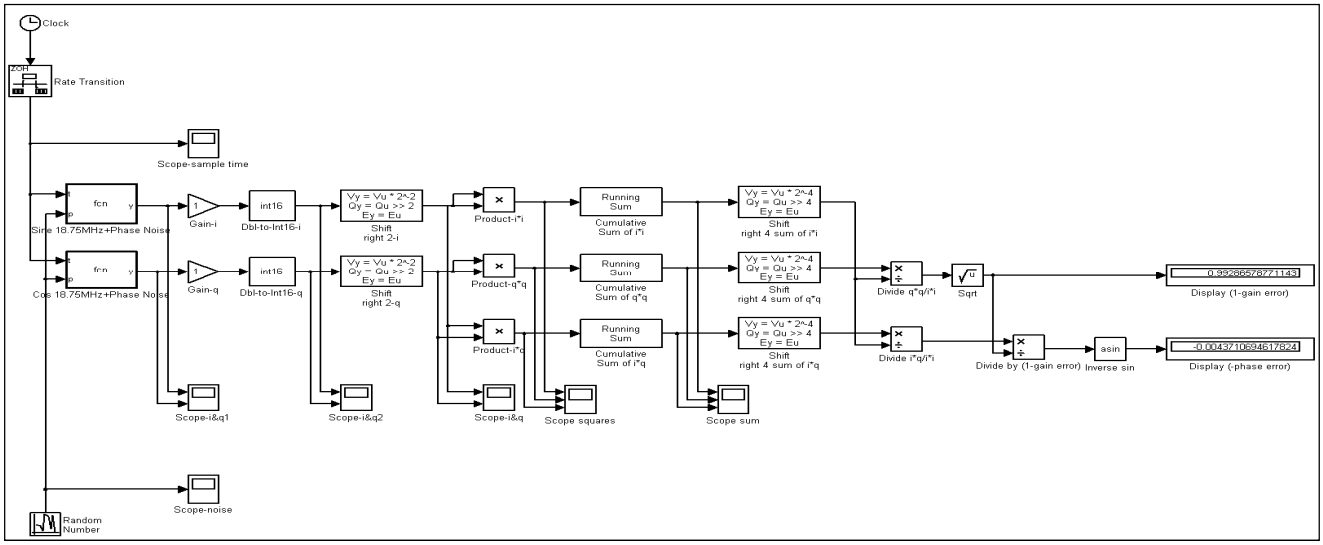


Figure 9. Simulation of error detection block with phase noise

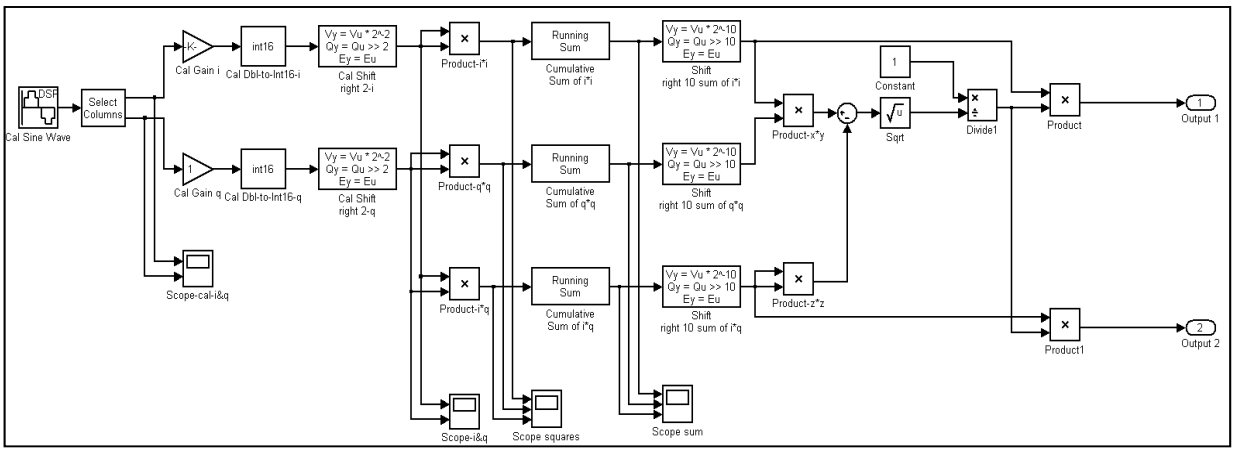


Figure 10. Error detection block with multiplying factors as output

with integrated VCOs. The phase noise performance of the device can be found in Table 1.

Table 1. Phase noise performance of calibration signal source [20].

VCO Phase Noise (measured open loop)	**Centre frequency 3000 MHz**	10 kHz offset	-83.5 dBc/Hz
		100 kHz offset	-111 dBc/Hz
		1 MHz offset	-136 dBc/Hz
		5 MHz offset	-149 dBc/Hz
	Centre frequency 4500 MHz	10 kHz offset	-75 dBc/Hz
		100 kHz offset	-104 dBc/Hz
		1 MHz offset	-130 dBc/Hz
		5 MHz offset	-145.5 dBc/Hz
	Centre frequency 6000 MHz	10 kHz offset	-71.5 dBc/Hz
		100 kHz offset	-100.5 dBc/Hz
		1 MHz offset	-128 dBc/Hz
		5 MHz offset	-143.5 dBc/Hz

To simulate the effects of phase noise and uncorrelated noise, the error detection block was slightly modified as shown in Figure 9. The 'sine wave' and the column select' block were replaced by two functional blocks. The outputs of these functional blocks were $Asin(\omega t)$ and $Acos(\omega t)$ respectively. Phase noise was simulated by changing the functions to $Asin(\omega t + \xi)$ and $Acos(\omega t + \xi)$. ξ is the phase error that will originate from a noise source with zero mean and standard deviation equal to the RMS phase error in radians.

For RMS phase error of 0.06321 radians, the error in the gain calculation was 0.71341 % and error in the phase calculation was 0.004371 radians. These errors will deteriorate the image rejection to 47.6 dB.

The calculation was then carried over 1024 samples representing exactly 192 cycles of the I and Q waveforms. The 'Shift right' block now shifted the inputs by 10 bits. The error in the gain calculation reduced to 0.0569023 % and error in the phase calculation reduced to 0.00037917 radians. Therefore, it was concluded that the effect of phase noise can be minimised by averaging the gain and phase error calculation over many waveform cycles.

For RMS phase error of 0.00511534 radians, the error in the gain calculation was further reduced to 0.026622 % and error in the phase calculation was further reduced to 0.00002435 radians. From this observation, it was concluded that there is some advantage in keeping the phase noise as low as possible.

The effect of uncorrelated noise on the error detection block is simulated next. The outputs of the functional blocks in Figure 9 were changed to $(Asin(\omega t) + N)$ and $(Acos(\omega t) + N)$ respectively. 'N' is random noise with maximum amplitude set to 50 dB below the amplitude of the I and Q signals. The

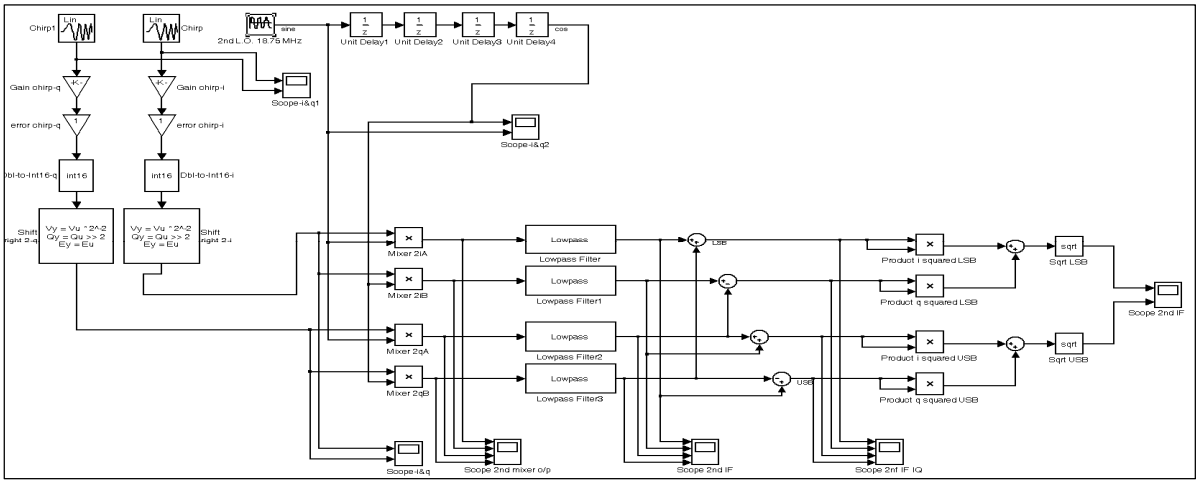


Figure 11. Simulation of Weaver base-band architecture

simulation is carried over 1024 samples. The error in the gain calculation was 0.02161% and error in the phase calculation was 0.0002123 radians. Hence, effect of uncorrelated noise is also minimised when averaging of gain and phase error calculation is performed.

The division and square root operations shown in the error detection block are there to calculate and display gain and phase errors. These operations do not need to be performed in the actual hardware implementation. The main aim is to calculate the multiplying factors $1/cos(\xi)(1+\alpha)$ and $sin(\xi)/cos(\xi)$. It was proved in the previous section that $1/cos(\xi)(1+\alpha) = x/\sqrt{(xy-zz)}$ and $sin(\xi)/cos(\xi) = z/\sqrt{(xy-zz)}$, where x, y and z are the three correlation outputs, $corr(\overrightarrow{Q_{REAL}}, \overrightarrow{Q_{REAL}})$, $corr(\overrightarrow{I_{IDEAL}}, \overrightarrow{I_{IDEAL}})$ and $corr(\overrightarrow{I_{IDEAL}}, \overrightarrow{Q_{REAL}})$ respectively. Therefore, subtraction, inverse square-root and multiplication (or subtraction, square root and division) operations are needed to be implemented in hardware to calculate the multiplying factors from the correlation outputs. The actual outputs from the error detection block are shown in Figure 10.

For signal to noise ratio of 50 dB, averaging 1024 samples was enough to achieve more than 60 dB of image rejection. However, it was observed that if the signal to noise ratio is 36.1 dB, averaging 1024 samples will achieve 54.2 dB of image rejection, averaging 4096 samples will achieve 56.68 dB of image rejection and averaging 65536 samples will achieve 57.43 dB of image rejection. From this observation, it was concluded that as signal to noise ratio deteriorates, averaging will have to increase exponentially to achieve the desired image rejection. In a spectrum analyser application where this computation process must be repeated for many thousands of sub-bands and then repeated periodically to account for temperature drifts, averaging the calculation over large number of samples will make the computation time unacceptably long. Therefore, it is imperative to keep the signal to noise ratio as high as possible.

B. Simulation of Weaver base-band architecture

Simulink model of the Weaver base-band architecture is shown in Figure 11. The 18.75 MHz In-phase and Quadrature inputs are mixed directly down to baseband with 18.75 MHz In-phase and Quadrature inputs from the local oscillator. The cut-off frequency of the anti-alias filter for 18.75 MHz IF and 100 MHz sampling rate would approximately be equal to 40 MHz. A chirp signal source is used to simulate this effect in the simulation. The frequency is swept from 1 MHz to 41 MHz in 400 us.

The LO frequency is equal to 3 Fs / 16 where Fs is the sampling rate (100 MHz). The signal can then be simply generated by repeating the sequence [0, 0.9239, 0.7071, -0.3827, -1, -0.3827, 0.7071, 0.9239, 0, -0.9239, -0.7071, 0.3827, 1, 0.3827, -0.7071 and -0.9239]. The 90-degree phase shifted version is [-1, -0.3827, 0.7071, 0.9239, 0, -0.9239, -0.7071, 0.3827, 1, 0.3827, -0.7071, -0.9239, 0 0.9239 0.7071 and -0.3827] (original sequence delayed by four clock cycles).

The four low-pass filters are narrow-band RBW filters. Magnitude response of the low-pass filter is shown in Figure 12.

Amplitude detection is performed on the Upper Side Band (USB) and Lower Side Band (LSB) signals. The wanted sideband is passed and the unwanted sideband is attenuated as shown in Figure 13.

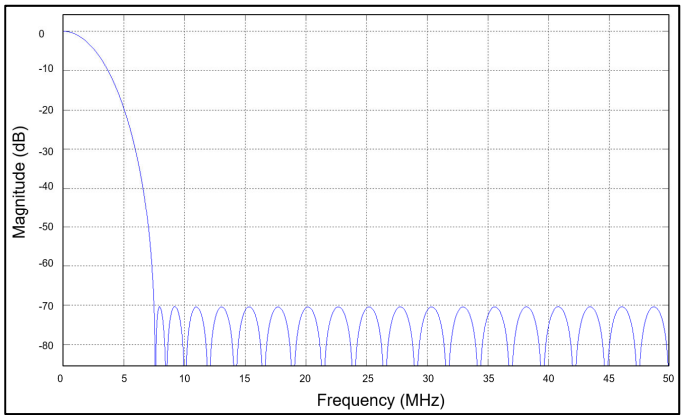


Figure 12. Magnitude response of the resolution bandwidth filters

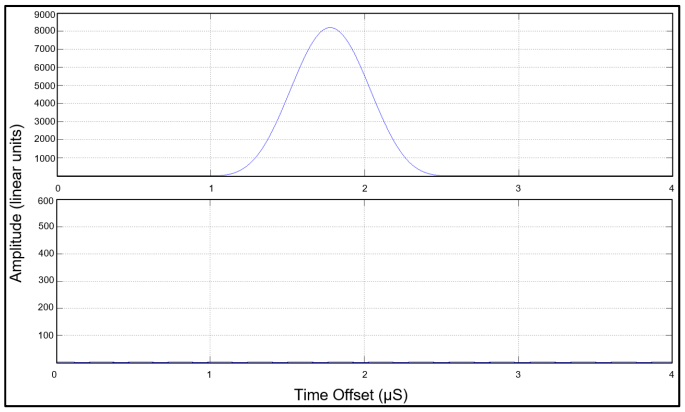


Figure 13. Wanted and image outputs.

C. Simulation of imbalance computation using Weaver base-band architecture

It has been proved that the gain and phase imbalance compensation parameters could be calculated using equations (34) and (35). This is verified in the simulation shown in Figure 14.

A gain imbalance of -0.2 % and phase imbalance of 22.5 degrees was introduced in one of the channels of the 18.75 MHz IF. The measured imbalance compensation parameters from the simulation were 1.39864 and 0.414952 respectively which closely matches the theoretical result (1.35299 and 0.414213).

D. Simulation of IQ imbalance compensation within the IF passband

To calculate the filter coefficients of the FIR compensation filter, the gain and phase imbalance across the IF passband is measured. The measured results are shown in Table 2. The gain and phase imbalance are only measured up to half the clock frequency and for the other half the readings are duplicated to form a conjugate symmetric.

The gain and phase imbalance are then normalised with respect to the gain and phase imbalance at the IF frequency (the filter should provide no compensation at IF frequency as the compensation that is applied at this frequency is correct).

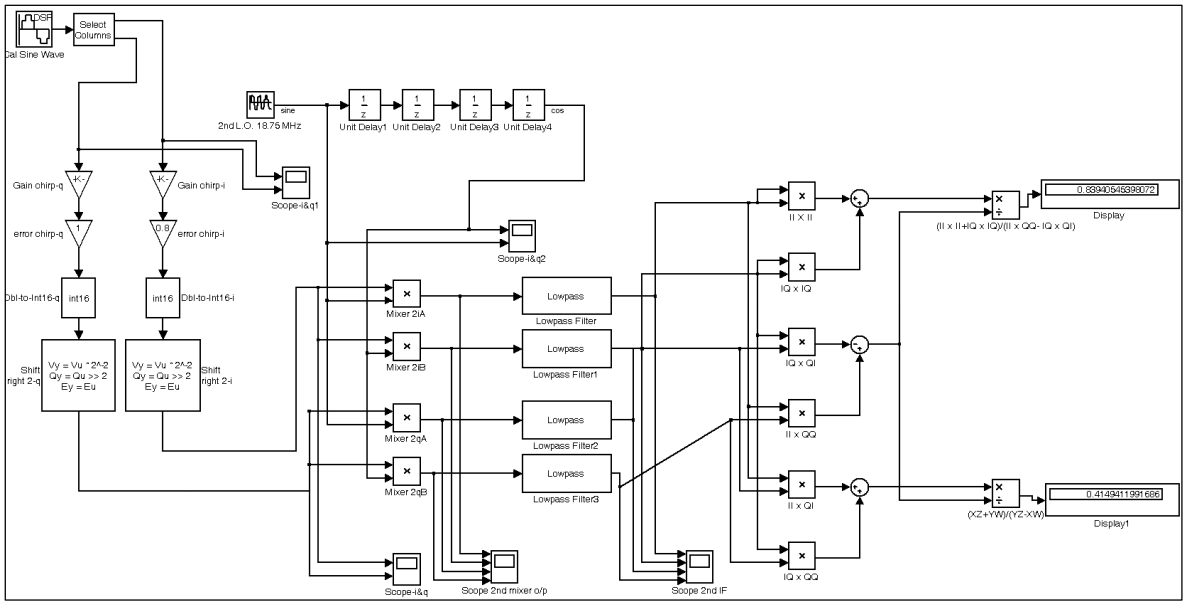


Figure 14. Simulation of imbalance computation using Weaver base-band architecture.

If α is the normalised gain and θ is the normalised phase at a given frequency, then the input to the inverse FFT for that frequency is $Xreal + jYreal$ where

$$Xreal = \sqrt{\frac{\alpha^2}{1 + \tan^2\theta}} \tag{36}$$

and

$$Yreal = Xreal \times tan(\theta) \tag{37}$$

Inverse FFT is calculated using the 'ifft' function in Matlab. The output of the inverse FFT is shifted to remove the sharp edges and then used as coefficients of the FIR filter defined in Matlab. A window function such as Blackman-Harris window could be used for further smoothing of the response of the filter.

Table 2. Measured gain and phase imbalance across IF passband

Gain Imbalance (ratio)	Phase Imbalance (radians)	Normalised Gain	Normalised Phase	Real	Imaginary
-1.1493	-0.2718	1.0000	0.0000	1.0000	0.0000
-1.0879	-0.2089	1.0564	-0.0629	1.0543	-0.0664
-1.1076	-0.1823	1.0376	-0.0895	1.0335	-0.0927
-1.1628	-0.2017	0.9884	-0.0701	0.9860	-0.0692
-1.1493	-0.2718	1.0000	0.0000	1.0000	0.0000
-1.0724	-0.2763	1.0717	0.0045	1.0717	0.0048
-1.0567	-0.2329	1.0876	-0.0389	1.0868	-0.0423
-1.0718	-0.2753	1.0723	0.0035	1.0723	0.0038
-1.1493	-0.2718	1.0000	0.0000	1.0000	0.0000
-1.0718	-0.2753	1.0723	0.0035	1.0723	-0.0038
-1.0567	-0.2329	1.0876	-0.0389	1.0868	+0.0423
-1.0724	-0.2763	1.0717	0.0045	1.0717	-0.0048
-1.1493	-0.2718	1.0000	0.0000	1.0000	-0.0000
-1.1628	-0.2017	0.9884	-0.0701	0.9860	0.0692
-1.1076	-0.1823	1.0376	-0.0895	1.0335	0.0927
-1.0879	-0.2089	1.0564	-0.0629	1.0543	0.0664

The magnitude and phase response of the FIR filter are shown in Figure 15 and Figure 16, respectively.

The measured gain and phase imbalance at different frequencies matches the gain and phase imbalance compensation for the same frequencies provided by the filter.

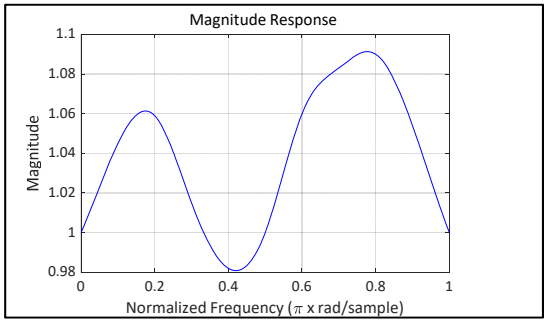


Figure 15. Magnitude response of the FIR filter

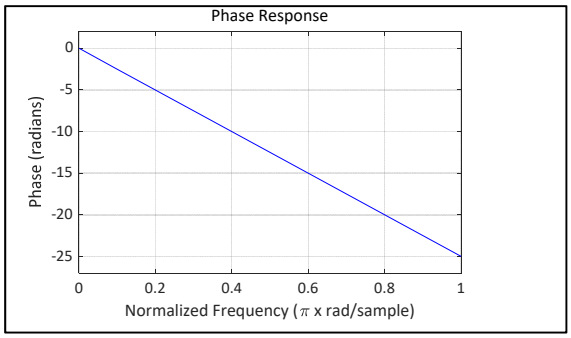


Figure 16. Phase response of the FIR filter

IV. Spectrum Analyser – FPGA Design, Synthesis and Results

Certain aspects of the RF architecture outlined in the previous sections such as the frequency limits for the lower and upper RF frequency bands and the final IF for further digital processing were revised. The sampling clock frequency was revised down to 40 MHz and the final IF going into the digital

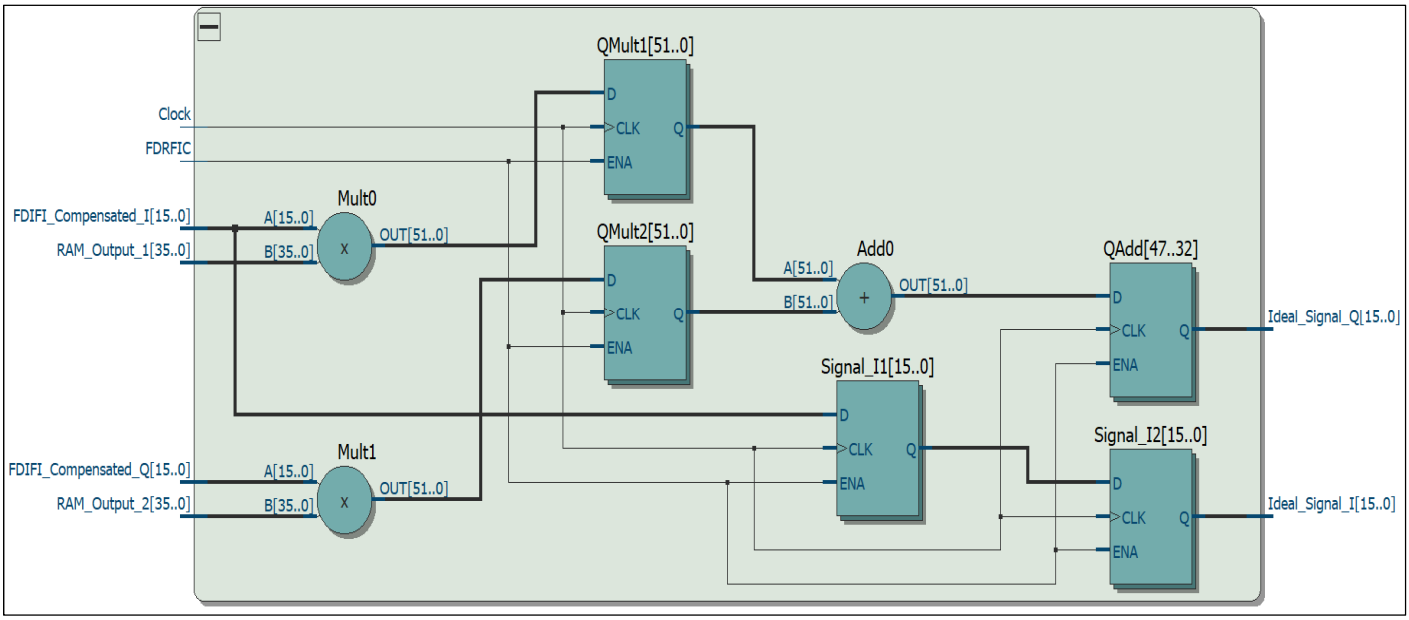


Figure 17. RTL view of RF imbalance compensation

section was chosen to be 10 MHz. The low-pass filters before the ADC removes the aliasing frequency. The filters attenuate frequencies above 28 MHz by more than 80 dB. A dual 16-bit ADC digitises the IQ signals for further processing in the digital domain.

It was initially assumed that a DSP processor would be used for the digital section of the design. However, it later became clear that it would be quite a challenge to implement all the parallel multipliers and filters in a DSP. FPGAs are characteristically ideal to perform multiple bits multiplication and addition operations at very high speed. The advantages of using FPGAs as opposed to ASICs are obvious. Designs implemented in a FPGA are less risky as they can easily be re-configured, and the design cycle is much smaller compared to other types of semiconductors. FPGAs configure themselves upon every power up and therefore, changes in the design can simply be made by downloading a new configuration into the device. Competing ASICs have fixed functionality that cannot be changed without great cost and time. Very high-speed integrated circuits Hardware Description Language (VHDL) was predominantly used to design the spectrum analyser which makes the design even more versatile as it can be easily moved to any new FPGA platform.

FPGAs from different manufacturers and of different families were evaluated. Cyclone IV series FPGAs from Intel Altera was identified to closely meet the requirements for the development of this product and therefore became an obvious choice for implementing the digital section. The FPGA used was Altera Cyclone IV EP4CE40F23C9L [21]. Choosing an Altera FPGA made the Altera Quartus II design software the most obvious choice for FPGA design. Altera also provides ModelSim, a comprehensive simulation and debug environment for FPGA designs. The Mega Function Wizard of Quartus II was used for some specific designs. Filter design software from Matlab were used to calculate the coefficients of the FIR filter used in the RBW and Video Band Width (VBW) filter section. Design analysis and implementations of spectrum analyser sub-systems will be discussed in this section.

A. FPGA design

The outputs from the chosen ADC are serial LVDS. The sampling frequency of the ADC is 40 MHz. The ADC is configured to output two bits at a time per channel at 320 MHz clock frequency. LVDS receiver is instantiated using Mega Function Wizard in Quartus to convert the serial LVDS data to parallel. The ADC also provides the clock to the FPGA. The input data are in offset binary format and are converted to two's complement data by inverting the MSBs of the data inputs.

To compensate for imbalance variation within the IF passband, a FIR filter is implemented in one of the channels. The FIR filter is realised in simple direct form. The number of coefficients in the filter is 32. Therefore, the filter requires 31 delay registers for each of it input bits, 31 additions, and 32 multiplications. The coefficients are set by the controlling processor and are stored in the FPGA RAM. The process of calculating the coefficients has been outlined in section II. The other channel is simply delayed by the number of cycles that the filter operation requires to maintain the phase relationship of the IQ signals.

The RF imbalance compensation block is shown in Figure 17. Channel Q is multiplied with $1/cos(\xi)(1+\alpha)$ and channel I is multiplied with $sin(\xi)/cos(\xi)$.

The outputs of the multipliers are added together to give Q_{IDEAL}. Channel I is simply delayed by the number of cycles required for the multiplication and addition process. The parameters $1/cos(\xi)(1+\alpha)$ and $sin(\xi)/cos(\xi)$ are computed by the Weaver base-band method for various frequency bands and stored in the FPGA RAM. The implementation of the computation process is explained later in this section.

The I and Q signals free from any imbalances are now converted down to baseband in the Weaver mixer stage. The 10

MHz In-phase and Quadrature local oscillator signals are generated in the FPGA using DDS techniques. The LO frequency is equal to Fs / 4 (10 MHz) where Fs is the sampling rate (40 MHz). Therefore, it was possible to generate the IQ LOs by simply repeating the four values [0, 1, 0, -1] and [1, 0, -1, 0] respectively. However, DDS techniques were used to allow for fine frequency tuning of the LO. The RF LO step resolution was limited to 1 MHz. The digital LOs provides fine frequency stepping resolution required for narrow band RBW filters. The lengths of the accumulators in the DDS were chosen to be 24 bits which gives 2 uHz resolution (for 40 MHz clock frequency). 12 MSBs of the accumulators were used to address the Sin and Cos ROM to generate the quadrature oscillator signals. The compensated I and Q inputs are multiplied by the I and Q LO outputs to provide four outputs from the Weaver mixers.

The four identical low-pass filters that follow the mixers remove the sum frequency components from the mixer outputs. These low-pass filters also function as resolution band-width filters. The requirement was to implement a wide range of RBW filters (300 Hz to 3 MHz in 1 – 3 steps). It is not possible to design a digital low-pass filter with cut-off frequency 150 Hz to get 300 Hz bandwidth running at 40 MHz. The resource requirement would have been prohibitively large. The above problem was resolved by using Cascaded Integrator-Comb (CIC) filters for decimations, followed by a FIR filter to provide the filter shape at each of the mixer outputs.

The low-pass FIR filter was designed with cut-off frequency 1.5 MHz for 3 MHz bandwidth at 40 MHz clock frequency. The other bandwidths were simply achieved by decimating the clock frequency using CIC filters [22]. A fifth order CIC filter of differential delay two was found to be enough for all the required decimation rates. The bit growth for the narrowest RBW is 72 bits. The mixer outputs are 16 bits long. Therefore, the additions and subtractions in the CIC filters are carried out in 88 bits. Owing to the large number of bits, the additions and subtractions operations are pipelined. The outputs of the CIC filters are truncated to 16 bits before being used as inputs to the FIR filters.

Table 3. RBW filters – decimation rate and CIC bit growth

RBW	Fpass (-3 dB)	Fstop (-60 dB)	Fs	Rate change	CIC bit growth
3 MHz	1.5 MHz	6.6 MHz	40 MHz	1	5
1 MHz	500 kHz	2.2 MHz	13.33 MHz	3	12.925
300 kHz	150 kHz	660 kHz	4 MHz	10	21.61
100 kHz	50 kHz	220 kHz	1.33 MHz	30	29.534
30 kHz	15 kHz	66 kHz	400 kHz	100	38.219
10 kHz	5 kHz	22 kHz	133.33 kHz	300	46.144
3 kHz	1.5 kHz	6.6 kHz	40 kHz	1000	54.829
1 kHz	500 Hz	2.2 kHz	13.33 kHz	3000	62.754
300 Hz	150 Hz	660 Hz	4 kHz	10000	71.439

Table 3 provides clock frequency, rate change and bit growth for various RBW filters used in the design. The FIR filters were designed using filter design software from Matlab. The filters were designed as direct form symmetric FIR filters. The length of the filter is 49. However only 25 coefficients are required as the filter is symmetric in nature. Each filter requires 49 delay registers for each of its input bits, 49 additions and 25 multiplications. A Gaussian filter shape with bandwidth selectivity 5:1 was selected. The coefficients of the filter were stored in the FPGA ROM.

The filtered I and Q signals are then added and subtracted together to get the wanted and unwanted sideband I and Q signals.

After resolution bandwidth filtering, the I and Q signals are squared and added together, and the square root of the results gives the amplitude of the signal. Dedicated multipliers embedded in the FPGA are used to perform squaring of I and Q signals. It was also possible to perform 32-bit addition in one 40 MHz clock cycle. Implementing square root function in FPGA is not straight forward and requires a lot of hardware. The I and Q signals are 16 bits long where the signal value only occupies 15 bits as the Weaver adder blocks halves the signal. The multiplication output is 32 bits long. The addition should add one more bit. However, as the signal value was only 15 bits to start with, there is no need to add a bit. The square root operation results in a 16-bit output. Square root implementation was based on non-restoring square root algorithm. Starting from the MSB, a count of one is subtracted from every pair of bits. The sign of the result determines the quotient bit and the remainder is added or subtracted to the next pair of bits based on the sign of the previous result. This process is repeated for every pair of bits down to LSB. The quotient is the desired result. For calculating the square root of a 32-bit number, 16 iterations are required which results in 32 pipeline stages.

A VBW filter is a low-pass filter that comes after amplitude detection that determines the bandwidth of the video signal. A similar structure to the RBW filter is used to implement the wide range of VBW filters as well. A fifth order CIC filter is used to provide all the required decimation rates and a FIR filter designed using Matlab filter design software is used to provide low-pass filtering.

The availability of I and Q base-band signals makes signal demodulation analysis quite straight forward. Amplitude modulation can be extracted from I and Q by taking the square root of the sum of the squares of I and Q. In other words, the output from the amplitude detector is the AM demodulated output as well. The instantaneous phase of the modulated signal is the result of the derivative of the arctangent of Q divided by I. Division requires a lot of hardware. Inverse operation is performed by storing the values of the inverse of a signal in a ROM. The rate of change of phase will result in FM modulating signal. The rate of change is simply the subtraction of two consecutive phase samples. If subtraction is performed after inverse operation, then two ROMs are required. This is not ideal. Therefore, instead of dividing Q by I, $\left(I_{current}Q_{next} - Q_{current}I_{next}\right)$ is divided by $\left(Q_{current}Q_{next} - I_{current}I_{next}\right)$ which gives tangent of the difference of two consecutive phase samples. The inverse will result in FM demodulated output. Dedicated embedded multipliers are used for the multiplication of $I_{current}$ and Q_{next}, $Q_{current}$ and I_{next}, $Q_{current}$ and Q_{next}, and $I_{current}$ and I_{next}. The results are 32-bit long. It was possible to perform 32-bit subtractions in one 40 MHz clock cycle. The ROM holds 1024 samples of the inverse function. Therefore, the divider needs to output 10-bit result which is used as an address to the ROM. Division of a 32-bit number, by a 32-bit number to output 10 bits requires a lot of

hardware. The divider implementation is based on non-restoring division algorithm. The denominator is subtracted from the numerator. The sign of the result determines the quotient bit and the denominator is added or subtracted to the result based on the sign of the previous result. This process is repeated for the number of desired bits in the result. For a 10-bit result, 10 pipeline stages are necessary.

The RF imbalance compensation block calculates the gain and phase imbalance compensation parameters used in the RF compensation block using equations (34) and (35). During the computation process, normal acquisition is halted, and an internal calibration signal is routed to the FPGA. The input level of the calibration signal is very close to the maximum input amplitude to the ADC to achieve maximum image rejection. No digital compensation is applied to this input signal and is passed to the Weaver architecture where compensation parameters are computed. Some averaging is performed before the calculation to further reduce the noise for more accurate results. The computed values are stored in the FPGA RAM for future use. Since the imbalance is not the same for all input frequencies, the entire frequency band is sub-divided, and calibration is performed for each sub-band. The process is repeated periodically to account for the drifts in the gain and phase imbalance with temperature and therefore maximum image rejection is always maintained.

B. FPGA Synthesis

Once the design was functionally verified, it was synthesized using Quartus II in a Cyclone IV FPGA (EP4CE40F23C9L). The summary of synthesis is presented in Table 4.

Table 4. Quartus flow summary for the spectrum analyser project

Flow Status	Results
Quartus II Version	13.1 Build 163 10/23/2013 SJ Web Edition
Revision Name	PSA6005_Spectrum_Analyser_Top_Level
Top-level Entity Name	PSA6005_Spectrum_Analyser_Top_Level
Family	Cyclone IV E
Device	EP4CE40F23C9L
Timing Models	Final
Met timing requirements	Yes
Total logic elements	39,126 / 39,600 (99 %)
Total combinational functions	31,270 / 39,600 (79 %)
Dedicated logic registers	26,660 / 39,600 (67 %)
Total registers	26668
Total pins	74 / 329 (22 %)
Total virtual pins	0
Total memory bits	896,672 / 1,161,216 (77 %)
Embedded Multiplier 9-bit elements	232 / 232 (100 %)
Total PLLs	1 / 4 (25 %)

Following synthesis, the design was fitted in the FPGA. The design was analysed to check whether it meets the timing requirements. Finally, programming files were generated to allow programming or configuration of the device. All these procedures were performed by the Quartus II software tool provided by Altera. The design was also analysed to find out how much power it will consume using 'Power Play Power Analyzer Tool' in Quartus II. A schematic was then prepared for the FPGA. Input and output signals were assigned to various pins in the FPGA. Synthesis was carried out again to check the validity of the assignments.

Schematic was prepared so that the FPGA can be configured in JTAG programming mode using 'Altera USB Blaster' during the development stages and in Active Serial (AS) programming mode using serial configuration device during production. Finally, FPGA interface to ADC, micro controller, and other analogue hardware were finalised. Figure 18 shows the interface between the FPGA and the ADC.

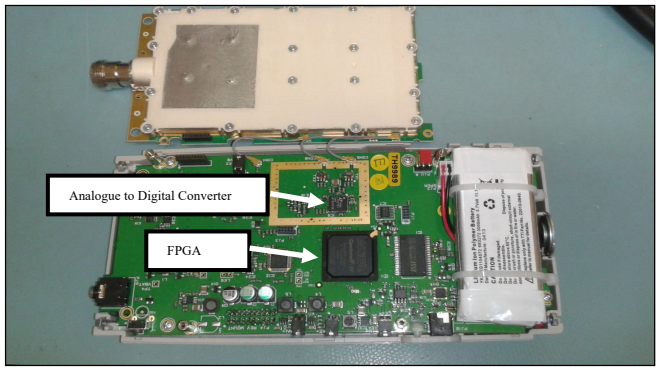


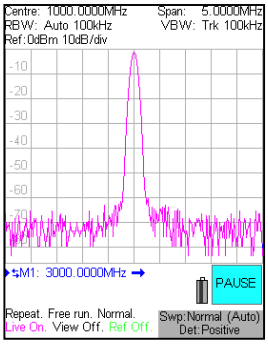
Figure 18. Spectrum analyser prototype board

After preparing the FPGA schematic for the instrument, it was integrated with the RF section and the display interface to prepare the complete spectrum analyser schematic. The PCB layout was then prepared, and the prototype was built, followed by the testing and validation of the functional prototype. The analyser prototype control board as well as the RF board is shown in Figure 18. The device dimensions are 192 mm high, 92 mm wide and 49 mm deep. The device is sufficiently small and lightweight to fit comfortably into the hand, unlike most other handheld spectrum analysers. The total power consumption of the design implemented in FPGA is 373.63mW. The power consumption of the complete unit is 620mA from a 3.7 V lithium-ion battery source. The unit can operate for more than three hours from a fully charged battery.

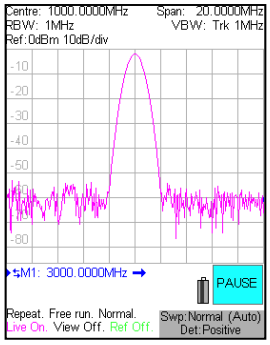
C. Results

The spectrum analyser is a measurement receiver. Therefore, the displayed output provides functional verification of the design. The results presented in this section are screen shots of the actual finished and working spectrum analyser. In the complete unit, measurement sweep is controlled by the controlling processor whereas measurement and sweep detection are done by the FPGA receiver. The control processor then passes on the sweep data to the display processor via Universal Asynchronous Receiver Transmitter (UART) interface. The display processor then displays the measurement on a Thin Film Transistor (TFT) Liquid Crystal Display (LCD). An RF generator was used to provide signal input to the analyser.

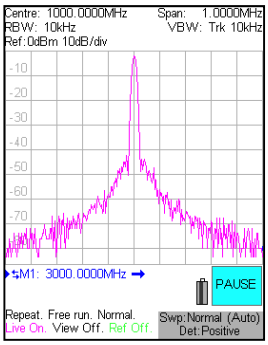
The signal input frequency was chosen to be 1 GHz. The signal source used to test the performance of the spectrum analyser was Keysight (Agilent) N5181A signal generator. The spectrum analyser was programmed to perform a sweep with centre frequency 1 GHz and frequency span of 5 MHz. The frequency range falls in the lower RF frequency band of the architecture. The first RF LO is swept from 4405 MHz to 4415



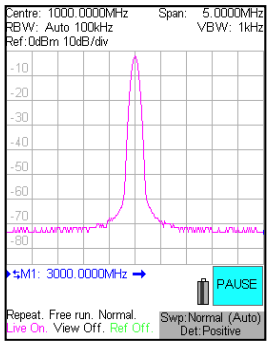
(a). Spectrum of 1 GHz signal input



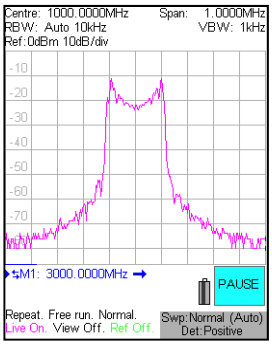
(b). Spectrum of 1 GHz signal input for wide RBW setting



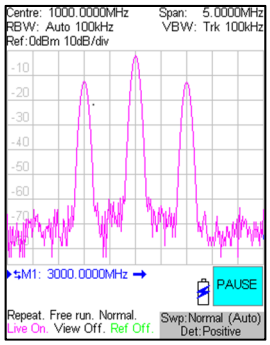
(c). Spectrum of 1 GHz signal input for narrow RBW setting



(d). Spectrum of 1 GHz signal input for narrow VBW setting



(e). Spectrum of FM modulated 1 GHz signal input



(f). Spectrum of AM modulated 1 GHz signal input.

Figure 19. Spectrum results

MHz. The sum frequency is filtered out and the difference frequency is passed to the second RF LO which is fixed at 3410 MHz. The second RF LO down converts the frequency to 10 MHz final analogue IF which is then digitised for further processing.

The RF LO is stepped in 1 MHz steps. The digital LO is stepped in finer resolution. The stepping resolution is RBW dependent. For 100 kHz RBW, the digital LO is stepped in 33 kHz steps.

Figure 19 (a) shows the spectrum result. The result shows that the analyser can display the input waveform. The result validates the amplitude accuracy, resolution bandwidth selectivity and noise floor performance specification of the analyser. RBW and VBW filters were set to 100 kHz. The Gaussian shape of the RBW filter can be clearly seen in the spectrum.

Figure 19 (b) shows the spectrum result for a wider RBW filter setting of 1 MHz. Span is increased to 20 MHz to show the full filter shape. The signal to noise ratio is approximately 10 dB worse than it was for a 100 kHz RBW which is expected. A wider filter will allow more noise to pass through. The filter shape has not changed because it uses the same FIR filter. This result is presented to show that the RBW is a selectable parameter. RBW can be changed from 10 MHz to 300 Hz in 1 – 3 steps.

Figure 19 (c) shows the spectrum result for a narrower RBW filter setting of 10 kHz. Span is decreased to 1 MHz to present a clear spectrum. The noise floor has gone down as expected. But the noise on the skirts of the filter has increased. This is due to the limited phase noise performance of the RF local oscillators. The phase noise of the local oscillators is specified as -83.5 dBc/Hz at 10 kHz offset which is not particularly good. The filter follows the Gaussian shape down to about 50 dB from reference before it hits the noise floor of the oscillators. The shape then becomes horizontal up to the cut-off frequency of the PLL loop filter bandwidth when it starts to decrease again.

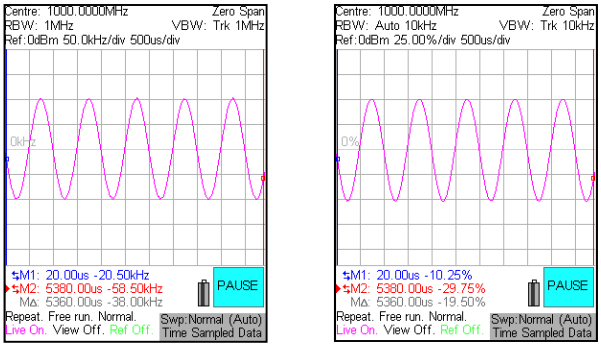
Figure 19 (d) shows the spectrum result for 100 kHz RBW and 1 kHz VBW. As expected, a narrow video bandwidth filter removes more noise from the spectrum output. The effect is like averaging. This result validates the functional verification of the video bandwidth filter performance of the analyser. The video bandwidth filter can be changed from 10 MHz to 300 Hz in 1 – 3 steps.

The signal input is then frequency modulated with 1 kHz sine wave and frequency deviation of 100 kHz. To test the AM and FM modulation performance, the signal source used was Rohde and Schwarz SMR40 signal generator. The spectrum results for FM and AM are shown in Figure 19 (e) and 19 (f) respectively. The following two results validate the frequency demodulation specification of the spectrum analyser.

Figure 20 (a) shows the demodulated waveform. The x-axis is time axis which clearly shows the modulation frequency to be 1 kHz. The y-axis is the deviation axis. The deviation is 100 kHz in either direction. The RBW setting must be wider than the frequency of the modulating waveform and frequency deviation to perform demodulation.

The signal input is then amplitude modulated with 1 kHz sine wave with depth set to 50 %. Figure 20 (b) shows the demodulated waveform. This result validates the amplitude demodulation specification of the spectrum analyser. The x-axis is time axis which clearly shows the modulation frequency to be 1 kHz. The y-axis is the depth axis. The depth is 50 % in either direction. The RBW setting must be wider than the frequency of the modulating waveform to perform demodulation.

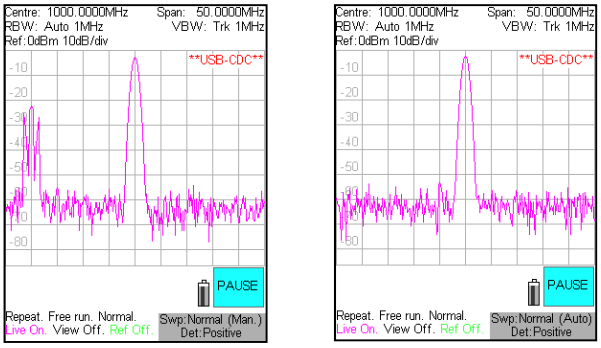
Image rejection is analysed next. For an input signal frequency of 1 GHz, the image falls at 980 MHz. As it is evident from Figure 21 (a), when imbalance compensation is not applied, the inherent image rejection is only about 20 dB which is not acceptable. The peculiar shape of the image is attributed to the coarse and fine stepping sweep method that is used in the instrument. The span is increased to 50 MHz to show both the wanted and image response.



(a). FM Demodulated waveform

(b). AM Demodulated waveform

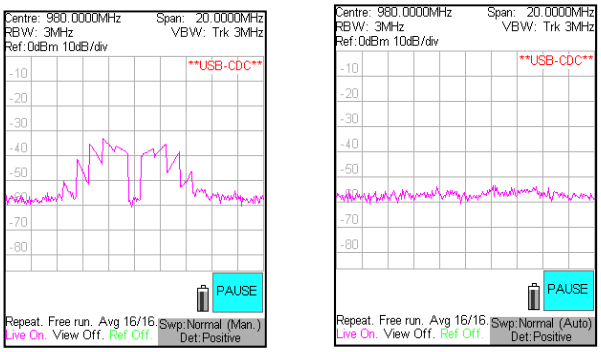
Figure 20. Demodulated results



(a). Image rejection when compensation is not applied

(b). Image rejection when compensation is applied

Figure 21. Image rejection results



(a). Image rejection when IF passband compensation is not applied

(b). Image rejection when IF passband compensation is applied

Figure 22. Results for image rejection in the IF passband

When the gain and phase imbalance is compensated, the image rejection improves drastically as shown in Figure 21 (b). For the same setting, the image is suppressed down to the noise floor when compensation is applied. It is possible to achieve 60 dB of image rejection over the entire input frequency range using the compensation method.

The RF compensation only achieves maximum image rejection at one point in the IF filter passband. Therefore, compensation is required for imbalance variation within the IF passband. This is demonstrated in Figure 22 (a) and Figure 22 (b).

Span is reduced to only concentrate on the image response. A wider RBW is used as the effect is more evident for wide RBWs. Figure 22 (a) shows the image response when IF passband compensation is not applied. The image rejection is maximum at IF. However away from the IF, the image rejection deteriorates. Figure 22 (b) shows the image rejection when IF passband compensation is applied. When IF passband compensation is applied, the image disappears.

Table 5 compares the specification and selling price of the proposed method with other hand-held spectrum analysers that uses state-of-the-art techniques. The table shows that the proposed method achieves the performance and image rejection specification expected from any standard spectrum analyser. The dimensions, weight, and selling price comparisons show that the proposed method significantly simplifies the RF hardware. The power efficiency performance of the proposed method is also considerably better than the products that uses state of the art techniques. The information provided in the table was true when the analysis was carried out. The specification of the products may have changed since then.

V. Conclusions

Spectrum analysers or signal receivers are probably the most important instrument used in test and measurement applications. Recent availability of high performance and low-cost FPGAs opens the possibilities to design customised solutions for this instrument in a single chip.

In this paper, a complete system on chip radio frequency spectrum analyser based on digital signal processing has been developed. IQ image-reject mixers were tailored for application in a wide band system using novel techniques. The results presented validates the new design. The design is completely portable and therefore find use in any generic digital platform.

The spectrum analyser achieved wide frequency range from 10 MHz to 6000 MHz to 100 Hz resolution. A wide range of RBW and VBW filters between 300 Hz and 10 MHz were implemented. The instrument achieved a dynamic range of 84 dB, displayed average noise floor less than -120 dB with -40 dB reference level and a typical specification of 60 dB of image rejection over the entire frequency range. Amplitude accuracy and linearity specification was better than +/- 1 dB.

The linear nature of the image rejection suppression algorithm developed for the analyser design makes it suitable for transient signal analysis. The spectrum analyser design could also be used in a modulator design in a RF generator application where the base band I and Q signals are mixed with RF I and Q LO signals and then added together to generate the RF output. The modulator enables the possibility of implementing complex modulation schemes in the RF generator.

VI. References

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Table 5. Comparison of specification

	Anritsu MS2713E	**Rohde and Schwarz FPH6**	**Keysight N9912A**	**Proposed design**
Architecture	Multi-stage superheterodyne receiver, image rejection performed by analogue RF filters			Low-IF quadrature down conversion receiver, with image rejection in digital baseband
Maximum frequency	6 GHz	6 GHz	6 GHz	6 GHz
Maximum level	+30 dBm	+30 dBm	+20 dBm	+20 dBm
Phase noise (at 100 kHz offset at 1 GHz)	-105 dBc/Hz	-98 dBc/Hz	-95 dBc/Hz	-99 dBc/Hz
Image and other signal related spurs (worst case)	-52 dBc	-50 dBc	-50 dBc	-55 dBc (worst case) -60 dBc (typical)
Battery Life (typical)	3 hours from a 7.5A-hr battery	7 hours from a 11.25 V, 72W-hr battery	4 hours from a 10.8 V, 4.6 A-hr battery	> 3 hours from a 3.7 V, 3A-hr battery
Dimensions	273 x 199 x 91 mm	294 x 202 x 76 mm	292 x 188 x 72 mm	192 x 92 x 49 mm
Weight	3.45 kg	2.5 kg	2.8 kg	0.580 kg
Selling price (approximate)	$11950	$8250	$11900	$2660

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