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ORIGINAL RESEARCH PAPER

A novel resonant ZVS power converter with self-driven synchronous rectifier for low-voltage high-current applications

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Abstract

This paper presents a novel isolated resonant zero-voltage switching converter with a self-driven synchronous rectifier for low-voltage high-current applications. The active resonant tank comprises of a transformer leakage inductance, a capacitor and a diode-connected MOSFET which provides zero-voltage switching conditions for all switches. Due to the use of leakage inductance of the transformer in both the primary and secondary sides, the resonant tank and the output section require no external inductor, resulting in a major size reduction of the circuit. The proposed converter has the advantages of high efficiency; low switching, conducting, and thermal losses; high switching frequency range and isolation; and small size. To verify the proposed converter, a laboratory prototype was manufactured with satisfactory performance. The practical results show that the power efficiencies of the converter including self-driven synchronous rectifier for the light load and the full load are 91.9% and 94.95% at output power P_{out} = 20 W and P_{out} = 100 W, respectively.

1 | INTRODUCTION

Enhancing power density and efficiency are the main requirements of a modern power supply. Soft-switching techniques are developed to reduce switching losses. At zero-voltage switching (ZVS) conditions, not only is the switch voltage-current overlap eliminated, but also the turn-on losses created due to the MOSFET output capacitance (C_{oss}) and reverse recovery of the PN junctions are removed properly [1, 2]. In resonant converters, passive LC circuits are adopted to provide soft switching conditions. In ZVS resonant converters, the switching frequency is increased significantly while the switching, conducting and thermal losses are kept low suitably. Therefore, an ZVS resonant converter is one of the best candidates for a modern power supply [3, 4].

An ever increasing demand is the requirement of off-line low-voltage high-current power supply for electronics loads [5, 6]. Synchronous rectifiers (SR) present much lower conduction losses than the conventional PN/Schottky rectifying diodes [7]. For the SR MOSFETs, the required gate signals should be generated synchronously with the converter DC/AC section [8–10].

The traditional methods use integrated circuits (IC) and self-driven synchronous rectifiers (SDSR). A major problem is the short-circuit condition occurring at the transition intervals created due to reverse-recovery of the PN junctions and the transformer secondary side leakage inductance [11, 12]. Employing current-doubler can intensify this problem [13, 14]. To obviate it, employing current sensors are suggested at the cost of increasing the converter cost and complexity [15]. In the SDSR, the gate signals are generated directly by the transformer auxiliary windings [16, 17]. Compared with gate driving methods which are using ICs, SDSR decreases the design complexity, production cost, elements number, and gate driving loss [18–20]. A problem is the malfunction of SDSR in converters using dead time to regulate output voltage. This happens as, within dead-time intervals, the induced voltage on the auxiliary winding is reduced and consequently the SR may not be driven properly [21].

Integration of ZVS condition and SR is a challenging topic in many researches for different applications [22, 23]. In [12], SR is adopted with asymmetrical half-bridge converter where the output voltage polarity is used to generate gate signals. However, a large inductor should be used after the rectifiers. Another

similar work is presented in [24] where a cascade synchronous boost ZVS converter is introduced. Literature [14] integrated a half-bridge converter with SR and current-doubler. Here, ZVS operation is not achieved for all switches and a DC-block capacitor should be used in this regard. In [25, 26], the converter core comprised a series-resonant converter and a four-diode full-wave rectifier used at the transformer secondary side, but only two diodes are *SR*. The other variant with complicated control and operation is proposed in [27].

This paper presents a converter which benefits from zero-voltage switching, resonance, isolation, integrated transformer and self-driven synchronous rectifier for low-voltage high-current applications. Profiting from advantages of high efficiency; low switching, conducting, and thermal losses; low EMI (electromagnetic interference) and gate driver loss; small size; and high switching frequency range and isolation, this converter can be applied in various applications such as domestic electronic appliances, LED power sources, battery charging purposes, inductively heated appliances, wireless power charging of portable electronics, transcutaneous power transfer systems, biomedical implants, photovoltaic power optimizer, telecom, and other centralized modular and distributed power applications [3, 5, 8, 12]. Furthermore, low-voltage high-current power electronic converters have received huge interest of both industry and academia for their application in stand-alone electric power generating systems. After introducing the operation of the converter, a comparison between three versions of this converter including the converter with simple diode-base rectifier, the converter with SDSR, and the one with diode-connected MOSFET in resonant tank and SDSR in rectification section, is given.

The transformer leakage inductance in conjunction with a resonant capacitor and a diode-connected MOSFET called Q_r form an active resonant network (tank) showing a remarkable difference of the proposed converter from LLC [28]. Thereby, the transformer leakage inductance reflected on the transformer primary side is not problematic, as it is used as a resonant inductor. The employed active resonant tank decreases switching-frequency deviation over the whole range of load variations as well as provides ZVS operation for all switches [25, 27]. The mechanism of this converter, due to its active resonant tank, drastically limits the switching frequency variations to appropriate small values (typically, 10% variations from zero-load to full-load). Thus, components can be designed optimally. A self-driven synchronous rectifier with center-tapped transformer is employed at the transformer secondary side. The output section does not need any additional inductor; therefore, the converter size is greatly reduced. Theoretical analysis and experimental verifications are presented in detail in the following sections to verify the proposed converter.

The paper is organized as follows: Section 2 provides information about our proposed converter and its operation intervals. In Section 3, we further discuss self-driven synchronous rectifier. Section 4 describes experimental results while Sections 5 and 6 discuss the analysis of power loss and concludes the paper respectively. Finally, in the Appendix, ZVS analysis is presented.

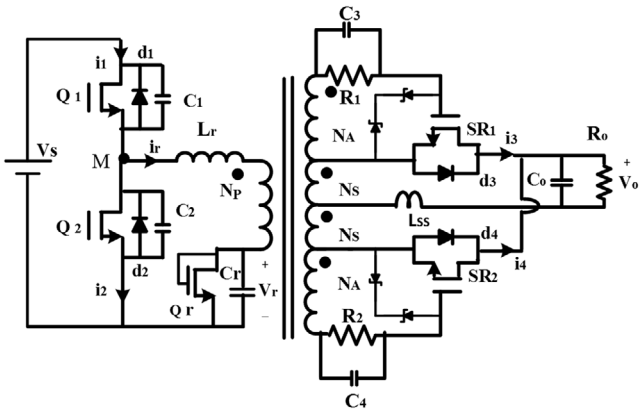

FIGURE 1 Proposed resonant ZVS converter

2 | PROPOSED CONVERTER

The proposed converter is presented in Figure 1 and its operation intervals are illustrated in Figure 2. The converter has seven operation intervals in case of using diode rectifier [29] and 10 in case of using SDSR as shown in Figure 3. The switches Q_1 and Q_2 constitute an inverter leg. The capacitors C_1 and C_2 (with the MOSFET parasitic output capacitance C_{oss}) are set in parallel with the switches to provide ZVS condition at class D [1, 3]. An active resonant tank including L_r, C_r, and Q_r is employed. The resonant inductor L_r can be the sum of the transformer primary leakage inductance and an external inductor. The MOSFET Q_r stabilizes the converter operation. Its junction capacitance is absorbed by C_r; therefore, its reverse-recovery time is not problematic. The switches SR_1 and SR_2 are the output synchronous rectifiers driven by the transformer auxiliary windings. It is assumed that the converter is in the steady state, all the circuit elements are ideal, and the output capacitor C_o is large enough to keep the output voltage constant during one switching cycle. In Equations (1)–(3), we define various parameters which will be used in the following discussion: The parameters α and β are used to simplify the equations and B is the converter normalized voltage gain "$B = nA = nV_o/V_s$. Shown in Figure 2, φ_1 and φ_2 are the conduction angles of Q_1 and Q_2, respectively. In each operation interval, $I_{number} = i_r(t_{number})$. In addition, the parasitic inductance is also used as resonant inductance since its total value is around nH, which will be added to the 25 μH resonant inductance.

$$\omega_r = 2\pi f_r = \frac{2\pi}{T_r} = \frac{1}{\sqrt{L_r C_r}},\ R_o = \frac{n^2 V_o^2}{P_{out}}, \tag{1}$$

$$B = n\frac{V_o}{V_S} = nA,\ Z_r = \sqrt{\frac{L_r}{C_r}}, \tag{2}$$

$$\alpha = \frac{C_r}{C_1 + C_2},\quad \beta = \frac{1+\alpha}{\alpha},\quad \omega_\alpha = \sqrt{1+\alpha}\,\omega_r. \tag{3}$$

Mode 1 ($t_0 < t < t_1$): Prior to t_0, the diode d_1 was conducting and the gate signal for Q_1 has been set. Therefore, at t_0, the

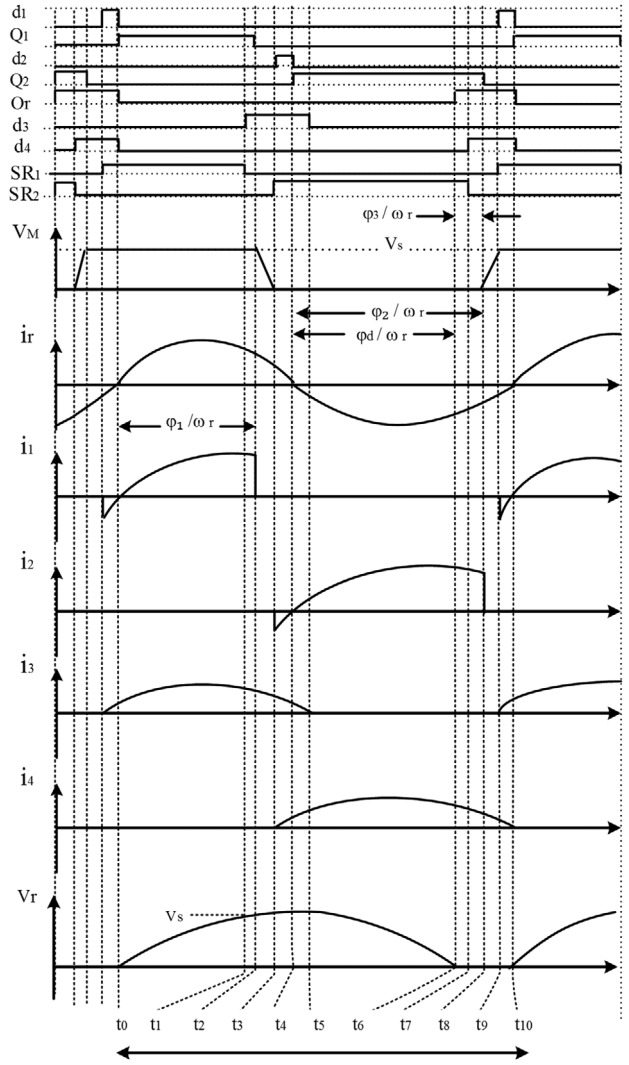

FIGURE 2 Key waveforms of the proposed converter

Q_1 is turned on under the ZVS condition. The voltage of the resonant capacitor (called resonant voltage v_r) is zero at t_0. Due to L_r, v_r starts increasing in a resonant fashion when Q_1 conducts. Then, a positive voltage applies on the primary side of the transformer which reflects to the secondary and auxiliary windings (which provide gate voltage signal for SR_1). Then, the switch SR_1 is turned on and power is delivered to the output.

$$t_1 - t_0 = T_1, \quad T_1 = \frac{\phi_1}{\omega_r}, \tag{4}$$

$$v_r(t) = V_S(1-B)\left[1-\cos(\omega_r(t-t_0))\right], \tag{5}$$

$$i_r(t) = \frac{V_S}{Z_r}\left[(1-B)\sin(\omega_r(t-t_0))\right]. \tag{6}$$

Mode 2 ($t_1 < t < t_2$): By reaching v_r to the voltage of the input source (V_S), the voltage across the primary winding is reduced. Therefore, the auxiliary voltage applied on the gate of SR_1 is also decreased to less than the threshold voltage which causes the MOSFET to turn off.

However, due to the transformer leakage inductance at the secondary side, L_{SS2}, the anti-parallel diode of SR_1 remains ON and continues the current. At the end of this mode, Q_1 is turned off. Due to C_1, Q_1 is turned off at ZVS condition. According to Figure 2, durations of this mode along with the previous mode, in which Q_1 is conducting, is defined as φ_1/ω_r. To provide the phase lag needed to maintain ZVS turn-off, i_r should be positive at t_2, or in other words $\varphi_1 < 180$. All equations of this mode are identical to those of the previous interval.

Mode 3 ($t_2 < t < t_3$): Since t_2 is prior to the zero-crossing instant of the resonant current, i_r, by turning Q_1 off at t_2, the remaining current of L_r flows through C_1 and C_2. Then, the middle voltage (the voltage of node M in Figure 1 which is denoted by v_M), is reduced to zero through a resonant with L_r at t_3.

$$\frac{i_r(t)}{V_s/Z_r} = \frac{(1-B)\cos\phi_1}{\sqrt{1+\alpha}}\sin(\omega_\alpha(t-t_1)) + (1-B)\sin\phi_1\cos(\omega_\alpha(t-t_1)) \tag{7}$$

$$\frac{v_r(t)}{V_s} = \frac{(1-B)\cos\phi_1}{\sqrt{1+\alpha}}\sin(\omega_\alpha(t-t_1)) - \frac{(1-B)\sin\phi_1}{1+\alpha}\cos(\omega_\alpha(t-t_1)). \tag{8}$$

Mode 4 ($t_3 < t < t_4$): At t_3, the diode d_2 is forward biased and i_r flows through it until t_4, when the resonant current i_r becomes zero. The auxiliary winding of the transformer applies a positive voltage on the gate of SR_2 and turns it on. During this mode, the gate signal for Q_2 is set which leads to turning on MOSFET at ZVS. At the time of t_3, the current of I_r is called I_3 which is used in Equation (10). Here, it should be mentioned that $\varphi(t_4 < t < t_5)$ and $\varphi(t_5 < t < t_6)$ are called φ_{x1} and φ_{x2}, respectively. Considering $\frac{-B}{\sin\phi_2} = \gamma$, the equations are as below.

$$\frac{i_r(t)}{V_s/Z_r} = (2B-\gamma)\sin(\omega_r(t-t_3)), \tag{9}$$

$$\frac{v_r(t)}{V_s} = V_s[I_3\sin(\omega_r(t-t_3)) + B], \tag{10}$$

$$\phi_{x1} + \phi_{x2} = \phi_d. \tag{11}$$

Mode 5 ($t_4 < t < t_5$): At t_4, the current of Q_2 becomes positive, then the MOSFET of Q_2 conducts. Due to the transformer secondary side leakage inductance L_{SS2}, the diode d_3 remains ON until t_5, when the current of L_{SS2} is reversed and d_3 is turned OFF at ZCS condition. During this mode, the energy stored in C_r is transferred to the output, but v_r is still positive at t_5.

$$\frac{i_r(t)}{V_s/Z_r} = (2B-\gamma)\sin(\omega_r(t-t4)), \tag{12}$$

$$\frac{v_r(t)}{V_s} = -(2B-\gamma)\cos(\omega_r(t-t_4)) + B. \tag{13}$$

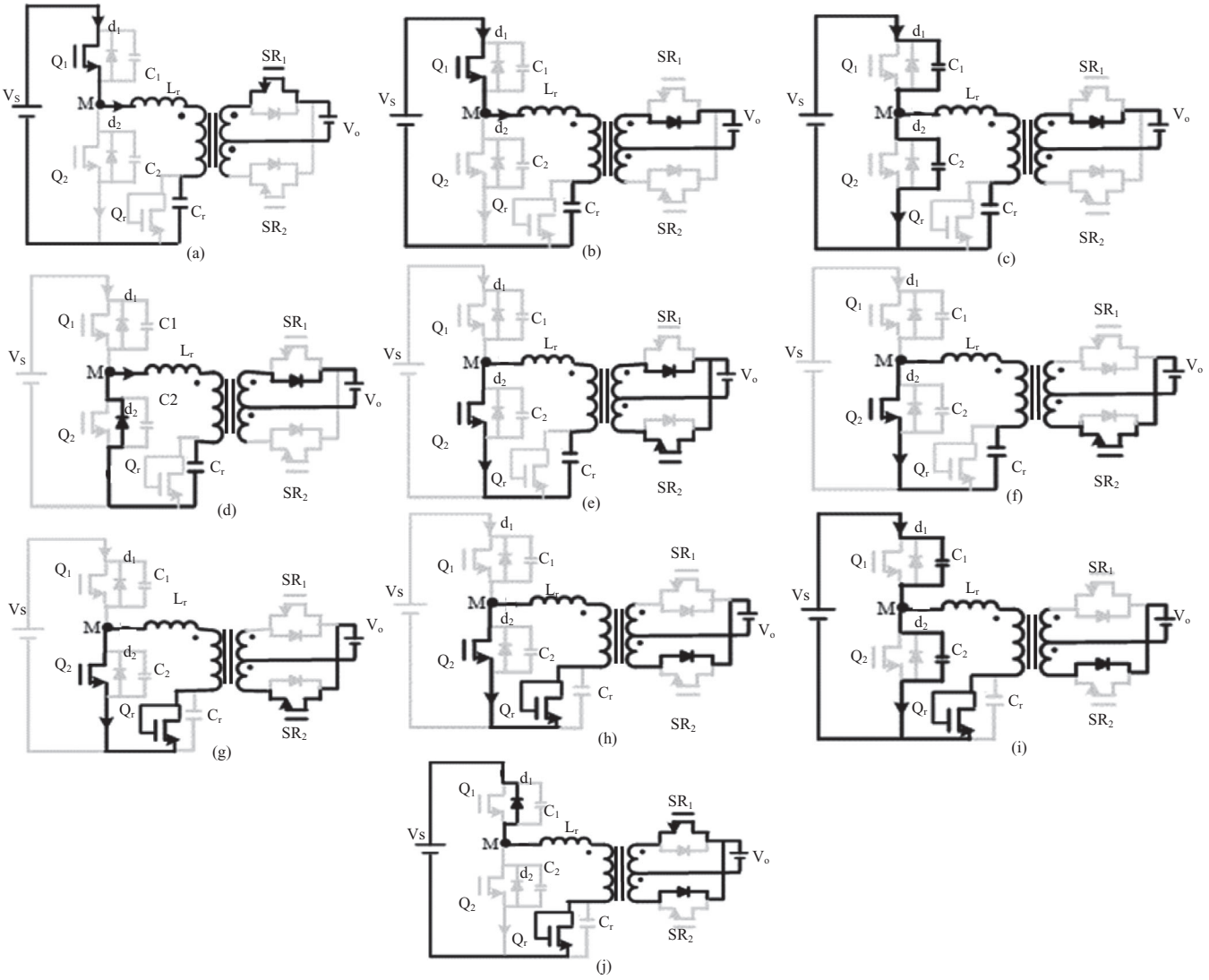

FIGURE 3 Schematic circuit of the proposed high efficiency isolated resonant using a self-driven synchronous rectifier

Mode 6 ***($t_5 < t < t_6$)***: During this mode, remaining energy stored in C_r is transferred to the output until v_r reaches zero at t_6. Shown in Figure 2, the interval from t_4 to t_6 is defined as φ_{d}, which indicates the conduction angle of Q_r.

$$\frac{i_r(t)}{V_s/Z_r} = (2B-\gamma)\left[-\frac{(\cos\phi \mathrm{x}2)}{(\sin\phi x1)}\cos(\omega_{\mathrm{r}}(t-t5)) + [\cos(\omega_{\mathrm{r}}(t-t5))] + \frac{(\sin\phi \mathrm{x}2\cot\phi \mathrm{x}1)}{\mathrm{Cr}} + \frac{\cos\phi \mathrm{x}2}{Cr}\right], \tag{14}$$

$$T_5 + T_6 = \frac{\phi_d}{\omega_r}, \quad \phi_d = \cos^{-1}\left(\frac{B}{2B-\gamma}\right), \tag{15}$$

$$\frac{v_r(t)}{V_s} = (2B-\gamma)\left[\frac{(\cos\phi \mathrm{x}2)}{(\sin\phi \mathrm{x}1)}\sin(\omega_{\mathrm{r}}(t-t_5)) + \cos(\omega_{\mathrm{r}}(t-t_5))\right]. \tag{16}$$

Mode 7 ***($t_6 < t < t_7$)***: By setting v_r to zero at t_6, the diode-connected MOSFET Q_r is forward biased at ZVS. Then the resonant current i_r continues through it and the voltage of v_r is clamped at zero. During this mode, the magnetic energy stored in L_r is transferred to the output and the magnitude of i_r decreases linearly.

$$\frac{i_r(t)}{V_s/Z_r} = B\omega_r(t-t_6) + i_r(t_6). \tag{17}$$

Mode 8 ***($t_7 < t < t_8$)***: At t_7, the voltage of auxiliary winding of SR_2 is reduced to less than the threshold voltage. Hence, SR_2 is turned off while its anti-parallel diode d_3 is still conducting. The preceding equations remain valid for this period, since the substitution of SR_2 with its anti-parallel diode applies no changes in equations. The switch Q_2 is turned off at t_8.

The capacitor C_2 keeps the voltage across Q_2 almost constant at zero and therefore Q_2 turn-off is performed at the ZVS

conditions.

$$T_x = T_7 + T_8 = \frac{\phi_3}{\omega_r}, \tag{18}$$

$$i_x = i_7 + i_8. \tag{19}$$

Mode 9 ($t_8 < t < t_9$): By turning Q_2 off at t_8, the flow of the remaining current in L_r continues through C_1 and C_2 resulting in v_M increasing until its value reaches V_S at t_9.

$$\frac{v_r(t)}{V_s} = V_s\left[\left(-\mathrm{I_x}\sqrt{\alpha}\right)\sin(\omega_r\sqrt{\alpha}(t-t_x)) + \mathrm{B}\cos(\omega_r\sqrt{\alpha}(t-t_x)) - B\right] \tag{20}$$

$$\frac{i_r(t)}{V_s/Z_r} = \left[\frac{\mathrm{B}}{\sqrt{\alpha}}\sin(\omega_r\sqrt{\alpha}(\mathrm{t}-\mathrm{t_x})) + \mathrm{I_x}\cos(\omega_r\sqrt{\alpha}(\mathrm{t}-\mathrm{t_x}))\right] \tag{21}$$

$$T_9 = \frac{1}{\sqrt{\alpha}\omega_r}\cos^{-1}\left[\frac{I_9 I_x(\alpha+B)(1+B)}{B^2 + aI_5^2}\right] \tag{22}$$

$$\frac{i_r(t)}{V_s/Z_r} = \omega_r(t-t_9) + i_r(t_9), \tag{23}$$

$$t_{10} - t_9 = \frac{i_r(t_9)}{\omega_r}. \tag{24}$$

Mode 10 ($t_9 < t < t_{10}$): By reaching v_M to V_S at t_9, the diode d_1 is turned on at ZVS and i_r flows through it until it becomes zero at t_{10}. Then, d_1 and Q_r are turned off at ZCS conditions. At any desired time during this mode, the gate signal of Q_1 is set to turn it on at ZVS condition in the next cycle. It should be mentioned here that no additional mode will be added by C_3 and C_4.

3 | SELF-DRIVEN SYNCHRONOUS RECTIFIER

Considering the literature of driving synchronous rectifiers, there are two methods for driving SR MOSFETs: external and internal gate drivers. This paper uses the latter in the SR stage of the proposed converter. As shown in Figure 1, SR_1 and SR_2 function as a synchronous rectifier and together R_1, R_2, C_3, C_4 as well as Zener diodes protect the SDSR circuit; the transformer auxiliary windings generate the gate signals protected by the back-to-back Zener diodes; also series of resistors control the driving current (Figure 4). The simplicity of this self-driven circuit is one of the advantages of the proposed converter. Enhanced driving circuits may also be employed for further improvement of the system performance at the cost of the circuit complexity [10, 11]. Figure 5 shows the schematic model of the constructed transformer with five layers of winding. Considering the number of winding layers, core size, diameter of wire and the distance between each turn of wire, in this circuit the transformer leakage inductance is used as a whole resonant inductance (i.e. $L_{lk} = L_r$). Thus, the transformer leakage inductance is not problematic. However, its value effects on the resonant tank characteristic impedance Z_r which controls the output power. Furthermore, there is a reflected inductance of 2.7 uH on the secondary side which is called L_{ss} in Figure 1. This reflected inductance is large enough for the synchronous rectifier to work well. To increase the converter power handling capability, the resonant inductor should be small enough and then the transformer leakage inductance should be kept as small as possible.

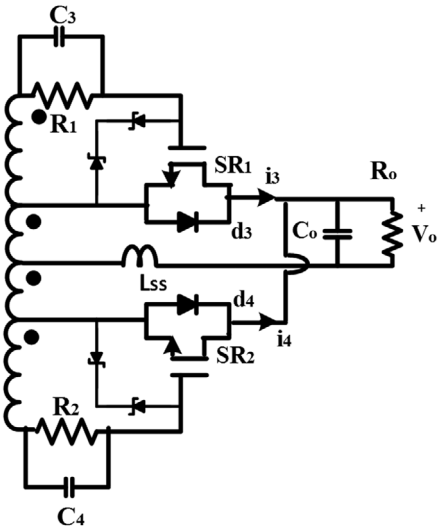

FIGURE 4 Output side of proposed converter with SDSR

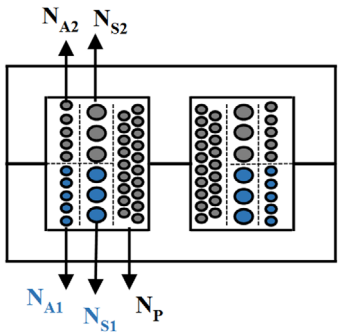

FIGURE 5 Transformer construction model

3.1 | Geometry construction of transformer

As shown in Figure 5, the primary winding (N_P) is the first layer, then the secondary windings (N_{S1} and N_{S2}) are wound as close as possible to N_P. The windings of N_{S1} and N_{S2} should be symmetric with respect to the transformer center line. Then, the auxiliary windings are wound symmetrically; N_{A1} is wound on N_{S1} where N_{A2} is on N_{S2}. Appropriate range of the auxiliary turn number can be found in Equation (25).

where $V_{\text{th,max}}$ and $V_{\text{GS,max}}$ are the maximum threshold-voltage and gate-source voltage of the SR MOSFET, respectively. Lower values for N_A/N_S results in improper turn on, and higher values results in overcurrent and heating up of the gate resistors.

$$\frac{V_{th,\max}}{V_O} < \frac{N_A}{N_S} < \frac{V_{GS,\max}}{V_O} \tag{25}$$

$$\sqrt{1-\left(\frac{L_{ss}}{L_m}\right)^2} = k \tag{26}$$

Moreover, as it is explained in Appendix, the value of n is 10 ($B = 0.33$). Thus, N_A should be a number between 0.8 and 4, which is considered as 2 (notice that $N_S = 1$).

Among all types of cores, ferrite cores are generally used for switching power supplies. Ferrites can work during operation at higher flux densities and frequencies. Among different ferrite cores, the PQ cores with high flux density and permeability are applicable for power supplies. Concluding all reasons given, the PQ 40/40 core is selected. To improve the performance and to decrease the size of circuit together, three transformers are merged into one in this paper. Also, to have a lower leakage inductance, all gaps are avoided between cores. Another factor which is very important to take into account is transformer coupling. Considering Equation (26), by using PQ 40/40, an excellent coupling of 0.99 will be reached for transformer ($L_m = 19$ uH attained in PSPICE).

4 | EXPERIMENTAL RESULTS

A prototype of the proposed converter with SDSR was made in laboratory with specifications such as: input voltage $V_s = 150$ V, output voltage $V_o = 5$ V, output current $I_o = 20$ A, switching frequency fs-full = 220 kHz for full-load waveforms, and fs-light = 330 kHz for light-load waveforms. Furthermore, the components used in this converter are: $Q_1 = Q_2 = Q_r =$ IRF640, $SR_1 = SR_2 =$ IRF1404, and $C_r = 23$ nF (SMD/600 V). The gate signal for the switches in the primary side has been produced by the external gate drivers. For the resonant inductance, the leakage inductance of transformer is used as Llk = 25 μH. To measure currents of Q_1, Q_2, and L_r, two resistors of 0.5 and 0.33 Ω are used for full-load and light-load modes, respectively. Considering $f_r = 202$ kHz (selected close to $fs = 220$ kHz), $C_1 = C_2$ (symmetrical design), overdesign = 1.2, $\alpha = 6$ (explained in Appendix), and the Equations Equations (1), (2), and (28), the values of C_r, L_r, C_1, and $C2$ are attained, as presented in Table 1. It should be mentioned that fs and Pout for full-load are equal to 220 kHz and 100 W, while they are 330 kHz and 20 W for light-load, respectively. To wind the transformer, a wire with diameter of 0.55 mm is used for the primary side as well as two parallel wires with diameters of 0.55 mm for the secondary side.

To have a reliable self-driven method, a wire with diameter of 0.25 mm is used to transfer both SRs gate signals. In addition,

TABLE 1 Parameters and components of the circuit

Symbol	Full-Load—Light-load
Vs	150 V
Vo	5 V
P_{out}	100–20 W
f_s	220–330 kHz
C_r	23 nF
L_r	25 μH
C_1	1 nF
C_2	1 nF
R_1	0.5 Ω
R_2	0.5 Ω
f_r	202 kHz

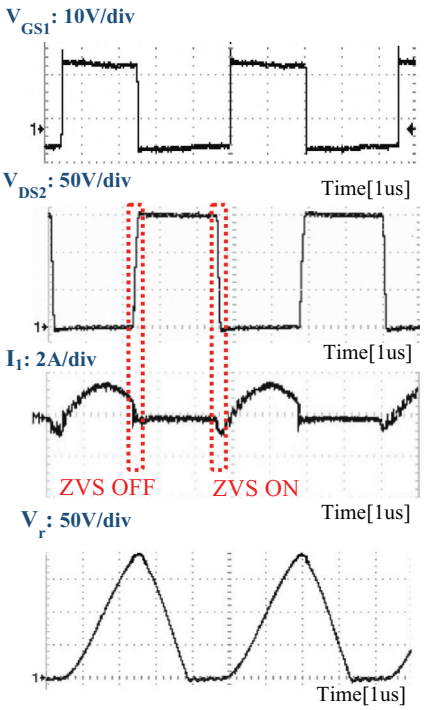

FIGURE 6 Practical waveforms for Q_1 and resonant voltage in full load mode (Pout = 100 W, fs = 220 kHz, 1 us/div, Period = 4.54 us)

Figures 6 and 7 show practical waveforms for primary side of transformer in full-load case, where both "ZVS turn-on" and "ZVS turn-off" are obtained for Q_1 and Q_2. In addition, it is demonstrated that currents of Q_1 and Q_2 are negative for a few tenths of microseconds, when the primary side switches are turned on and off. It should be noted that the horizontal axes in all figures from Figures 6–11 represents time with time division mentioned below each figure, while the vertical axe is defined above each figure.

The behavior of v_r and i_r is also shown in Figures 6 and 7, where v_r rises until the moment i_r becomes negative. At this time, v_r starts decreasing gradually to zero, when Q_r is turned on for transferring magnetic energy stored in L_r to the output,

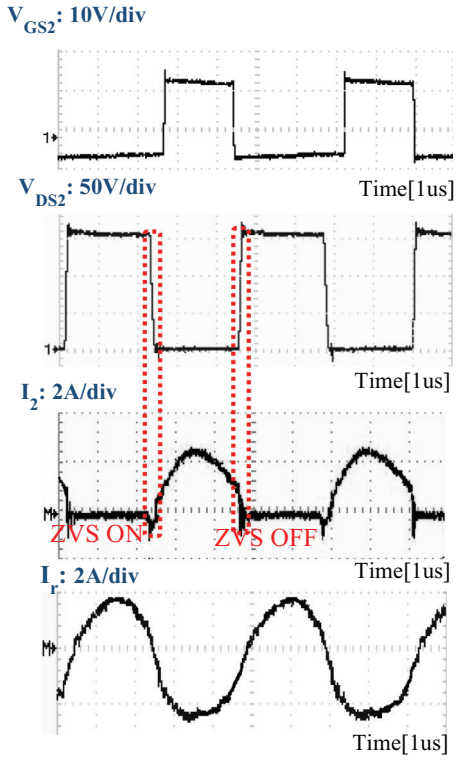

FIGURE 7 Practical waveforms for Q_2 and resonant current in full load mode (Pout = 100 W, fs = 220 kHz, 1 us/div, Period = 4.54 us)

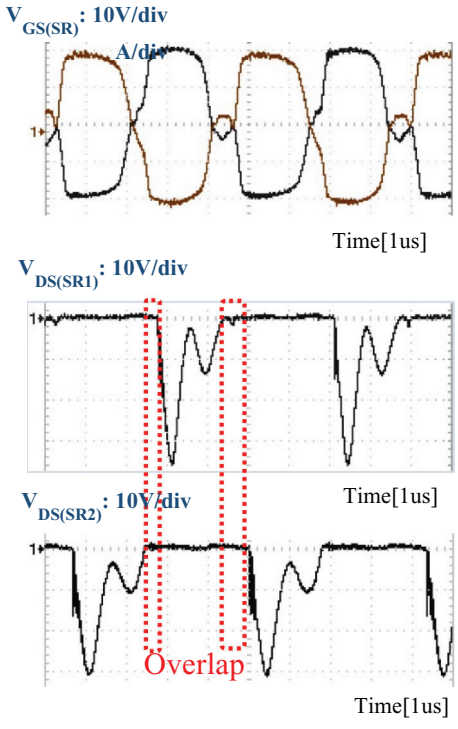

FIGURE 8 Practical waveforms for secondary side in full load mode (Pout = 100 W, fs = 220 kHz, 1 us/div, Period = 4.54 us)

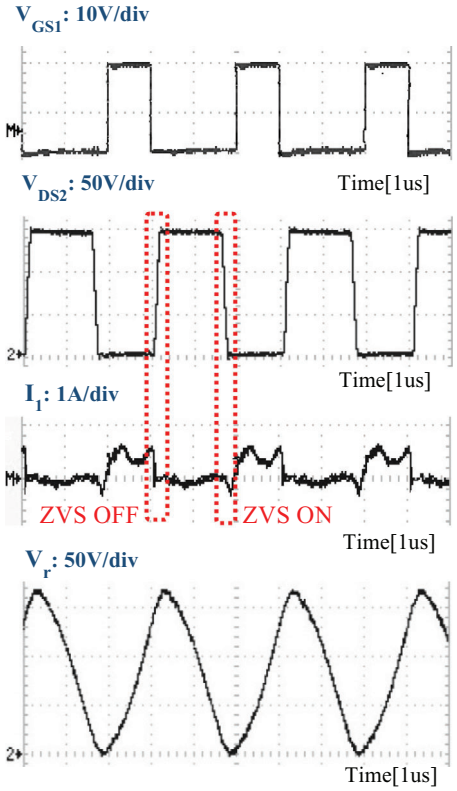

FIGURE 9 Practical waveforms for Q_1 and resonant voltage in light load mode (Pout = 20 W, fs = 330 kHz, 1 us/div, Period = 3.03 us)

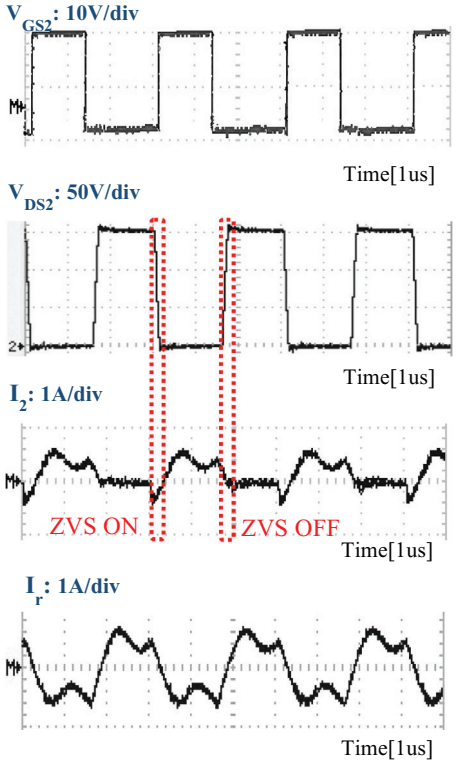

FIGURE 10 Practical waveforms for Q_2 and resonant current in light load mode (Pout = 20 W, fs = 330 kHz, 1 us/div, Period = 3.03 us)

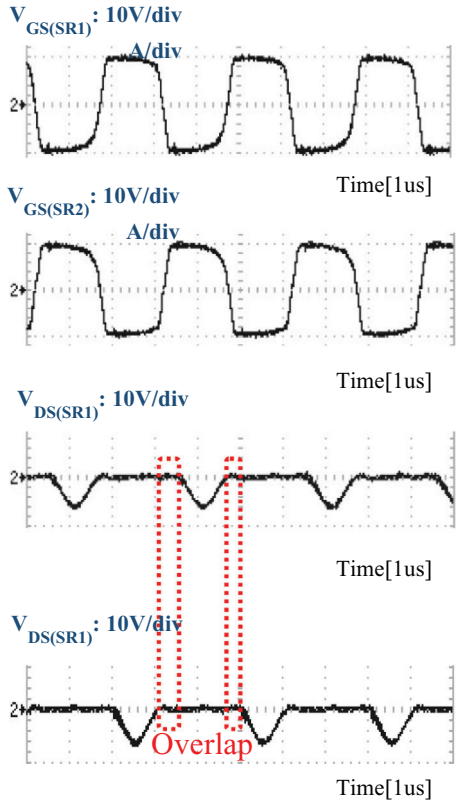

FIGURE 11 Practical waveforms for secondary side in light load mode (Pout = 20 W, fs = 330 kHz, 1 us/div, Period = 3.03 us)

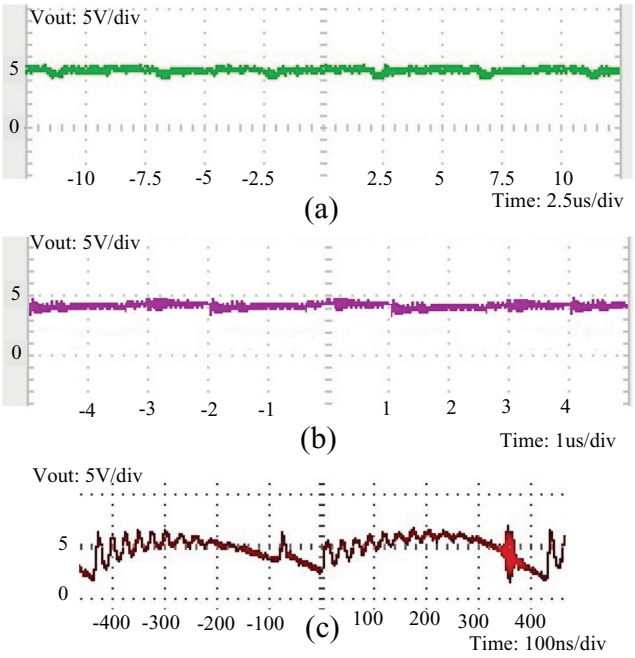

FIGURE 12 Output voltage. (a) Output voltage of full-load mode (Pout = 100 W, fs = 220 kHz, 2.5 us/div, 5 V/div), (b) Output voltage of light-load mode (Pout = 20 W, fs = 330 kHz, 1 us/div, 5 V/div), (c) Output voltage ripple of full-load (Pout = 100 W, fs = 220 kHz, 100 ns/div, 5 V/div)

resulting in the linear reduction of i_r. In Figure 8, experimental waveforms of secondary side are illustrated, where both gate signals generated from a transformer with self-driven circuit and two drain-source voltages of SRs with indicated overlapping periods are highlighted. Figures 9 and 10 show practical waveforms of the prototype for Q_1, Q_2, v_r, and i_r in the light-load case. Similar to full-load approach, "ZVS turn-on" and "ZVS turn-off" are attained for both Q_1 and Q_2. Compared to full load case, the period of Q_r conducting is very short; in other words, the linear interval is not long compared to others.

The gate signals produced by the transformers are very appropriate for running both SRs correctly as shown in Figure 11. In Figure 12, the output voltages for both modes are shown where the R_{out} is 0.25 and 1.175 Ω for full-load and light-load, respectively.

As shown in Figure 13, reducing f_n ($f_n = f_s/f_r$) increases the output power. Thus, by selecting two close values for resonant and switching frequencies, that is, f_r and f_s, the output power will rise. Figure 14 shows the impact of output power on efficiency of the proposed converter.

A comparison between different converters is also shown in Figure 14. It should be mentioned that the winding capacitance of the proposed converter in secondary side is low enough to be neglected. Furthermore, in the primary side, the winding capacitance is not problematic, since the resonant capacitor is 23 nF; thus, the winding capacitance which is about pF, is absorbed by C_r. As illustrated in Figure 14, for a range of output powers

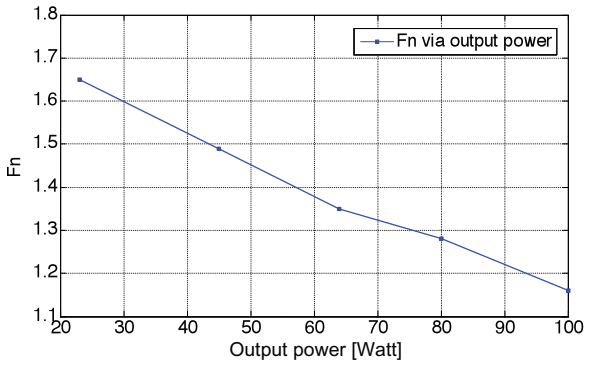

FIGURE 13 Ratio of switching frequency to resonant frequency for different output powers

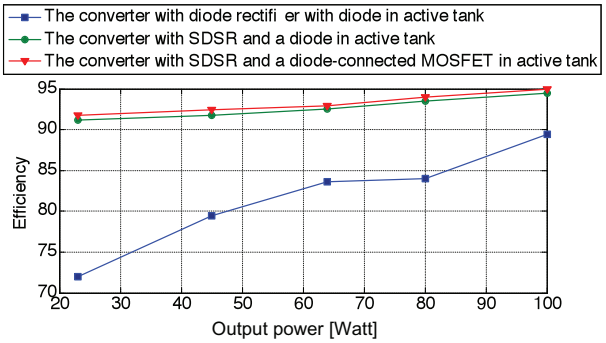

FIGURE 14 Efficiency versus output power

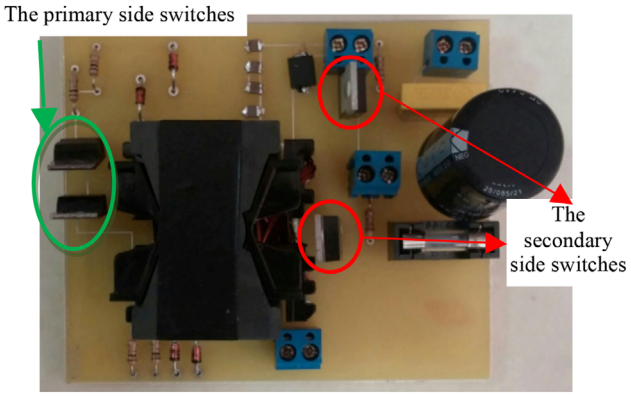

FIGURE 15 Converter prototype

TABLE 2 Comparison of the proposed converter and prior art

References Features	[7]	[31]	[27]	Proposed converter
Input voltage	12 V	390 V	120 V	150 V
Output voltage/Current	5 V/2 A	12 V/25 A	80 V/8 A	5 V/20 A
Maximum efficiency	79.50%	92.50%	93.00%	94.95%
Switching frequency	40 kHz	110 kHz	180 kHz	220 kHz
Resonant frequency	40 kHz	56 kHz	167 kHz	202 kHz
Self-driven circuit	No	No	No	Yes
Zero-voltage switching	No	Yes	Yes	Yes

between light-load and full-load cases, the proposed converter including diode-connected MOSFET in the active tank with SDSR has a higher efficiency than the one working with diode in the resonant tank. The efficiency has a slight rise from 91.9% to 94.95% for diode-connected MOSFET with SDSR and a gradual rise from 91.2% to 94.35% for the converter with diode in resonant tank and SDSR in rectification section, which shows a slight better performance of this circuit. Furthermore, the proposed structure of the converter with diode in active tank and rectifier has the efficiency gradually raised from 72% to 89% for different output powers [30, 31]. This comparison can show the slightly better efficiency of the proposed converter with diode-connected MOSFET and SDSR. Comparing all experimental and theoretical waveforms, the correctness of theoretical analysis is verified. Finally, Figure 15 shows the manufactured laboratory prototype. Regarding the size of the converter, the main PCB board size is 15 cm × 10 cm where the bulky part of constructed converter is the transformer core (PQ 40/40).

Considering the problems that can arise from mismatch in converter operation, we will further discuss it in detail in the subsequent paragraphs. Mismatch in transformer design such as turn-ratio can affect the performance of the converter. Firstly, change in the transformer turn-ratio can affect power conversion, voltage, and current as they are a function of the ratio. However, in transformer design, the turn-ratio can be kept relatively constant since a small mismatch in transformer design could hardly change the number of turns in the transformer primary and secondary sides. Secondly, mismatch in turn-ratio, geometry of construction, or distance between coil windings of a transformer may change the leakage inductance of the transformer, reflected on the primary and secondary sides, which may further affect the active resonant frequency and voltage level. However, we would not expect that such changes are significant due to our careful design, and if it is necessary, small change in the leakage inductance can be compensated by adding a small inductor in series or parallel depending on if the leakage inductance becomes smaller or larger due to the mismatch.

Finally, mismatch in transformer design may affect its resistance and thus the converter efficiency. This is less significant though, as in the design of the transformer we have very few turns of windings to achieve the desired inductance which leads to very small negligible resistance in the transformer. Thus, any possible change in transformer resistance due to mismatch would unlikely increase the transformer resistance and decrease the converter efficiency significantly.

Table 2 compares the performance of the proposed converter with prior researches [7, 27, 31] in terms of power efficiency, switching and resonant frequencies, self-drive, and ZVS methods. The proposed converter provides better efficiency than the others as seen in Table 2. Furthermore, the significant higher switching and resonant frequencies are applied in the proposed converter, which contribute to the high efficiency. Additionally, comparisons are made in terms of self-driven gate driver used for SRs which leads to reduced gate driver losses and whole converter size by omitting the external gate drivers, as well as the ZVS condition which provides advantages such as lower switching and capacitance losses.

5 | POWER LOSS ANALYSIS

The proposed converter mentioned here benefits from low switching, conducting and thermal losses due to ZVS condition which removes not only the switch voltage–current overlap, but also the losses produced by the MOSFET output capacitance (C_{oss}) and reverse recovery of PN junctions. Hence, the main power loss in the proposed circuit is created due to the overlap occurred in two drain-source voltages of SRs in the output section. Considering the efficiency and input power of the converter, the total power dissipation can be calculated as 5.05 Watt in full-load and 1.65 Watt in light-load condition.

With regards to voltage gain in a constant state, the voltage gain can be found by using energy balance in one switching cycle. In Equations (27) and (28), input and output energy as well as voltage gain are shown as ε_{in}, ε_{out} and A, respectively. Considering that ε_{in} should be equal to ε_{out}, the final equation is found for A which will further help to find the theoretical value of different elements in circuit.

$$\begin{cases} \varepsilon_{out} = \dfrac{1}{R}\displaystyle\int_{Ts} V_o^2 dt \cong \dfrac{V_o^2 T_s}{R} \\ \varepsilon_{in} = 2(1-B)C_r V_s^2 \end{cases}, \tag{27}$$

$$\begin{cases} \varepsilon_{in} = \varepsilon_{out}, \\ A = -nRC_r f_s + \sqrt{n^2 R^2 C_r^2 f_s^2 + RC_r f_s} \end{cases}. \quad (28)$$

6 | CONCLUSION

A new isolated resonant converter with ZVS and SDSR is presented for low-voltage and high-current applications. The active resonant tank is composed of a transformer leakage inductance, a capacitor, and a diode-connected MOSFET in the primary side which provides ZVS conditions for all switches. A simple SDSR with a center-tapped transformer is employed at the secondary side to improve converter performance. The converter itself produces the required gate signals to run MOSFETs in a synchronous rectifier. Due to the use of transformer leakage inductance in the primary and secondary side as the resonant and output inductors, respectively, there is no need to add any further external inductor, resulting in a major size reduction of the circuit. Experimental results show that the power efficiencies of the converter including SDSR for the light load and the full load are 91.9% and 94.95% at output power $P_{\text{out}} = 20$ W and $P_{\text{out}} = 100$ W, respectively.

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APPENDICES

ZVS Analyses: The conditions needed to provide ZVS operation are studied in [29] and presented here. ZVS operation for both Q_1 and Q_2 are considered. At the end of mode 3, if i_r is still positive, the anti-parallel diode of Q_2 will be turned on at the next interval and consequently ZVS turn-on is achieved for Q_2. It can be shown this constraint leads to the inequality of Equation (A1) where B_{max} is a maximum for normalized voltage gain $B = nA$. Considering that V_M should decrease from V_S to zero, energy in L_r would remain enough at t_2. So, $i_r(t_3)$ is set larger than zero $i_r(t_3) > 0$ and then to have root for this inequality, Δ should be greater than zero $\Delta \geq 0$. Solving this inequality, B_{max} is found. Having B_{max} and solving $i_r(t_3) > 0$, the roots are found as it is shown in Figure 4. For different values of α, φ_{1u} is always between 1 and -1. As a result, the inequality of $\varphi_1 < \varphi_{1u}$ is reached for the whole range of $B < B_{max}$ in Equation (A1).

Considering Figure A1(a), it is shown that for some values of B, $\varphi_{1k} > 1$. Thus, φ_{1k} should be limited to $\varphi_{1k} < 1$. Solving this inequality, a new value for B, named B_k, is achieved (Figure A1(b)). In this figure, B_k is always less than B_{max}. So two conditions for Q_2 ZVS turn-on are reached in Equations (A2) and (A3).

$$B \leq B_{max}, \qquad B_{max} = 1 - \frac{1}{\sqrt{\alpha}} \tag{A1}$$

$$\phi_{1U} = \cos^{-1}\left[\frac{1}{\alpha(1-B)} - \sqrt{1 - \frac{1}{\alpha(1-B)^2}}\right], \tag{A2}$$

$$\phi_{1K} = \cos^{-1}\left[\frac{1}{\alpha(1-B)} + \sqrt{1 - \frac{1}{\alpha(1-B)^2}}\right]$$

At mode 9, the voltage V_M can reach V_s if Equation (A4) is satisfied (ZVS turn-on conditions for Q_1). The constraint of Equation (A4) results in φ_3 has an upper limit as φ_{3u} which is given by Equation (A5). Solving the inequality of $\varphi_{3u} > 0$, two roots are found, named φ_{1f} and φ_{2f} (Figure A1(c)). Regarding Figure A1(c) for whole range of α, φ_{2f} is greater than 1 but for some cases $\varphi_{1f} \leq -1$. The limitation of $1 > \varphi_{1f} \geq -1$ should be considered. Solving the inequality $\varphi_{1f} \geq -1$ by curve fitting in MATLAB, a new value for B is found, named B_d. Figure A1(d)

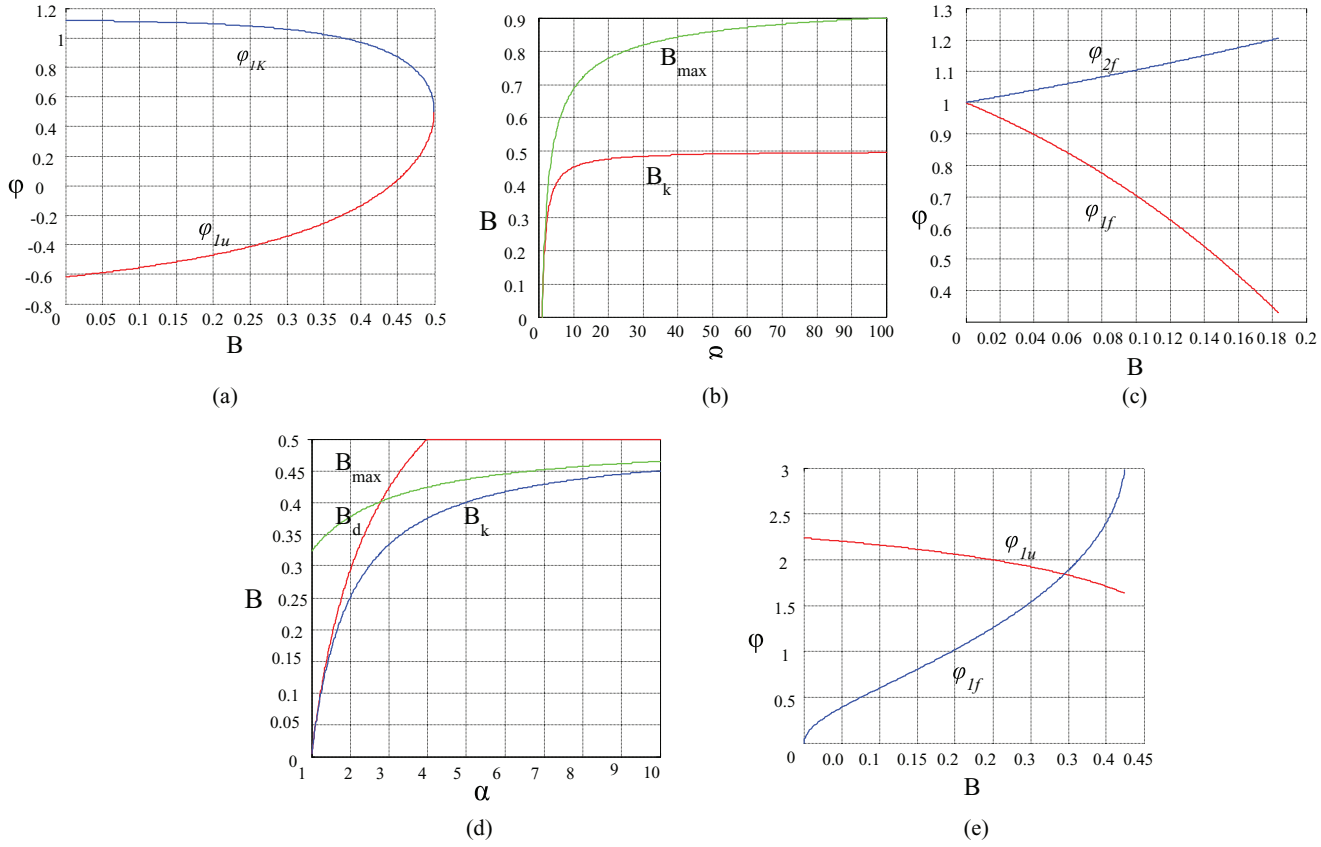

FIGURE A1 Graphs plotted in MATLAB: (a) φ_{1U} and φ_{1K} versus φ, (b) B versus α, (c) φ_{2f} and φ_{1f} versus φ, (d) B_d, B_{max}, B_k versus α, (e) φ_{1f} and φ_{1u} versus B

shows the graphs plotted for B_{max}, B_d, and B_k. As shown in this figure, B_k is always less than B_{max}. Therefore, the inequality of $B < (0.5, B_{max}, B_d)$ should be considered and then the result of this unity is $\varphi_{1f} < \varphi_{1u}$ (Figure A1(e)). As shown in Figure A1(e) for some values of α, φ_{1f} is less than φ1u. To solve it, curve fitting method is used and it results in B_f in Equation (A6). Concluding all these conditions for B, the best values for B and α are 0.33 and 6 (a number between 5.5 and 6.5), respectively. Thus, the proper value for n is 10.

$$\left\{ \begin{cases} B < B_k \\ \phi_1 < \phi_{1u} \end{cases}, \begin{cases} B > B_k \\ \phi_{1k} < \phi_1 < \phi_{1u} \end{cases} \right. \tag{A3}$$

$$\left| i_r(t_7) + i_r(t_8) \right| \geq \sqrt{\frac{1+2B}{\alpha}} \quad \rightarrow \phi_3 \leq \phi_{3U} \tag{A4}$$

$$\phi_{3U} = \sqrt{\frac{(2B-\gamma)^2 - B^2}{B^2}} - \sqrt{\frac{2B+1}{\alpha B^2}} > 0 \tag{A5}$$

$$\begin{cases} B_d = \dfrac{0.5a + 0.231}{a + 1.263} \\ B_f = \dfrac{a+1}{2a + 0.7574} \end{cases} \tag{A6}$$