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A Multi-Value 3D Crossbar Array Nonvolatile Memory Based on Pure Memristors

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Abstract. How to improve the storage density and solve the sneak path current problem has become the key to the design of nonvolatile memristive memory. In this paper, a high storage density and high reading/writing speed 3D crossbar array non-volatile memory based on pure memristors is proposed. The main works are as follows: 1) an extensible memristive cluster is proposed, 2) a memristive switch is designed, and 3) a 3D crossbar array non-volatile memory is constructed. The memory cell of the 3D crossbar array non-volatile memory is constructed by pure memristors and can be extended by adding memristor in a memristive cluster or adding memristive clusters in a memory cell to realize multi-value storage. The memristive switch can effectively reduce the sneak path current effect. The pure memristive memory cell solves the conflict between the storage density and sneak path current effect, greatly improve the storage density of memory cells. Furthermore, the 3D cross-array structure allows different memory cells on the same layer or different layers to be read and written in parallel, which greatly improves the speed of reading and writing. Simulations with PSpice verifies that the proposed memristive cluster can realize stable multi-value storage, has higher storage density, faster reading and writing speed, fewer input ports and output ports, better stability, and lower power consumption. Moreover, the structure proposed in this paper can also be used in the circuit design of the neuromorphic network, logic circuit, and other memristive circuits.

1 Introduction

With scaling of CMOS in the Nano ranges, the technology advances predicted by Moore's Law are becoming difficult to meet, which limits the rapid development of

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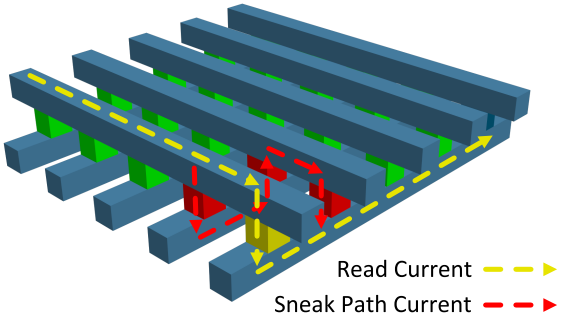


Fig. 1. The sneak path current in crossbar-array.

information technology. Memristor[1,2], as a new device after resistor, capacitor and inductor, owning to the property of low power, low area footprint, device scalability, nonvolatility, fast switching speed, high switching endurance and CMOS compatibility has been widely used in the design of neuromorphic network[2–6], logic circuit[10–14] and chaotic circuit[15,16]. Especially in design of non-volatile memory devices[17,18], memristor is considered as one of the most promising candidates, gaining significant interest.

Memristor is realized with sandwich metal-oxide-metal structure. In terms of theoretical research, conducting filament mechanism has been well acknowledged, research results show that the growth of the conducting filament determines the conductivity of the memristor and switching speeds, which are related to the area and thickness. Different area and thickness of memristor can have different V_{set}, V_{reset}, R_{on} and R_{off} properties of the memristor[19,20].

The developments of memristor materials[21,22], models[23–26], and the circuit realize based on memristor[7–9] have promoted the development of memristive memory technology. There are two main designs to realize memristive memory. One is two value storage with one memristor, such as 1T1R and 2M1M[29] memory cell. This kind of designes based on the binary characteristics of the memristor have the advantages of stability, simplicity, and easy implementation, but the disadvantage is low storage density. The other one is multi-value memory design with higher storage density. Early designs of multi-value memory cell takes the advantage of the internal state of the memristor as a function of applied voltage, but the resistance of memristor is susceptible to drift due to external environmental influences, such as temperature, voltage, and current, thus does not fit the stable requirement of memory[30]. Then more multi-value memory cells are designed with two or more binary feature memristors, such as 1T2M[31,32] memory cell, which can save 4 values in one memory cell with 1 transistor and 2 memristors.

Sneak path are undesired paths for current, parallel to the intended path, as shown in Fig. 1, which can read and change the unselected cells, and decrease the reliability of memory. The source of the sneak path is the fact that the memristor is bidirectional[33]. To solve this problem, switches are required in the cell structure to prevent the current flow through the unexpected cells. Early researchers proposed a memory cell structure of one diode and one memristor (1D1R)[34], then a more common one transistor and one memristor structure (1T1R)[35], recently, a 2D1M memory cell is proposed[38]. But the use of diode and transistor changes the memory cell circuits to a hybrid circuit, which decreases the storage density. The literature[29] proposed a 2M1M memory cell, where two memristors are employed to compose a switch, and one memristor is used to store two values. The 2M1M memory cell changes

the circuit of memory cell to a pure memristive circuit. However, this structure does not implement multi-value storage.

Based on the above analyses, in this paper, a pure memristive multi-value 3D crossbar array nonvolatile memory is proposed. The main contributions of this paper are as follows.

1) A memristive cluster including N different memristors in parallel is proposed. The cluster can store 2^N values with a stable state, and the writing operations and reading operations can be achieved through a single input and single output.
2) A pure memristive memory cell is proposed, which is composed of a memristive cluster and a memristive switch. The switch is composed of two memristors connected in reverse. The memory cell has smaller area, and the sneak path current effect of the crossbar-array can be eliminated effectively.
3) A 3D crossbar array is proposed with the above memristive memory celles, which has only one reading line and writing line for each cell, and a line connecting each layer, controlling the switch on or off state. Compared with the existing crossbar arrays, the proposed 3D crossbar-array has higher density, lower power and more reliability.

The remainder of this paper is organized as follows. In Section 1 the background of memristive memory, switch and crossbar array are presented. The memristor model used in this paper is introduced in Section 2. In Section 3, the details of the proposed memristive cluster and memristive switch are discussed. Section 4 presents a 3D crossbar array for for multi-value storage. Section 5 displays simulation results, and compares the proposed crossbar array with existing works. Section 6 concludes the paper.

2 Preliminaries

2.1 Memristor Device

After HP memristor device, a lot of memristor devices with different material have been provide, where Yu el[36] developed a physics-based compact device model and applied it in conducting-bridge random-access memory (CBRAM). By considering the dependence of ion migration velocity on the electric field, the vertical and lateral growth/dissolution dynamics for the metallic filament are investigated. Currently, the result about conductive filaments (CF) has been widely accepted.

The filamentary conduction mechanism can be described as follows. A compact memristor is a stack of active electrode, solid electrolyte, and inert electrode. Due to the influence of electric field, ions will migrate, so CF will experience four processes from the vertical growth, the lateral growth, the lateral dissolution to the vertical dissolution. Considering the CF vertical evolution dynamics, when the CF height h is known, the resistance R_{off} is estimated to be

$$R_{off} = (\rho_{on} h + \rho_{off}(L - h))/A, \tag{1}$$

ρ_{on} is the CF resistivity, ρ_{off} is the nonconducting solid- resistivity. And A is the area under CF. When considering the CF lateral evolution dynamics, CF was considered to be cone-shaped, and the cell resistance after the set occurs is expressed as

$$R_{on} = \rho_{on} L/(\pi \cdot r \cdot R). \tag{2}$$

In this case, R is the radius at the bottom of CF. In view of the mechanism of creating conductive filaments, the resistors R_{on} and R_{off} have the property of being modifiable.

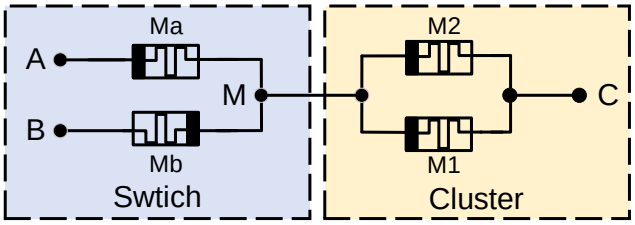


Fig. 2. The proposed pure memristive memory cell.

2.2 Memristor Model

The VTEAM model possesses many advantages, it is simple, general, and flexible and can characterize different voltage controlled memristors. In the VTEAM model, resistance changes when the voltage is higher than the threshold voltage. Compared with the non-threshold model, this model is simpler, more universal and can achieve sufficient accuracy. In this paper, VTEAM model is used for simulation, analysis and calculation.

The VTEAM model is represented by

$$\frac{d\omega(t)}{dt} = \begin{cases} k_{off} \cdot (\frac{v(t)}{v_{off}} - 1)^{\alpha_{off}} \cdot f(\omega), & v < v_{off} < 0 \\ 0, & v_{off} < v < v_{on} \\ k_{on} \cdot (\frac{v(t)}{v_{on}} - 1)^{\alpha_{on}} \cdot f(\omega), & 0 < v_{on} < v \end{cases} \tag{3}$$

and

$$i(t) = \left[R_{on} + \frac{R_{off} - R_{on}}{\omega_{off} - \omega_{on}} \cdot (\omega - \omega_{on}) \right]^{-1} \cdot v(t). \tag{4}$$

Where ω represents the internal state variable, $\omega \in [\omega_{on}, \omega_{off}]$, v(t) and i(t) represent the voltage and current flowing through the memristor, respectively, R_{on} and R_{off} represent the resistance of the memristor in the low resistance state (LRS) and high resistance state (HRS). $f(\omega)$ in Eq. (3) is expressed as a velocity adaptive function. The window function used in this paper is

$$f(\omega) = \begin{cases} (a \cdot (1 - \frac{\omega}{D}))^p, & v < v_{off} < 0; \\ (a \cdot \frac{\omega}{D})^p, & 0 < v_{on} < v. \end{cases} \tag{5}$$

The window function can solve the boundary problem well. The shape of the curve can be adjusted by controlling the exponential parameter p, and the linear parameter a.

The memristor with threshold voltage is more suitable for storage and logic circuit, and its binary characteristic will improve the storage stability.

3 The Extensible Full Memristive Memory Cell

In order to solve the problem of sneak path current, and improve the storage density. In this paper, a pure memristive memory cell is proposed. As shown in Fig. 2, the memory cell is composed of a memristive switch and an extensible memristive cluster. The pure memristive switch can smoothly solve the sneak path current problem and improve storage density. The multi-value storage function is realized by the extensible memristive clusters. Theoretically, the memory cell can realize 2^N multi-value storage through flexible expansion. There are two ways to extend the memory cell, one is to add memristors in a memristive cluster, the other one is to add memristive clusters in a memory cell. The detailed discussion is as follows.

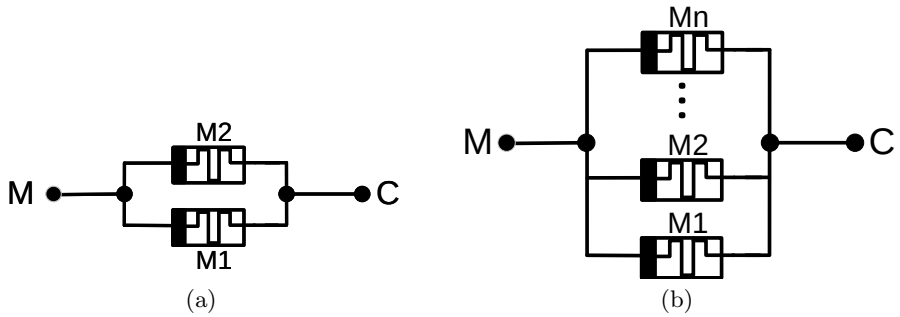


Fig. 3. (a)Proposed 2-bit memristive cluster with two memristors. (b) Extensible N-bit memristive cluster with n memristors.

3.1 Extensible Memristive Cluster Model

The proposed memristive cluster is a composite unit, as shown in Fig. 3, which includes N memristors with different threshold voltages and R_{on} and R_{off}, can realize N-bit storage. The memristive cluster can be extended as needed by adding memristors in the memristive cluster. The memristive cluster greatly increases the storage density of memristive memory.

Take the 2-bit memristive cluster as an example, as shown in Fig. 3(a), the terminal M is connected to the positive pole of the memristor, and the terminal C is connected to the other end. According to properties of memristor, when the input voltage is higher than the positive threshold V_{1thp}/V_{2thp}, the memristors M1 and M2 change to LRS R_{on1}/R_{on2}, when the input voltage is lower than the negative threshold V_{1thm}/V_{2thm}, the memristors M1 and M2 change to HRS R_{off1}/R_{off2} respectively. With the equation of parallel circuit $\frac{1}{R_{MC}} = \frac{1}{R_{M1}} + \frac{1}{R_{M2}}$, the total resistance of the proposed memristive cluster R_{MC} is $\frac{R_{M1}R_{M2}}{R_{M1}+R_{M2}}$. Therefore, R_{MC} can realize four different resistances under different resistances of M1 and M2, as shown in Table 1.

Table 1. The Resistance of the Proposed Memristive Cluster

$M2$	$M1$	R_{MC}
R_{off2}	R_{off1}	$\frac{R_{off1}R_{off2}}{R_{off1}+R_{off2}}$
R_{off2}	R_{on1}	$\frac{R_{on1}R_{off2}}{R_{on1}+R_{off2}}$
R_{on2}	R_{off1}	$\frac{R_{off1}R_{on2}}{R_{off1}+R_{on2}}$
R_{on2}	R_{on1}	$\frac{R_{on1}R_{on2}}{R_{on1}+R_{on2}}$

In order to better read and write the memristive cluster structure, M1 and M2 are set to meet the following two conditions:

i. $R_{off1} \gg R_{on1}$ and $R_{off1} \gg R_{on2}$ and $R_{off2} \gg R_{on1}$ and $R_{off2} \gg R_{on2}$

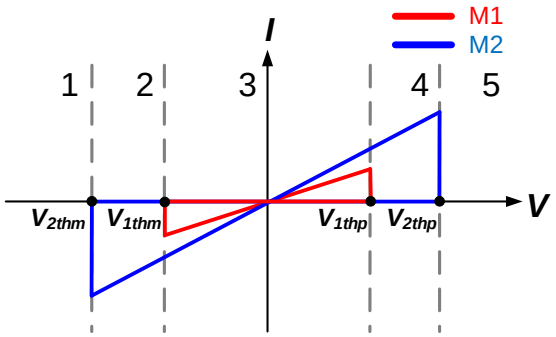


Fig. 4. I-V characteristic curves of M1 and M2.

ii. $\mid V_{2th} \mid > \mid V_{1th} \mid$

The current-voltage characteristic curves of M1 and M2 are shown in Fig. 4.

For easy understanding and calculation, suppose M1, M2 are satisfied with Eq. (6).

$$R_{off1} = R_{off2} = R_{off}, R_{on2} = R_{on}, R_{on1} = 2 \times R_{on} \tag{6}$$

The relationship between the resistances of the cluster and the resistance of M1, M2 is shown in Table 2.

Table 2. The Resistance of the Proposed Memristive Cluster

$M2$	$M1$	R_{MC}
R_{off}	R_{off}	$\frac{R_{off}}{2}$
R_{off}	$2R_{on}$	$\frac{2R_{on}R_{off}}{R_{off}+2R_{on}}$
R_{on}	R_{off}	$\frac{R_{on1}R_{off2}}{R_{on}+2R_{off}}$
R_{on}	$2R_{on}$	$\frac{2R_{on}}{3}$

3.1.1 Write

The control of the memristive cluster is determined by the voltage drop between ports M and C (V_{MC}). The current-voltage curves of M1 and M2 are divided into five intervals, as shown in Fig. 3. The relationship between the resistances of M1 and M2 and the interval of the input voltage are shown in Table 3.

This memristive cluster can be used to store two binary bits, assuming that M1 stores low bit and M2 stores high bit, we consider LRS R_{on} as logic 0, and HRS R_{off} as logic 1. The write operations to achieve four different states of memristive cluster are presented as follows.

Table 3. The Resistance Variation Under Different Input Voltage

Interval	$\boldsymbol{V_{MC}}$	$\boldsymbol{R_{M2}}$	$\boldsymbol{R_{M1}}$
1	$(-\infty, V_{2thm})$	R_{off}	R_{off}
2	(V_{2thm}, V_{1thm})	R_{ini2}	R_{off}
3	(V_{1thm}, V_{1thp})	R_{ini2}	R_{ini1}
4	(V_{1thp}, V_{2thp})	R_{ini2}	$2 \times R_{on}$
5	(V_{2thp}, ∞)	R_{on}	$2 \times R_{on}$

i. Logic 00 ($M2/M1 = R_{off2}/R_{off1}$) : V_{MC} in interval 1 of Fig. 3 is applied to the memristive cluster, and M1 and M2 are converted to R_{off2}/R_{off1}.

ii. Logic 01 ($M2/M1 = R_{off2}/R_{on1}$) : To write logic '01', two steps are required. First, V_{MC} in interval 1 is applied to the memristive cluster, both memristors are converted to R_{off}. Second, V_{MC} in interval 4 is applied to the memristive cluster, the state of M1 is changed to R_{on1}, and the state of M2 remains unchanged. Therefore, the states of M1/M2 change to R_{off2}/R_{on1}.

iii. Logic 10 ($M2/M1 = R_{on2}/R_{off1}$) : Similar to writing logic '01', writing logic '10' also need two steps. First, V_{MC} in interval 5 is applied to the memristive cluster, M1 and M2 are converted to R_{on1}/R_{on2}. Second, V_{MC} in interval 2 is applied to the memristive cluster, the states of M2/M1 are converted to R_{on2}/R_{off1}.

iv. Logic 11 ($M2/M1 = R_{on2}/R_{on1}$) : To writing '11' into the memristive cluster, V_{MC} in interval 5 is employed.

The writing operation can be summarized in Table 4.

Table 4. The Resistance Variation Under Different Input Voltage

Logic Value	**M2**	**M1**	**Interval of Voltage**
00	R_{off}	R_{off}	1
01	R_{off}	$2R_{on}$	1 4
10	R_{on}	R_{off}	5 2
11	R_{on}	$2R_{on}$	5

3.1.2 Read

According to Ohm's Law, when the read voltage V_r ($V_{1thm} < V_r < V_{1thp}$) is applied to the memristive cluster, the current of the terminal C is

$$I_c = \frac{V_r}{R_c} = \frac{V_r R_{M1} R_{M2}}{R_{M1} + R_{M2}}. \tag{7}$$

According to Eq. (6) and $R_{off} \gg R_{on}$, the cluster reading current is analyzed :

i. When $M2/M1 = R_{on2}/R_{on1}$ (logic '11'), $I_c = \frac{3V_r}{2R_{on}}$.

ii. When $M2/M1 = R_{on2}/R_{off1}$ (logic '10'), because $R_{off} \gg R_{on}$, then $I_c \approx \frac{V_r}{R_{on}}$.

iii. When $M2/M1 = R_{off2}/R_{on1}$ (logic '01'), because $R_{off} \gg R_{on}$, $I_c \approx \frac{V_r}{2R_{on}}$

iv. When $M2/M1 = R_{off2}/R_{off1}$ (logic '00'), $I_c = \frac{2V_r}{R_{off}}$, because $R_{off} \gg R_{on}$, compared to the above three cases, I_c can be approximately equal to zero.

Under this assumption, the amplitude of the current I_C has a good correspondence with the logic value of the memristive cluster, and can be distinguished well. The relations between the logic value of memristive cluster and the read current I_C are summarized in Table 5.

Table 5. The Reading Current Variation of the Cluster

$M2$	$M1$	R_{MC}	$R_{MC}*$	I_C	I_C*
R_{off}	R_{off}	$\frac{R_{off}}{2}$	$\frac{R_{off}}{2}$	$\frac{2U}{R_{off}}$	0
R_{off}	$2R_{on}$	$\frac{2R_{on}R_{off}}{R_{off}+2R_{on}}$	$2R_{on}$	$\frac{U}{2R_{on}}$	$\frac{1}{2} \times I$
R_{on}	R_{off}	$\frac{R_{on}R_{off}}{R_{on}+R_{off}}$	R_{on}	$\frac{U}{R_{on}}$	$1 \times I$
R_{on}	$2R_{on}$	$\frac{2R_{on}}{3}$	$\frac{2R_{on}}{3}$	$\frac{3U}{2R_{on}}$	$\frac{3}{2} \times I$

Furthermore, memristive cluster can be expanded by adding memristors, as shown in Fig. 3(b). As long as the memristive cluster has distinguishable 2^N resistances and the memristors have distinguishable threshold voltages, N bit multi-value storage can be realized, the storage density can be increased greatly.

3.2 Proposed Switching Circuit

In this part, a memristive switch for connecting memristive clusters is proposed. The memristive switch can replace the transistor, solve the problem of sneak path current, furthermore can reduce the area of the memory cell. As shown in Fig. 2, the switch consists of two identical memristors connected in reverse.

The switch circuit has three states: ON, OFF and NC. By applying two input voltages, V_A and V_B, and grounding port C, the voltage V_M can be determined by Kirchhoff current law,

$$\frac{(V_M - V_A)}{R_{Ma}} + \frac{(V_M - V_B)}{R_{Mb}} + \frac{V_M}{R_{MC}} = 0 \tag{8}$$

where $R_{Ma}, R_{Mb} \ll R_{MC}$,

$$V_M = (\frac{R_{Mb}}{R_{Ma} + R_{Mb}}) \times V_A + (\frac{R_{Ma}}{R_{Ma} + R_{Mb}}) \times V_B \tag{9}$$

V_A and V_B values would be +V, -V and 0. The voltage of V_{MA} and V_{MB} will change the resistance of switching memristor Ma and Mb, and then get the value of V_M according to Eq. (9), so as to achieve the effect of switching. Therefore, $V_{MA}(V_{MB})$ is required to be greater than the threshold $V_{tha}(V_{thb})$ of the switching memristor Ma(Mb). The state of the switch changes as follows.

3.2.1 $V_A = \mathsf{V}$, $V_B = \mathsf{V}$

According to (9), the node voltage should be

$$V_M = \frac{R_{Mb} + R_{Ma}}{R_{Ma} + R_{Mb}} \times V = V, \tag{10}$$

the state of the memristive switch is ON.

3.2.2 $V_A = \mathsf{-V}$, $V_B = \mathsf{-V}$

Similar to Case 1

$$V_M = \frac{R_{Mb} + R_{Ma}}{R_{Ma} + R_{Mb}} \times (-V) = -V, \tag{11}$$

the state of the memristive switch is ON.

3.2.3 $V_A = \mathsf{V}$, $V_B = \mathsf{0}$ or $V_A = \mathsf{0}$, $V_B = \mathsf{V}$

In these two cases, according to the applied voltage both switching memristers will reach the same state, either R_{off} or R_{on},

$$V_M = (\frac{R_{Mb}}{R_{Ma} + R_{Mb}}) \times V = (\frac{R_{on}}{R_{on} + R_{on}}) \times V = \frac{1}{2}V \tag{12}$$

or

$$V_M = (\frac{R_{Ma}}{R_{Ma} + R_{Mb}}) \times V = (\frac{R_{off}}{R_{off} + R_{off}}) \times V = \frac{1}{2}V. \tag{13}$$

$\frac{1}{2}V$ should not be over the minimum threshold voltage of any memrister in cluster, the state of memristive cluster would not be changed, so the switch is on the OFF state.

3.2.4 $V_A = \mathsf{-V}$, $V_B = \mathsf{0}$ or $V_A = \mathsf{0}$,$V_B = \mathsf{-V}$

Similar to case 3, the voltage of node M can be determined by

$$V_M = (\frac{R_{Mb}}{R_{Ma} + R_{Mb}}) \times (-V) = (\frac{R_{off}}{R_{off} + R_{off}}) \times (-V) = -\frac{1}{2}V \tag{14}$$

or

$$V_M = (\frac{R_{Ma}}{R_{Ma} + R_{Mb}}) \times (-V) = (\frac{R_{on}}{R_{on} + R_{on}}) \times (-V) = -\frac{1}{2}V. \tag{15}$$

Memristive switch would not be changed too, the switch is on the OFF state.

3.2.5 V_A = V, V_B = -V or V_A = -V, V_B = V

In both cases, the memristers Ma and Mb will be set to the same state.

$$V_M = (\frac{R_{Mb}}{R_{Ma}+R_{Mb}}) \times V + (\frac{R_{Ma}}{R_{Ma}+R_{Mb}}) \times (-V) \tag{16}$$

$$= (\frac{R_{on}}{R_{on}+R_{on}}) \times V + (\frac{R_{on}}{R_{on}+R_{on}}) \times (-V) = 0 \tag{17}$$

or

$$V_M = (\frac{R_{Mb}}{R_{Ma}+R_{Mb}}) \times (-V) + (\frac{R_{Ma}}{R_{Ma}+R_{Mb}}) \times V \tag{18}$$

$$= (\frac{R_{off}}{R_{off}+R_{off}}) \times V + (\frac{R_{off}}{R_{off}+R_{off}}) \times (-V) = 0. \tag{19}$$

Both of the results come to zero. So the memristive switch stay unchanged.

Based on the above analyses, port A and B are applied with V or -V synchronously, the state of switch turn on. For the other situations, the switch turn off. It is summarized in Table 6.

Table 6. The Resistance Variation Under Different Input Voltage

V_A	V_B	V_M	*Switch*	*State*
V	V	V	ON	
-V	-V	-V	ON	
V	0	$\frac{1}{2}V$	OFF	
0	V	$\frac{1}{2}V$	OFF	
0	-V	$-\frac{1}{2}V$	OFF	
-V	0	$-\frac{1}{2}V$	OFF	
V	-V	0	NC	
-V	V	0	NC	

3.3 Proposed Pure Memristive Multi-Value Memory Cell

Based on the above analyses, the proposed memory cell can avoid sneak path current by pure memristive switch, realize 2^N multi-value storage by memristive cluster, the composition of the pure memristor greatly improves the storage density of the proposed memory cell. Next, the operation of the proposed memory cell is given. The input voltages are applied to port A and port B of Fig. 2. Port C is the output port, and the output current can show the state of the memristive cluster.

3.3.1 Writing operation

By grounding node C, the memristive cluster can be written through changing the input voltage of port A and B. For example, when we want to write '01', ground port C and set the input voltage of port A and B as V_w in interval 1. So V_{MC} equals to

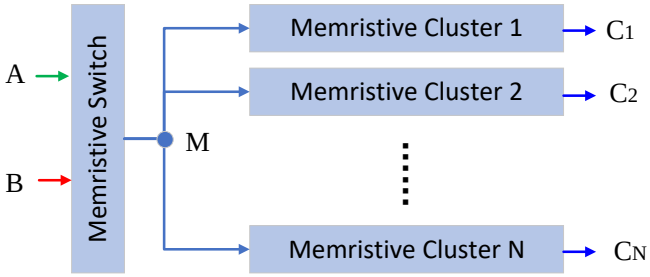


Fig. 5. The extended proposed memory cell of N memristive clusters.

V_w and both R_{M2}/R_{M1} is changed to R_{off}. Next, change V_w to voltage in interval 4, and R_{M2}/R_{M1} are changed to R_{on2}/R_{ini1}. As R_{M2}/R_{M1} is R_{on2}/R_{off1}, the logic of the memristive cluster is '01'.

The total writing operations of a memory cell are shown in Table 7.

Table 7. Writing Operations and Reading Output of Memristive Cluster

logic	**Write Input-voltage Interval**	**Read Output-current**
00	1	0
01	1 4	$\frac{1}{2} \times I$
10	5 2	$1 \times I$
11	5	$\frac{3}{2} \times I$

3.3.2 Reading Operation

According to the former analyses, the current flowing from node C reflects the value of the memristive cluster. In order to avoid changing the value of the memristive cluster, the input voltage should be less than the minimum threshold (in the interval 3 of Fig. 4), but over the threshold of the switching memristors. By judging the value of the current, the state of the cluster emerges.

Assuming Eq. (6) is satified, and applying the read voltage V_r to the cluster, the corresponding relationship between the output current and the resistance states of memristive cluster are shown in Table 7.

The proposed memory cell can also be extended by adding the memristive clusters. As shown in Fig. 5, When expanded to N memristive clusters, the entire memory cell has $N \times 2 = M$ memristors. The proposed memory cell could store M bit values and 2^M logical values. The read-write principle of the proposed memory cell is to control the voltage difference of V_{MCi} each memristive cluster. When the voltage value of node M is determined, the voltage value of V_{Ci} can be set to perform read and write

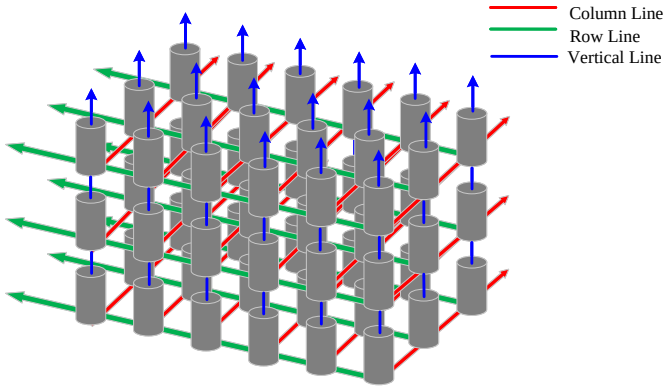


Fig. 6. 3D crossbar-array model.

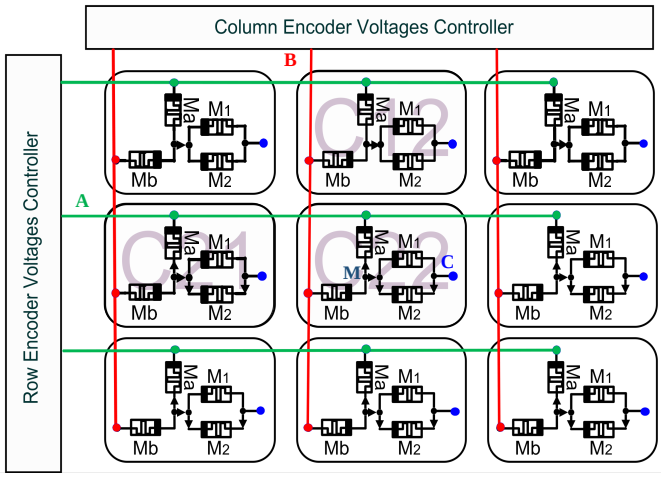


Fig. 7. The structure of one layer.

on particular memristive cluster, and N memristive clusters can be read and write simultaneously.

4 3D Crossbar Array Architecture Design

In this part, a 3D crossbar array storage architecture is proposed based on the above pure memristive memory cell. The architecture has the characteristics of high storage density, fast reading and writing speed, and low power consumption. In addition, the use of 3D structure and memristive switch also greatly improves the problem of sneak path current. The 3D crossbar array has $N \times N \times N$ ports, as shown in Fig. 6. The row and column ports in each layer are the input ports. The vertical ports are the output ports, whose potentials are always kept at zero. Take one layer in the 3D crossbar-array as an example for reading and writing analysis, as shown in Fig. 7, details as follow.

4.1 Writing Operation

When writing a cell, the writing voltage is applied to the row and column lines of the cell. As shown in Fig. 7, suppose write C22, the input voltage is required to interface A and B of C22, output port C of C22 is grounded. All other non-operating cells and wires are grounded. So in C22, $V_M = V_{MC} = V_W$, writing-voltage writes memory cell. When C22 is input different writing-voltage, the memory cell can be written to different logic values.

For other non-write cells, only the memory cells stay in the same row or same column with C22 maybe affected. The remaining cells remain unchanged, because both of their inputs are zero. If the cell is in the same row as C22, its port A is written in V_w and port B is grounded. Based on case 3 and 4 in Section B, the switch is turned off. The node M voltage of the non-write cell in the same row is $\frac{V_W}{2}$ (in interval 3), which will not change the resistance of the non-write cells, the resistance of the clusters keep unchanged. The cells in the same column as C22 are similar. Port A gets zero and port B gets V_W, $V_M = \frac{V_W}{2}$ (in interval 3). The switch is also in the OFF state, and the memory cell would not be changed. Based on the above analyses, write mode does not modify the stored value of the non-write cell.

4.2 Reading Operation

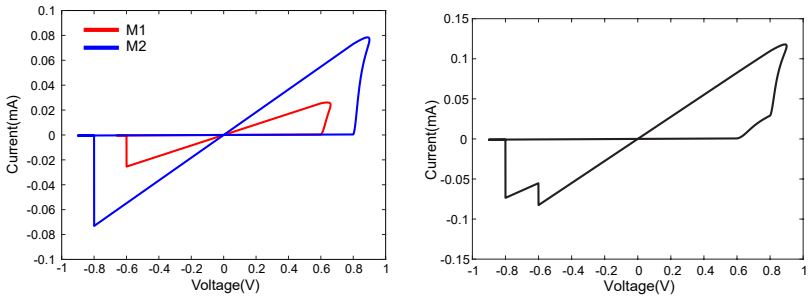
Same as writing operation, reading voltage pulses are input to the row and column lines of the reading cell, each port C of cells can output the judging current I_C, which can reflect on the stored values of the memory cell.

Sneak path current should also be considered in reading operations. The node M voltage of the cell in the same row or column is $|\frac{V_r}{2}| < |V_r| < |V_{1th}| < |V_{2th}|$ (in interval 3), which will not modify the stored value of the non-read cell. The cells that are not in the same column can be readed at the same time, and the read current is amplified through the output terminal. At the same time, since the output current of the cells in the same layer is not directly related to each other, the output current of the cells in the same layer and same row or same column has little influence on each other.

In a 3D crossbar array, when a writing operation is performed, the different layers can be executed simultaneously, but the vertical ports must always be grounded. However, in a reading operation, different layers should be avoided from reading the same row or column at the same time. So two cells with different layers, different rows, and different columns can be read simultaneously. Of course, cells in the same layer can also be read simultaneously.

5 Simulation and Results

In this part, the feasibility of the proposed pure memristive 3D crossbar array is verified with PSpice. A memristive cluster with two memristors is selected. When a memristor cluster has four resistance states, four resistance states and four reading currents should have a certain degree of differentiation. For easy understanding, the memristor in the memristive cluster satisfies Eq. (6), the resistance and current values have good multiple relations, which is convenient for analysis and calculation, conducive to the operation of computational circuits.



(a) (b)

Fig. 8. (a) Current-voltage characteristic of the memristor M1 and the memristor M2. (b) Current-voltage characteristic of the memristive cluster.

5.1 Pure Memristor Memory Cell Simulation

Table 8 is the parameters of memristor M1, M2 and switching memristor Mk in the memory cell. The current-voltage characteristic curves of M1 and M2 are shown in Fig. 8. Compared with Fig. 3, Fig. 8(a) shows the memristor M1 and M2 in the simulation, and the hysteresis loop reflects the two value characteristic. Fig. 8(b) shows the I-V curve of the memristive cluster.

Table 8. Simulation Parameters for Proposed Memory Cell

Parameters	***M1***	***M2***	***Mk***
α_{off}	1	1	1
α_{on}	3	3	3
$V_{off}(V)$	-0.8	-0.6	-0.09
$V_{on}(V)$	0.8	0.6	0.09
$R_{off}(\Omega)$	2×10^6	2×10^6	900
$R_{on}(\Omega)$	1×10^4	2×10^4	100
$k_{off}(m/s)$	2×10^6	2×10^6	2×10^6
$k_{on}(m/s)$	-3×10^7	-3×10^7	-2.8×10^7
$D(nm)$	10	10	10
$\omega_{off}(nm)$	10	10	10
$\omega_{on}(nm)$	0	0	0

5.1.1 Simulations of Writing

The writing process of '00' and '11' takes one step, while '01' or '10' takes two. Fig. 9(a) and Fig. 9(b) show the situation of writing '11' and '10' respectively, both R_{M1} and R_{M2} were written successfully.

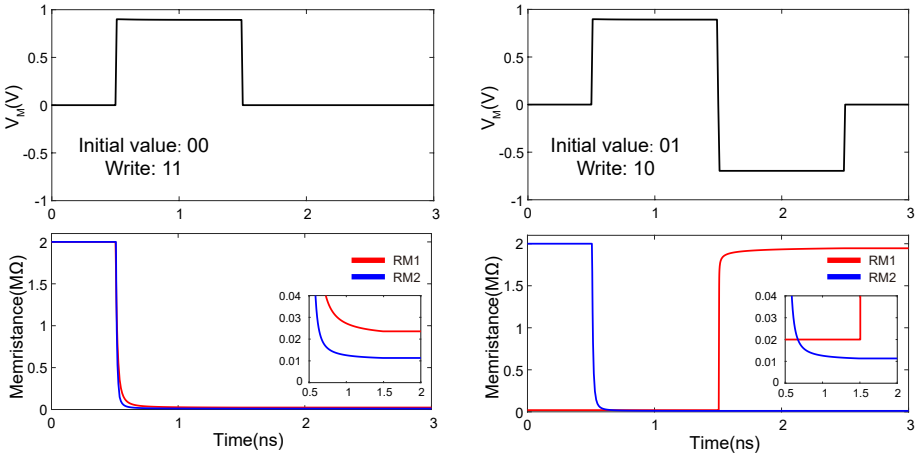


Fig. 9. Two cases of writing logic to a pure memristive cell. (a) Write logic '11' in C22 when the initial value is logic '00'. (b) Write logic '10' in C22 when the initial value is logic '01'.

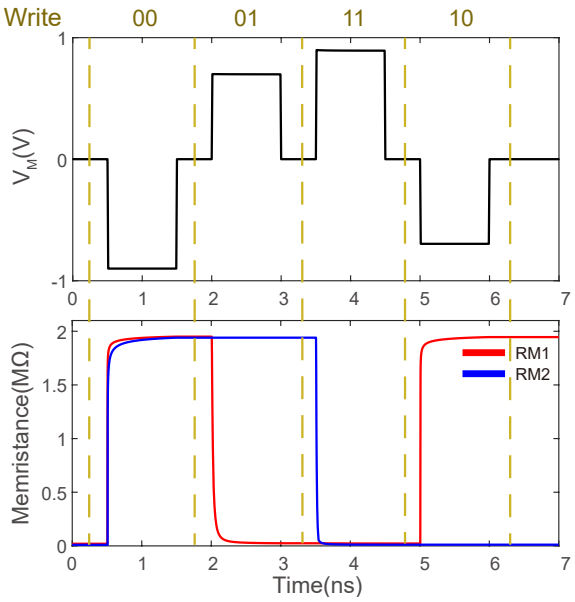
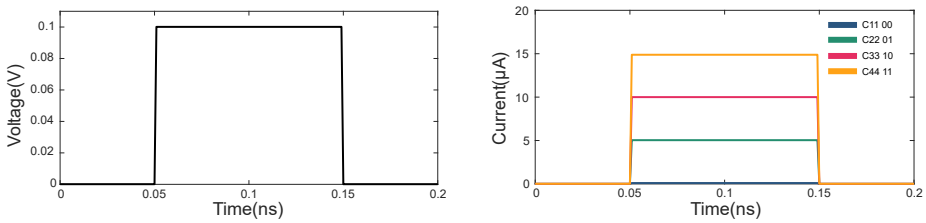


Fig. 10. The change of voltage and resistance as' 00 ', '01', '11' and '10' are continuously written to a single cell.

In addition to a single write to a single cell, multiple writes to the same cell are observed for resistance changes as shown in Fig. 10. Because the first step of writing '01' is to write '00', writing '10' needs to write '11' first, so the simulation design continuously writes '00'→'01'→'11'→'10', and the average writing of each logical value requires only one step. The simulation result shows that the resistance state and change of the cluster are consistent with the theoretical analysis.



(a) (b)

Fig. 11. (a) The reading voltage is a pulse voltage. (b) The reading current of a memory cell when the stored value in 00,01,10,11.

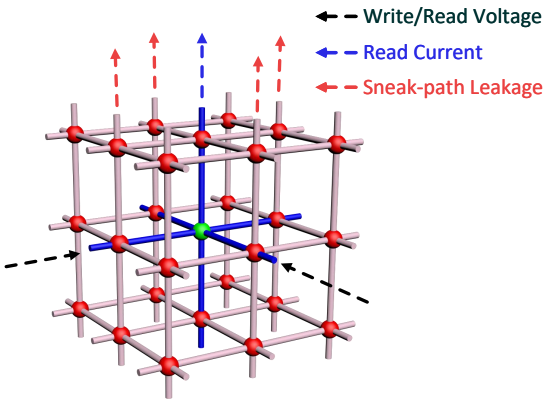


Fig. 12. The sneak path current in 3D crossbar-array.

5.1.2 Simulations of Reading

In the result of reading simulation, the frequency of reading voltage is higher than F_{TH}[29], and the value of reading voltage is lower than the minimum threshold voltage of M1 and M2. Fig. 11 shows the result of reading four different memory values simultaneously. The reading voltage is a pulse voltage of 0.1V for a time of 100ps, as shown in Fig. 11(a).

It can be obtained from Fig. 11(b) that the ratio of reading current values under the four logical values is $I_{00} : I_{01} : I_{10} : I_{11} = 0 : 1 : 2 : 3$. In fact, the current ratio needs not be in accordance with this ratio, as long as there is a degree of differentiation.

5.2 The Impact of the Sneak Path Current

The sneak path current affects the stored value of the non-operating cell, and increase the power consumption. Fig. 12 shows the possible effect of sneak path current in the 3D crossbar array.

In section IV, it is theoretically analyzed that the non-operating cell would not be changed during the writing and reading process of the 3D crossbar array structure. In the structure shown in Fig. 7, when C22 is written, the most vulnerable cells are the same column non-operational cell C12 and the same row non-operational cell C21. To reduce the effect of sneak path current and reduce power consumption, port C of

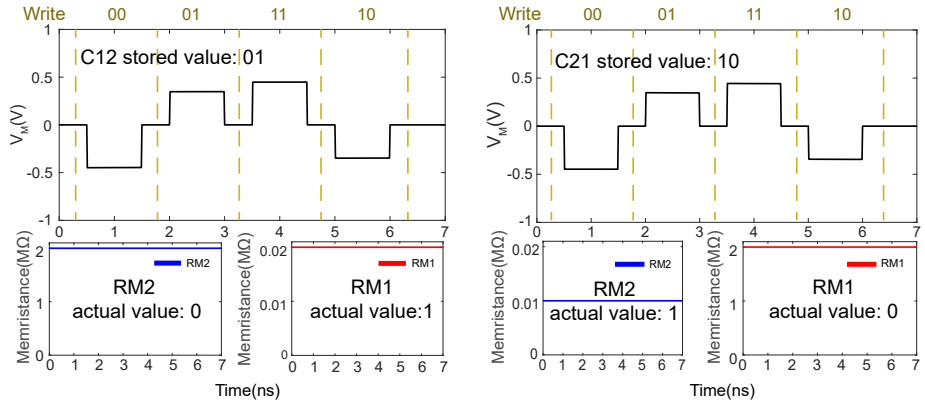


Fig. 13. The effect of sneak path current on a non-operating cell when four different logical values are written continuously to C22. (a) When the initial value of the non-operating cell C12 is '01', the voltage change of node M and the actual resistance change. (b) When the initial value of the non-operating cell C21 is '10', the voltage change of node M and the actual resistance.

Table 9. Comparison of Density With Previous Work

Designs	1T1M [37]	1T2M [32]	2D1M [38]	4M1M [39]	2M1M [29]	This Work
Density $(\boldsymbol{Gbt/cm^2})$	1.6	3.2	1.2	50	80	125

non-operating cells in the same row or column can be floated or connected to a large resistor.

When C22 is continuously written with four different logic values, the experiment simultaneously observes the resistance changes of non-operating cell C12 in the same column and C21 in the same row. The results are shown in Fig. 13. It can be seen that under the continuous change of resistance, the resistances of the two cells are almost unaffected.

5.3 Comparison

5.3.1 Density

Currently, there are two different memristive memory cells. One is hybird memory cell, which is composed of memristors and CMOS components. For example, transistors are used as switching components in 1T1M and 1T2M structures. However, the combination with CMOS components will greatly reduce the density and cannot reflect the advantages of memristors as nano devices. According to Reference[29], approximated device density the proposed architecture is compared with previous works in Table 9, the density of 2D1M memory cell is only $1.2Gbt/cm^2$, 1T1M memory cell is $1.6Gbt/cm^2$, and 1T2M is $3.2Gbt/cm^2$. The other one is pure memristive memory cell, such as 4M1M and 2M1M memory cells, the density can reach $50Gbt/cm^2$ and $80Gbt/cm^2$ respectively. In our work, the density of the proposed pure memristive

memory cell can reach $125Gbt/cm^2$, which is significantly higher than others structures. Furthermore, extensible memristive clusters allow more logical values to be stored in a memory cell, and the size of a memory cell can be controlled as needed. When N memristors are employed in a memory cell, the density of the crossbar-array is approximately $\frac{250N}{(2+N)}Gbt/cm^2$.

5.3.2 Speed

The reading/writing speed is an important property for a memory. The proposed 3D crossbar array memory is compared with the most recent memristive memory structures, as shown in Table 10. In this work, one step of writing operation requires 1ns, two steps requires 2ns, but each writing operation can write at least two bits, which is shorter than the other works. Each reading operation can read at least two bits, so the reading time is also shorter than other works. Furthermore, when there is more than one cluster in a memory cell, multiple clusters can perform simultaneous writing or reading operations. Compared with other circuits, it is possible to write multiple values at the same time. In the analysis of the simulation part, crossbar array can achieve a simultaneous reading of non-column cells.

Table 10. Comparison of Operating Time and Voltage

Memory Cell	**1T1M** [**40**]	**1T2M** [**31**]	**4M1M** [**39**]	**2M1M** [**29**]	**This Work**
Write Time	1.33ns	3ns	1.269ns	1.11ns	1-2ns
Read Time	-	0.5ns	0.25ns	0.2ns	0.1ns
Write Voltage	0.9V	$\leq 4V$	0.9V	0.9V	$\leq 0.9V$
Read Voltage	-	$< 0.5V$	0.1V	0.1V	0.1V

5.3.3 Power Consumption

The operating voltage will affect the power consumption. The reading voltage and writing voltage of the proposed memory cell are lower than those of the circuits with CMOS components, as shown in Table 10. Fig. 14 shows the power consumption of writing different values at different initial values, which is at least three orders of magnitude less than the 1T2M circuit.

6 Conclusion

This paper proposes a 3D memristive crossbar array nonvolatile memory. The memory cell is composed of a memristive switch and an extensive memristive cluster, which can store N-bit store according to the cluster settings. The pure memristive properties of the memory cell and the use of extensible clusters greatly improve the store density. Furthermore, memristive switch and 3D crossbar-array significantly alleviate the sneak path problem. Compared with the existing memristive nonvolatile memory, the proposed 3D crossbar array nonvolatile memory has higher reading/writing

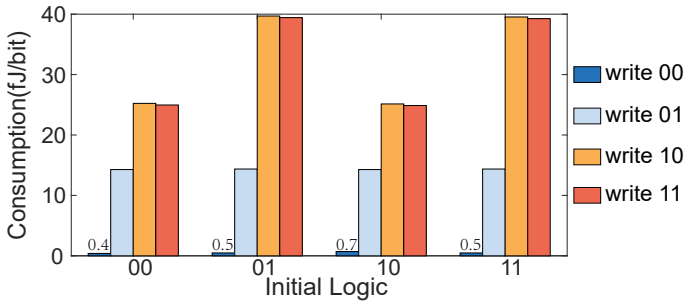


Fig. 14. The consumption of writing logic.

speed, higher storage density, and lower power consumption. The simulation results show store density of the proposed 3D crossbar array nonvolatile improves 56%, and the reading speed improves 50%. In addition, the storage density can be further increased to realize n-bit storage by expanding the memristive clusters or expanding the memristive memory cells with clusters. As a basic unit, memristive clusters can not only be applied to the design of memory and realize multi-value storage, but also can be applied to the design of circuits such as memristive logic and memristive neuromorphism, has a broad application space.

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