A W-Band SPDT Switch with 15 dBm P1dB in 55-nm Bulk CMOS

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***Abstract*—Power-handling capability of bulk CMOS-based single-pole double-throw switch operating in millimetre-wave and sub-THz region is significantly limited by the reduced threshold voltage of deeply scaled transistors. A unique design technique based on impedance transformation network is presented in this work, which improves 1-dB compression point, namely P1dB, without deteriorating other performance. To prove the presented solution is valid, a 70-100 GHz switch is designed and implemented in a 55-nm bulk CMOS technology. At 90 GHz, it achieves a measured P1dB of 15 dBm, an insertion loss of 3.5 dB and an isolation of 18 dB. The total area of the chip is only 0.14 mm^2.**

Index Terms—Bulk CMOS, millimetre-wave (mm-wave), RFIC, RF switch, W-band.

I. Introduction

The single-pole double-throw (SPDT) switch has been widely used in time-division multiplexing (TDD) systems. To minimise the design cost, extensive effort has been made for CMOS-based design, especially bulk CMOS. Several breakthroughs have been achieved for low-loss and high-isolation switch design in bulk CMOS technology [1]-[15]. However, the limited P1dB remains to be a fundamental issue. It is noted that although the P1dB can be significantly improved by using negative bias voltages along with stacked transistors, this approach is mainly available for SOI- and SiGe-based designs, not usually suitable for bulk CMOS-based ones. Among different design approaches for millimetre-wave (mm-wave) switch, it is still preferred to use the shunt-connected structure with quarter-wavelength transmission lines (TLs) for bulk CMOS-based design for the sake of design simplicity. Although CMOS-based SPDT switch could achieve an excellent power-handling capability at low frequency [1]-[3], most of the bulk CMOS-based switches operating at 60+ GHz can only provide a P1dB around 10 dBm [6], [11]-[13]. Therefore, there is a strong demand to further enhance P1dB of a mm-wave/sub-THz switch designed in bulk CMOS.

In this paper, an impedance transformation network (ITN)-based design technique is proposed for W-band SPDT switch. Although this technique has been used at sub-GHz [1], it has not been used for mm-wave switch design before. The rest of this paper is organized as follows. In Section II, the insight of the proposed design technique will be analysed. In Section III, the implementation of the designed switch will be discussed. The measurement results are given in Section IV and the conclusions are finally drawn in Section V.

II. Insight of Impedance Transformation Network for Switch Design

The drawback of using shunt-connected switching transistors has been very well documented in the literature [16]. The main concern here is the limited P1dB due to transistor scaling. To effectively improve the power-handling capability of a SPDT switch, it is necessary to understand the relationship among different design specifications, especially P1dB, IL and ISO. The P1dB limitation of a switch using shunt-connected switching n-type field-effect transistor (nFET) along with quarter-wavelength TLs can be estimated using the equation given below [16],

$$P_{1dB\_min} = \left(\sqrt{2}V_{TH}\right)^2 \times \frac{1}{Z_o} \quad (1)$$

where Zo is the load/source impedance that is typically 50 Ω. As shown in (1), to improve P1dB, two approaches can be used. One is to increase the value of V_{TH} and another is to reduce the value of Zo. As previously mentioned, the threshold voltage is a physical parameter that is related to the selected technology node and thus cannot be simply changed from a circuit design perspective. This also indicates the challenge for switch design in deep-scaled CMOS technology.

On the other hand, the value of Zo can be potentially controlled using an ITN. The key idea is that instead of using a standard 50-Ω impedance for internal matching, two ITN units can be inserted between the load/source terminals and the drain terminal of the switching nFET. The conceptual block diagram of this arrangement is given in Fig. 1. As mainly symmetrical SPDT switch design is discussed in this work, only half of the SPDT switch is shown. The internal impedance looking into the ITN unit from the drain terminal of a nFET is expressed in (2) [1],

$$Z_{Int} = \frac{Z_o}{n} \quad (2)$$

where n is a ratio between the standard 50-Ω impedance and Z_{Int} that is transferred by the ITN unit. Based on the different specifications of the design, the value of n can be selected accordingly. Substituting (2) into (1), the expression of P1dB is rewritten as,

* Manuscript received XXX; revised XXXX; accepted XXXX.

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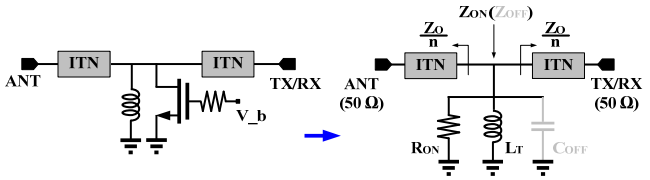


Fig. 1. The simplified half-circuit model of the presended design.

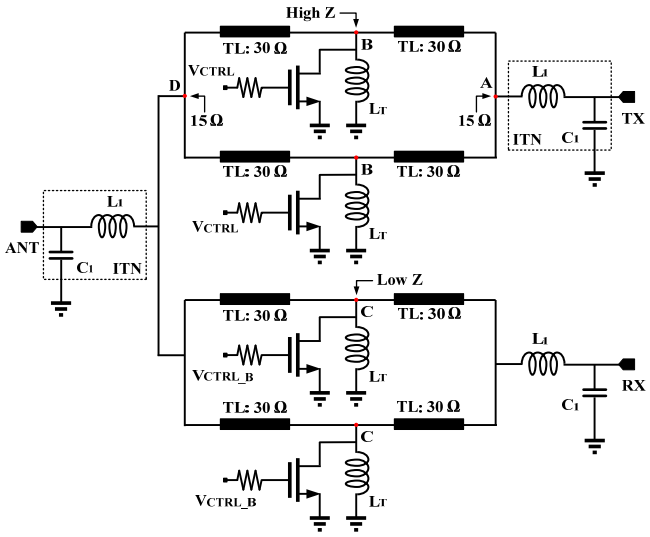


Fig. 2. The simplified circuit schematic of symmetrical SPDT switch using the proposed ITN-based technique.

$$P'_{1dB\_min} = \left(\frac{2V_{TH}}{\sqrt{2}}\right)^2 \times \frac{n}{Z_o} \quad (3)$$

According to (3), if the value of n is greater than 1, the power-handling capability of the switch can be improved. However, the impedance mismatch between the internal impedance, Z_{Int} and the impedance looking into the drain terminal of the switching nFET may also have an impact on other performance, such as IL and ISO. This impact can be calculated by using the S_{21} parameter under different conditions and expressed in (4a) and (4b), respectively.

$$IL_{Imp\_mismatch} = \frac{2}{2+\frac{Z_o}{Z_{OFF}}\times\frac{1}{n}} \quad (4a)$$

$$ISO_{Imp\_mismatch} = \frac{2}{2+\frac{Z_o}{Z_{ON}}\times\frac{1}{n}} \quad (4b)$$

As shown in (3) and (4), although using a large value of n is preferred for an improved P1dB and IL, it could deteriorate the ISO of the switch. Thus, there is a design trade-off between different design specifications and thus the value of n must be carefully selected. Moreover, the ideal loss-less passive network does not exist in practice. Thus, the additional IL due to parasitic loss effects of non-ideal ITN units also needs to be taken into considerations. The additional IL caused due to limited Q-factor of passive devices can be expressed as,

$$IL_{Lossy\_Q} = -20 \times Log_{10}(1+\frac{Q}{Q_c}) \quad (5)$$

where $Q = \sqrt{n-1}$, Q_c is the Q-factor of the ITN unit. In general, the value of Q_c is around 10 for the used technology, if a simple LC network is used. For an optimized design, the value of n is selected to be 1.7, which gives an approximately 30-Ω internal impedance.

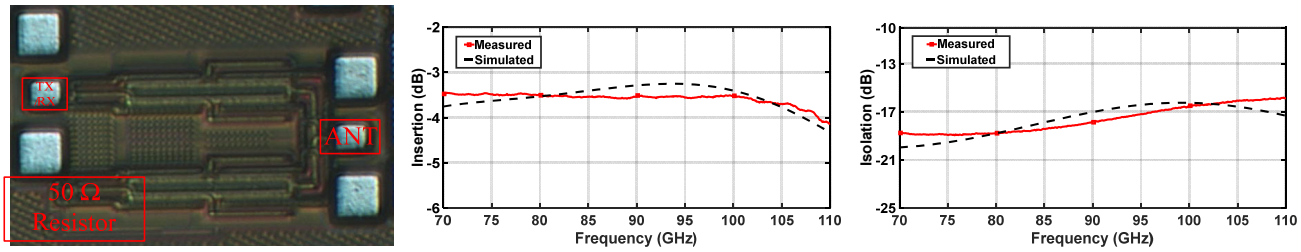
III. Design of the Presented SPDT Switch using ITN Technique

To apply the presented technique for SPDT switch design, a possible solution is proposed and its simplified schematic is given in Fig. 2. When an RF signal is injected into the TX port, it goes through an ITN unit first, which is formed by an LC network that consists of L_1 and C_1. Using the ITN unit, the common-mode impedance looking into node A is transferred from 50 to 15 Ω. Then, the RF signal is divided into two paths. Each path consists of two 30-Ω quarter-wavelength TLs, a switching nFET and a lumped inductor, L_T. At TX mode, the two nFETs are switched off. Thus, a shunt LC network is built by the parasitic capacitance (known as C_{OFF}) and the L_T. By looking into the ground, the constructed network can produce a required high impedance at node B. Meanwhile, the two nFETs at the RX branch are switched on, which results in a low impedance at node C. Consequently, the RF signal will not flow into the RX branch at TX mode. Once the RF signal passes through the switching section, the two divided signals are combined at node D and the impedance is transferred back to 50 Ω at ANT port. It must be noted that the power-combining network used at the input of the designed switch may not be necessary if a power-combined PA is used. For such a case, the power-splitter network and the ITN unit could be co-designed with each power cell used for the PA. As a result, the ITN unit could be embedded into the power-combining network to further minimize the overall insertion loss and die area of the switch.

To verify the presented concept, a 55-nm bulk CMOS technology is chosen. The size of switching nFETs is carefully determined by using the classical figure-of-merit (FoM) – the product of R_{ON} times C_{OFF}. An optimized performance can be achieved, while the value of nFET's width is 50 µm. Furthermore, the inductor L_T is required to form a resonator with the switching nFET. By using a grounded inductor at the designed frequency, the L_T can be determined as 170 pH. This nFET-microstrip-line-based LC tank will provide 480-Ω and 9-Ω impedances, respectively when the nFETs are switched off and on from a schematic simulation. The thickness of the TL is 1.325 µm and the width is 10 µm. As the TLs with different characteristic impedance are used in this design, depending on the required impedance, the gaps between the TL and ground wall can be effectively adjusted. Based on the EM simulated results, a 4 µm and a 10 µm gap are used for the 30-Ω and 50-Ω TL, respectively.

IV. Measurement Results

To validate the designed switch, it is fabricated in a 55-nm bulk CMOS technology. Without the pads, the die size of this design is only 0.3 × 0.44 mm^2. The die microphotograph is



(a) (b) (c)

Fig. 3. Measurement results, (a) die microphotograph, (b) insertion loss, and (b) isolation.

TABLE I

PERFORMANCE SUMMARY OF THE DESIGNED SPDT SWITCHES WITH THE OTHER STATE-OF-THE-ART DESIGNS

REF.	f_c (GHz)	Insertion loss (dB)	Isolation (dB)	P1dB (dBm)	Area (mm^2)	Tech. (nm)	Circuit Structure
[5]	50-94	3.3	27	15	0.24	90 CMOS	Travelling wave with shunt-connected FETs
[11]	58-85	1.8/4*	22	10	0.015	65 CMOS	Transformer with shunt-connected FETs
[12]	60-110	3-4	25	10.5	0.3	90 CMOS	λ/4-TL with shunt-connected FETs
[13]	94-110	4.2	25	n/a	n/a	65 CMOS	λ/4-TL with shunt-connected FETs
[14]	85-95	3.2 (TX) 3.6 (RX)	>25 (TX) >20 (RX)	>19.5 (TX)	0.26	55 CMOS	Ring resonator with shunt-connected FETs
THIS WORK	**70-100**	**3.5**	**18**	**15**	**0.14**	**55 CMOS**	**Impedance transformation network with shunt-connected FETs**

Note: *at 85 GHz.

given in Fig. 3(a). The performance of the designed switch is characterised through on-wafer measurement using a pair of Ground-Signal-Ground (G-S-G) probes along with a 2-port vector network analyser (VNA). It should be noted that as the designed switch is symmetrical in terms of RX and TX branches, one of these branches are terminated using an on-chip 50-Ω load, so that a 2-port VNA can be used for the measurements. A similar approach has also been used in [16]. In this case, the isolation can be only measured between ANT port and RX/TX port rather than from RX port to TX port. The measured and simulated results of IL and ISO are presented in Fig. 3(b) and 3(c). On-chip de-embedding structures are used to remove the impact on S-parameters due to G-S-G pads. As illustrated, at 90 GHz, the insertion loss and the isolation are better than 3.5 dB and 18 dB, respectively. To further verify the power-handling capability of the designed SPDT switch, power measurements are also conducted. The measured P1dB and the insertion loss (under large-signal condition) of the designed switch, are given in Fig. 4. As shown, a P1dB of approximately 15 dBm is achieved. The performance comparisons between the presented symmetrical SPDT switch and the other state-of-the-art designs are given in Table I. For fair comparisons, only the ones that are implemented in bulk CMOS and operated at W-band are considered here. As can be seen, the achieved P1dB for most of the state-of-the-art CMOS-based designs are limited to be about 10 dBm for 65-nm process and below. By using the presented approach, the P1dB of this design has been improved by approximately 5 dB without significantly deteriorating other performances in terms of IL and ISO.

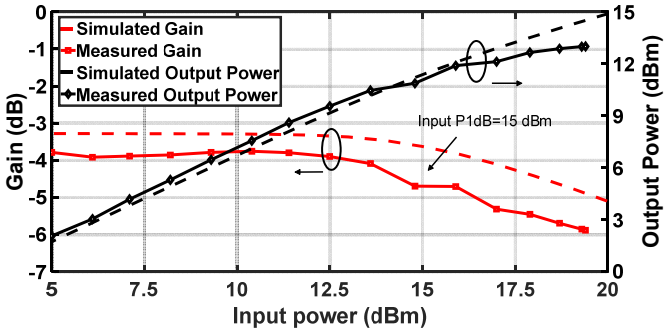


Fig. 4. Measured P1dB of the designed switch.

V. CONCLUSION

A passive-inspired approach for bulk CMOS-based mm-wave/sub-THz SPDT switch design has been presented in this work. It utilises an impedance transformation network to improve P1dB without deteriorating other key specifications. The designed SPDT switch is implemented in a 55-nm bulk CMOS technology. At 90 GHz, it achieves a measured P1dB of 15 dBm, an insertion loss of 3.5 dB, and an isolation of 18 dB. Therefore, it can be concluded that the presented approach is feasible in practice.

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