Experimental Investigation of Decoupled Discontinuous PWM Strategies in Open-End Winding Induction Motor Supplied by a Common DC-link

Mohammed Zerdani, Sid Ahmed El Mehdi Ardjoun, Houcine Chafouk, Senior *Member, IEEE,* and Mouloud Denaï.

***Abstract*— Currently open-end winding induction motors fed by a dual inverter (OEWIM-DI) present an innovative approach to enhance the performance of modern electric drive systems; such as electrical vehicles and electric aircraft applications. However, the dual inverter topology requires a proper switching control strategy to enable the OEWIM drive to fully achieve its performance. This work aims to investigate experimentally the impact of different Decoupled Discontinuous Pulse Width Modulation (DDPWM) control strategies on the performance of the OEWIM-DI supplied by a common DC-link. The criteria performance adopted in this study are: (i) the Total Harmonic Distortion (THD) of the current and voltage, (ii) the Zero Sequence Voltage (ZSV), (iii) the Common Mode Voltage (CMV), and (iv) the dual inverters losses. The various DDPWM control schemes for the 1.5 kW OEWIM-DI motor drive are implemented on a dSPACE 1104 board and the results are compared with the popular and widely used Space-Vector PWM (SVPWM) strategy. From the results, it can be concluded that the optimised DDPWM technique gives the best performance. This technique has reduced the CMV by one level and reduce the losses by 50% while having the same THD and ZSV obtained with the SVPWM technique.**

***Index Terms*— Open-end winding induction motor, Common DC-link, dual inverter, decoupled discontinuous PWM, Efficiency, common mode voltage, zero sequence component, THD. Optimization.**

I. I. INTRODUCTION

Variable-speed electric drives (VSD) are extensively used in various industrial applications such as manufacturing and automotive transportation. The current advances in power electronics devices and converter topologies have resulted in a significant improvement of variable-speed electric drive performance, efficiency, compactness, and cost.

Indeed, a key feature in the development of a high-performance, and high-efficiency variable-speed drive is the design of an optimal control scheme for the combined power electronics stage and the electrical machine. However, this combination has some impacts on the performance of VSDs in terms of power quality and energy efficiency [1][2]. This is currently an area of ongoing research and development both in academia and industry. These research areas can be classified into three categories: (i) active and passive filtering, (ii) power electronics re-configuration, (iii) improvement of PWM control strategies. The use of filters can be considered as a classical solution and has many drawbacks including high-cost, bulky and increased energy consumption [3][4]. Hence, most current research focuses on power electronics re-configuration and improvement of the control scheme.

Several configurations have been proposed for the integration of power electronics with electrical machines in VSD applications and among these is the one proposed by H. Stemmler and P. Guggenbach [5]. The idea of this structure is that instead of coupling the stator in a star/delta configuration, the authors proposed to open the neutral point of the stator windings, so that the windings are fed by two inverters (one inverter for each side). This structure is called; an Open-End Winding Motor with Dual Inverters (OEWM-DI). This structure has attracted a lot of attention recently and has been used in a wide range of applications, including electric vehicles [6][7], control systems in aircraft [8] and marine electric engines [9]. This is due to its advantages such as simplicity of the power circuit [10], absence of neutral point fluctuations [11], fault tolerance [12], reduced DC bus voltage [7] and wider speed range operation [13] [14]. Nevertheless, this structure has some disadvantages including the overcharging of low voltage capacitor caused by unequal DC-link voltages in the case of two isolated DC supplies [15], the Zero-Sequence Voltage (ZSV) because of the direct connection of the two inverters [16], and the presence of a Common Mode Voltage (CMV) due to the high frequency switching of the inverters' switches [17][18][19].

Overcharging can damage the capacitor and generate undesirable harmonics in the motor phase voltage [15], [20]. To eliminate the overcharging effects, the authors

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in [21] and [22] proposed adding rectifiers on the auxiliary inverter side but this structure is too complex and costly. In [23], the authors proposed a carrier-based unequal reference-sharing algorithm based on PWM, which inherently regulates the overcharging voltage. However, this method assigns unwanted voltage steps to the decoupled modulation, resulting in a deteriorated output voltage waveform. In [15], the authors proposed an equal-duty SVPWM and a proportional-duty SVPWM to overcome the DC-link capacitor overcharging problem. The main disadvantage of this technique is that it limits the number of vectors that can be used for modulation. The authors in [24], used a dual inverter topology fed by a DC-bus floating capacitor to power electromechanical drives. This configuration eliminates the need for an isolation circuit and avoids overcharging problems. The problem with this design is how to maintain a constant floating capacitor voltage due to its fluctuating nature [24]. Therefore, the most economical and simple solution to avoid overcharging problems is supplying the OEWIM by a common DC bus source. However, this configuration is still too critical because it creates the ZSV [25].

The ZSV problem creates a Zero-Sequence Current (ZSC) which results in triple current harmonics [26]. This current is detrimental to the motor windings, and causes increased copper losses and circuit saturation. Several attempts have been made to eliminate this voltage in the OEWIM-DI configuration. In [2], the authors proposed to add a coil in series with the motor windings. The authors in [27] proposed to add auxiliary switches, and in [28], one side of the OEWIM was supplied with a three-level inverter and the other side with a two-level inverter. However, these solutions involve additional hardware which increases the costs. Therefore, the best cost-effective solution would be to design appropriate control rules to eliminate the ZSV. For example, in [29] the authors proposed to decouple the control between the two inverters to create a phase-shift of 120° between the first inverter's voltages and the second inverter's voltages. The authors in [30] and [31] used the same method but with a phase shift of 180°, then they proposed to use either even or odd synchronous vectors. In [32], two approaches were proposed to freely select the switching states of the dual inverters. However, these approaches could neither eliminate the ZSV nor limit the switching of the inverters' switches. The authors in [33] and [11] proposed a technique called Decoupled Sample-Averaged Zero-Sequence Elimination (DSAZE) to force the ZSV to zero and minimise the switching losses. A new technique called Synchronous Off-Line Optimum PWM, which is specially designed for low switching frequency has been proposed in [34].

The CMV problem, on the other hand, creates common mode currents between the stator phase windings and the ground. This tends to erode the bearing surfaces, thus reducing their lifetime [35]. In addition, these currents do not participate in the conversion of electromechanical energy and contribute to the heat losses in the motor [36]. To overcome CMV problems, several solutions have been proposed in the literature. For example, the use of coils [37], filters [38], or additional switching branches [39]. However, these solutions require additional costly hardware. Other researchers have proposed to reduce the CMV by improving the control rules. The authors in [40] proposed a PWM technique that avoids the selection of zero vectors. In [19], a new hybrid PWM technique that allows the inverters to work independently has been proposed.

The major drawback of most previous research is that the energy efficiency of the dual inverters is not considered. This structure is gaining popularity in electric vehicles, where the main challenge is increasing the vehicle's autonomy. To address the energy efficiency problem and close this gap, this paper proposes to use the decoupled discontinuous PWM (DDPWM) technique which is well known for improving the energy efficiency of static converters. In the literature, there are several types of DPWM strategies, including DPWM Min, DPWM Max, DPWM1, DPWM2, DPWM3, DPWM4 [41] and optimised DPWM [42].

It is worth noting that some of these DDPWM techniques have already been investigated for the OEWIM-DI motor drive by several authors. In [43], the authors proposed to apply the DDPWM1 strategy when the OEWIM-DI is fed by two isolated sources. The results showed that the proposed technique solved the overcharging problem and reduced the ZSV levels. However, the authors did not discuss the efficiency and the CMV. Discontinuous decoupled SVPWM methods with a 180° shifting angle for the OEWIM-DI system fed by two isolated sources have been investigated in [44]. The results showed that the proposed technique solved the problem of overcharging and improved the CMV, but it did not improve the efficiency.

Unlike all previous research on the improvement of the OEWIM-DI's performance by means of control strategies, which only deals with one problem at a time, i.e., either the THD, CMV, ZSV, power losses or overcharging, this paper presents a comprehensive experimental evaluation of all DDPWM techniques for controlling the OEWIM-DI system supplied by a common DC bus. A comparative study of the motor drive performance with respect to the THD, ZSV, CMV and overall losses of the system in the frequency range from 20 Hz to 50 Hz is also presented.

The remaining of the paper is organised as follows: Section 2 summarises the main problems of the OEWIM-DI motor drive. Section 3 presents the DDPWM techniques and their applications to OEWIM-DI. Section 4 presents power loss optimization using the Genetic Algorithm. The experimental results and discussions are included in Section 5. Finally, the conclusion of this paper and future research directions are summarised in Section 6.

II. Problem Statement and Proposed Solution

In the literature, there are three different types of configurations of dual inverter fed OEWIM namely: (i) common DC bus, (ii) DC bus with a floating capacitor and (iii) two isolated DC bus. In our study, the common DC bus configuration is adopted, as shown in Fig.1. This structure overcomes overcharging problems without adding extra hardware [45], [24]. This structure includes two two-level

inverters, denoted by inverter i (main inverter) and j (auxiliary inverter), respectively.

The voltage vectors in a $\alpha\beta$ reference frame for each inverter (V_i and V_j)) are given as follows [46]:

$$V_i = \sqrt{\frac{2}{3}} V_{dc}(S_{i1} + \gamma\, S_{i3} + \gamma^2\, S_{i5}) \quad (1)$$

$$V_j = \sqrt{\frac{2}{3}} V_{dc}\left(S_{j1} + \gamma\, S_{j3} + \gamma^2\, S_{j5}\right) \quad (2)$$

Where $\gamma = e^{j\frac{2\pi}{3}}$, V_{dc} is the DC bus voltage, S_{i1}, S_{i3}, S_{i5} and S_{j1}, S_{j3}, S_{j5} are the switch states of the two inverters i and j respectively.

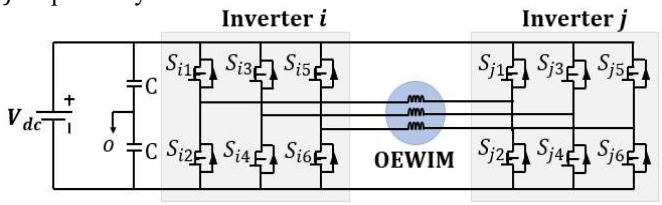
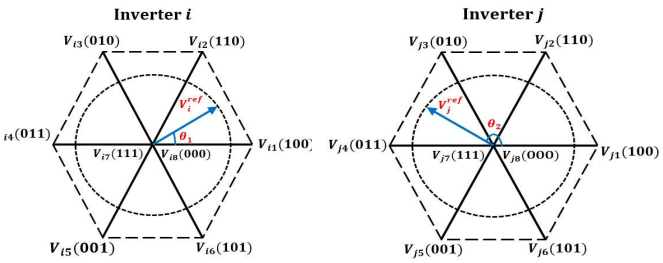


Fig. 1. Power supply configuration of the OEWIM-DI with a single DC bus.

Fig. 2 shows the hexagon of the eight voltage vectors (six active vectors and two zero vectors for each inverter) generated by equations (1) and (2). Where "1" and "0" denote the on or off state of the inverter switches, respectively.



(a) (b)

Fig. 2. Voltage space vector diagram of each inverter: (a) inverter i, (b) inverter j.

Therefore, the dual inverter configuration gives 64 ($2^3 \times 2^3$) possible switching combinations distributed across 19 distinct spatial locations, as shown in Fig.3 (this configuration is similar to a three-level inverter). Thus, the voltages v_{ij} that feed the OEWIM-DI are obtained by subtracting the voltages V_i and V_j of each inverter as follows [47]:

$$v_{ij} = v_i - v_j \quad (3)$$

According to equation (3), if both ends are supplied with the same voltage, the motor will not rotate. Therefore, to make the motor rotate, a phase angle α should be introduced into the voltages of one of the inverters. However, the choice of the phase shift angle α ($\alpha = \theta_2 - \theta_1$, see Fig.2) produces different combinations of switching vectors which affect the performance of the motor drive (effect of CMV and ZSV).

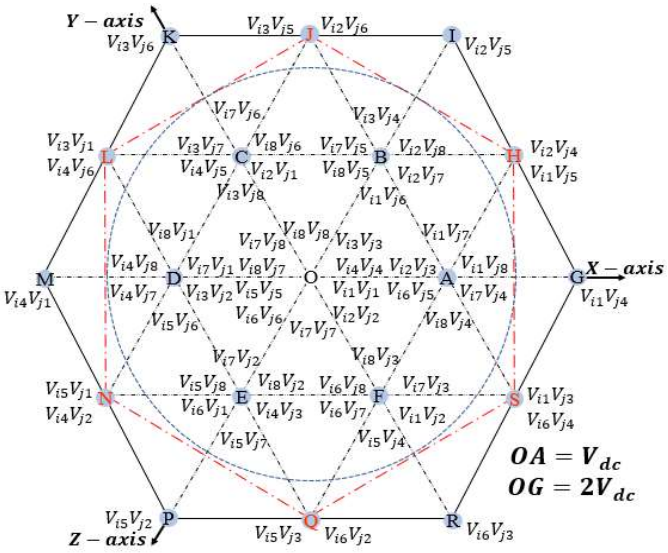


Fig. 3. Voltage space vector diagram for dual inverters.

Therefore, the reference voltages of inverters i and j can be expressed as follows:

$$\begin{cases} v_{ia}^{ref} = \mathrm{V}\sin(\omega t) \\ v_{ib}^{ref} = \mathrm{V}\sin\left(\omega t - \frac{2\pi}{3}\right) \\ v_{ic}^{ref} = \mathrm{V}.\sin\left(\omega t + \frac{2\pi}{3}\right) \end{cases} \quad (4)$$

$$\begin{cases} v_{ja}^{ref} = \mathrm{V}\sin(\omega t + \alpha) \\ v_{jb}^{ref} = \mathrm{V}\sin\left(\omega t - \frac{2\pi}{3} + \alpha\right) \\ v_{jc}^{ref} = \mathrm{V}\sin\left(\omega t + \frac{2\pi}{3} + \alpha\right) \end{cases} \quad (5)$$

Where, V is the peak value of the voltage, ω is the electrical pulsation ($\omega = 2\pi f$, f is the grid frequency).

In the system shown in Fig.1, the CMV for each inverter can be calculated as follows [48]:

$$V_{cmv_i} = \frac{S_{i1} + S_{i3} + S_{i5}}{3} V_{dc} \quad (6)$$

$$V_{cmv_j} = \frac{S_{j1} + S_{j3} + S_{j5}}{3} V_{dc} \quad (7)$$

Thus, for the dual inverter, the CMV is defined as [19]:

$$V_{cmv} = \frac{V_{cmv_i} + V_{cmv_j}}{2} \quad (8)$$

$$V_{cmv} = \frac{(S_{i1} + S_{i3} + S_{i5}) + (S_{j1} + S_{j3} + S_{j5})}{6} \quad (9)$$

As mentioned previously, the OEWIM-DI may suffer from a ZSC caused by the ZSV; this is due to the dual inverters being supplied by the same DC bus voltage source. This ZSC implies a high current/voltage THD, increased losses, overheating and vibrations in the machine. The ZSV can be expressed in terms of the CMV of each inverter (V_{cmv_i} and V_{cmv_j}) as follows [49]:

$$V_{zsv} = V_{cmv_i} - V_{cmv_j} \quad (10)$$

$$V_{zsv} = \frac{(S_{i1} - S_{j1}) + (S_{i3} - S_{j3}) + (S_{i5} - S_{j5})}{3} V_{dc} \quad (11)$$

The different levels of ZSV obtained with the 64 switching combinations using equation (11) are presented in Table I.

TABLE I. ZSV LEVEL VOLTAGE FOR OEWIM-DI.

Vectors Combinations	ZSV level
$V_{i8}V_{j7}$	$-V_{dc}$
$V_{i8}V_{j4}$, $V_{i8}V_{j6}$, $V_{i8}V_{j2}$, $V_{i5}V_{j7}$, $V_{i3}V_{j7}$, $V_{i1}V_{j7}$	$-2V_{dc}/3$
$V_{i8}V_{j5}$, $V_{i8}V_{j3}$, $V_{i5}V_{j4}$, $V_{i3}V_{j4}$, $V_{i8}V_{j1}$, $V_{i5}V_{j2}$, $V_{i3}V_{j6}$, $V_{i3}V_{j2}$, $V_{i4}V_{j7}$, $V_{i1}V_{j4}$, $V_{i1}V_{j6}$, $V_{i1}V_{j2}$, $V_{i6}V_{j7}$, $V_{i2}V_{j7}$, $V_{i5}V_{j6}$	$-V_{dc}/3$
$V_{i1}V_{j3}$, $V_{i6}V_{j4}$, $V_{i2}V_{j4}$, $V_{i1}V_{j5}$, $V_{i3}V_{j5}$, $V_{i2}V_{j6}$, $V_{i4}V_{j6}$, $V_{i3}V_{j1}$, $V_{i5}V_{j1}$, $V_{i4}V_{j2}$, $V_{i5}V_{j3}$, $V_{i6}V_{j2}$, $V_{i7}V_{j7}$, $V_{i8}V_{j8}$, $V_{i1}V_{j1}$, $V_{i5}V_{j5}$, $V_{i4}V_{j4}$, $V_{i3}V_{j3}$, $V_{i2}V_{j2}$, $V_{i1}V_{j1}$	0
$V_{i5}V_{j8}$, $V_{i3}V_{j8}$, $V_{i4}V_{j5}$, $V_{i4}V_{j3}$, $V_{i1}V_{j8}$, $V_{i2}V_{j5}$, $V_{i6}V_{j3}$, $V_{i2}V_{j3}$, $V_{i7}V_{j4}$, $V_{i4}V_{j1}$, $V_{i6}V_{j1}$, $V_{i2}V_{j1}$, $V_{i7}V_{j6}$, $V_{i7}V_{j2}$, $V_{i6}V_{j5}$	$V_{dc}/3$
$V_{i4}V_{j8}$, $V_{i6}V_{j8}$, $V_{i2}V_{j8}$, $V_{i7}V_{j5}$, $V_{i7}V_{j3}$, $V_{i7}V_{j1}$	$2V_{dc}/3$
$V_{i7}V_{j8}$	V_{dc}

Table I shows that there are twenty different combinations of voltage vectors to obtain the null ZSV. These combinations are located at the vertices of the hexagon HJLNQS and two combinations at the centre of the hexagon (see Fig.3) [50].

Since in this work a 120° shift angle has been used in the reference voltages[51], then the combinations used will reduce to ($V_{i1}V_{j3}$, $V_{i3}V_{j5}$, $V_{i5}V_{j1}$, $V_{i2}V_{j4}$, $V_{i4}V_{j6}$, $V_{i6}V_{j2}$, $V_{i7}V_{j7}$ and $V_{i8}V_{j8}$). Although these vector combinations result in a zero ZSV, the presence of CMV is inevitable. Table II shows the four possible CMV levels. To reduce this CMV level, we propose to use DPWMs techniques which will be presented in the next section.

TABLE II. ZSV AND CMV LEVELS.

Vectors Combinations	ZSV level	CMV level
$V_{i8}V_{j8}$	0	$-V_{dc}/2$
$V_{i1}V_{j3}$, $V_{i3}V_{j5}$, $V_{i5}V_{j1}$	0	$-V_{dc}/6$
$V_{i2}V_{j4}$, $V_{i4}V_{j6}$, $V_{i6}V_{j2}$	0	$V_{dc}/6$
$V_{i7}V_{j7}$	0	$V_{dc}/2$

III. APPLICATION OF THE DISCONTINUOUS PWM TECHNIQUE

The basic principle of the DPWM technique is to saturate the reference voltage for a period, thus maintaining an inverter leg switched-off for that time. This results in a switching discontinuity, hence its name "discontinuous PWM" [52]. This reduces the number of switching operations and reduces the switching losses [41]. Since during each time there are only two phases are switched on, the method is also called two-phase PWM [53].

To create this discontinuity, a saturation voltage must be added to the reference voltages. Equation (12) defines the general model of this saturation voltage. It should be noted that the addition of the saturation voltage does not affect the average value of the reference voltages, but it will impose a reduced DC bus voltage.

$$v_{sat} = \frac{V_{dc}}{2}(2\mu - 1) - \mu V_{max} + (\mu - 1)V_{min} \quad (12)$$

Where, V_{max} and V_{min} represent the highest and lowest levels of the recommended reference signals at a given time and μ is the distribution ratio. The range of possible values for μ is from 0 to 1. For different values of μ, various continuous and discontinuous modulation signals can be generated.

The new reference voltages of inverters i and j can therefore be expressed as follows:

$$\begin{cases} v_{ia}^{ref*} = v_{ia}^{ref} + v_{sat} \\ v_{ib}^{ref*} = v_{ib}^{ref} + v_{sat} \\ v_{ic}^{ref*} = v_{ic}^{ref} + v_{sat} \end{cases} \quad (13)$$

$$\begin{cases} v_{ja}^{ref*} = v_{ja}^{ref} + v_{sat} \\ v_{jb}^{ref*} = v_{jb}^{ref} + v_{sat} \\ v_{jc}^{ref*} = v_{jc}^{ref} + v_{sat} \end{cases} \quad (14)$$

If $\mu = 0.5$, equation (12) becomes:

$$v_{sat} = -\frac{1}{2}V_{max} - \frac{1}{2}V_{min} \quad (15)$$

In this case, the switching strategy that can be generated is the SVPWM. Fig.4(a) shows the signal of this technique.

If $\mu = 0$, the saturation voltage is defined as:

$$v_{sat} = -\frac{V_{dc}}{2} - V_{min} \quad (16)$$

In this case, there is only one 120° saturation in a period and the PWM technique hence obtained is called DPWM Min as shown in Fig.4(b).

If $\mu = 1$, this technique is also saturated by 120° in one period and the equation of the saturation voltage becomes:

$$v_{sat} = \frac{V_{dc}}{2} - V_{max} \quad (17)$$

This technique is called DPWM Max, its modified modulating signal and their relationship with μ are shown in Fig.4(c).

If μ varies between 0 and 1, there are four different techniques that can be generated: DPWM1, DPWM2, DPWM3 and DPWM4. These techniques are generated according to the saturation angle φ. As shown in Fig.4(d), Fig.4(e), Fig.4(f). and Fig.4(g) the saturation angle in the case of DPWM1 is 60° at the centre of the half-periods, and for DPWM2 the saturation is 30° ahead of the voltage maximum, while for DPWM3 a saturation angle of 120° is divided into four equal sections and for DPWM4 the saturation is lagging the maximum voltage by 30°.

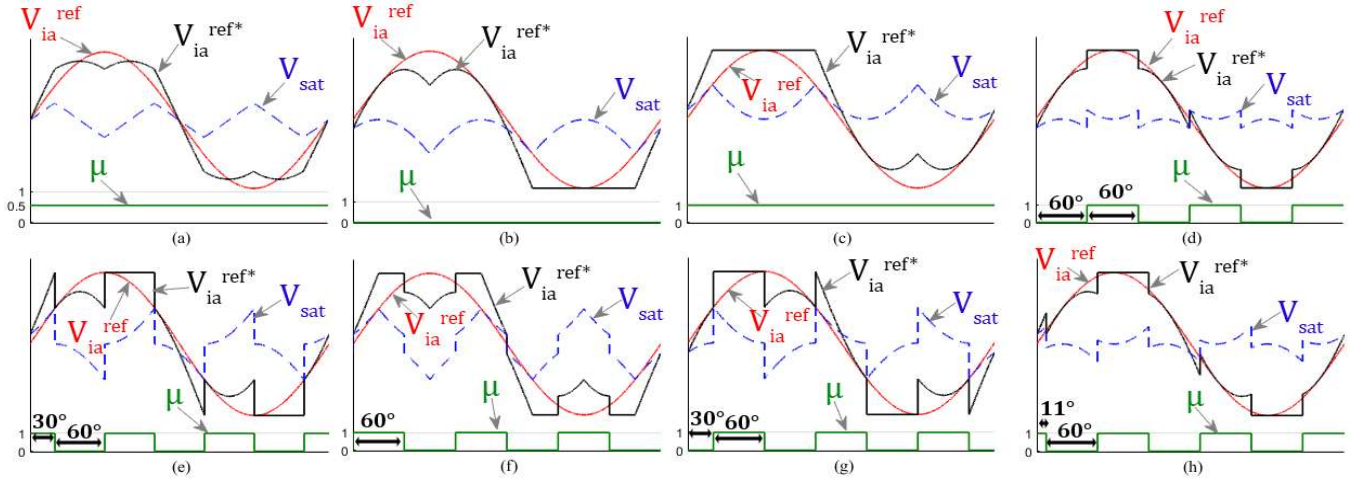


Fig. 4. Modified modulating waveforms and their relation with the μ and the angle saturation of the techniques of: (a) SVPWM, (b) DPWM Min, (c) DPWM Max, (d) DPWM1, (e) DPWM2, (f) DPWM3, (g) DPWM4, (h) Optimised DPWM.

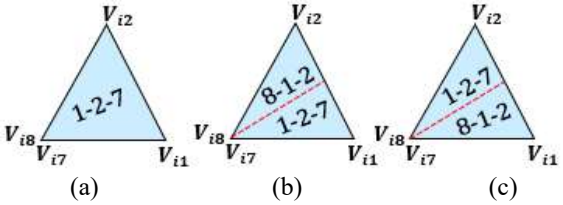


Fig.5. Sequence voltage vectors applied in sectors I for the conventional two-level inverter: (a) DSVPWM, (b) DDPWM1, (c) DDPWM3

TABLE III. SWITCHING SEQUENCES OF DIFFERENT DDPWM ON THE SECTORS 1 AND THEIR EFFECT ON THE CMV LEVELS.

PWM methods	Sector 1		CMV levels eliminated
	Inv. i	Inv. j	
DDPWM Min	$V_{i8}V_{i1}V_{i2}$	$V_{i8}V_{i3}V_{i4}$	$-V_{dc}/2$
DDPWM Max	$V_{i1}V_{i2}V_{i7}$	$V_{i3}V_{i4}V_{i7}$	$V_{dc}/2$
DDPWM1	$V_{i1}V_{i2}V_{i7}$	$V_{i3}V_{i4}V_{i7}$	$V_{dc}/2$
	$V_{i8}V_{i1}V_{i2}$	$V_{i8}V_{i3}V_{i4}$	$-V_{dc}/2$
DDPWM2	$V_{i1}V_{i2}V_{i7}$	$V_{i3}V_{i4}V_{i7}$	$V_{dc}/2$
DDPWM3	$V_{i8}V_{i1}V_{i2}$	$V_{i8}V_{i3}V_{i4}$	$-V_{dc}/2$
	$V_{i1}V_{i2}V_{i7}$	$V_{i3}V_{i4}V_{i7}$	$V_{dc}/2$
DDPWM4	$V_{i8}V_{i1}V_{i2}$	$V_{i8}V_{i3}V_{i4}$	$-V_{dc}/2$
Optimised DDPWM	$V_{i1}V_{i2}V_{i7}$	$V_{i3}V_{i4}V_{i7}$	$V_{dc}/2$
	$V_{i8}V_{i1}V_{i2}$	$V_{i8}V_{i3}V_{i4}$	$-V_{dc}/2$

The classical DSVPWM technique uses the conventional sequences $V_{i8}V_{i1}V_{i2}V_{i7}$ and $V_{i7}V_{i2}V_{i1}V_{i8}$ alternately in sector 1, as shown in Fig. 5(a). With DPWM1, the sector will be divided into two identical parts of 30° each. In the interval from 0° to 30°, DPWM1 will use the sequences $V_{i1}V_{i2}V_{i7}$ and $V_{i7}V_{i2}V_{i1}$ alternately, so V_{i8} is zero and between 30° to 60°, V_{i7} will be zero in this case as shown in Fig.5(b). So DDPWM1 will cancel the $-V_{dc}/2$ level of CMV in the first region and the $V_{dc}/2$ level in the second region. When DDPWM3 is used the result will be opposite to that of DDPWM1 technique as shown in Fig.5(c), in other words, V_{i7} is zero in the first range, and V_{i8} will be zero in the second range. The results obtained from the CMV, when applying the different DDPWM techniques, are summarised in Table III. From the results, it can be noticed that whichever DDPWM technique is used, the CMV will be reduced by only one level of $V_{dc}/2$ as compared to the DSVPWM technique.

IV. POWER LOSS OPTIMIZATION

Typically, in PWM-power electronics converters, losses are of two types: conduction losses (P_c) and switching losses (P_{sw}) (switching losses during the $t_{sw,on}$ on and $t_{sw,off}$ off transition).

In [54], the authors gave the expressions for P_{sw} and P_c for the dual-inverter system.

$$P_{sw} = \left[\frac{1}{2} v_{sw} i_{sw} (t_{sw,on} + t_{sw,off})\right] \times f_{sw} \quad (18)$$

$$P_C = \frac{v_{on} i_{on} T_{on}}{T_{sw}} \quad (19)$$

Where v_{sw} is the voltage clamped by the IGBT in the off state (i.e. V_{dc}), v_{on} is the voltage dropped in the on state, $i_{sw} = i_{on}$ is the current circulated in the IGBT in the on state, , f_{sw} is the switching frequency, $T_{sw} = 1/f_{sw}$ is the switching period.

As explained in the previous section, the DDPWM techniques are dependent on the saturation angle φ. And since the losses are directly related to the current, which is also a function of φ [55], the saturation angle φ can be optimised to minimise the losses.

Due to the stochastic relationship between the saturation angle φ and the losses in the system (see Fig.6), Genetic Algorithm (GA) optimisation is more appropriate to find the optimal value of φ. For GA, a population of 100 randomly selected individuals was used, the crossover probability, mutation probability and generation gap were set to 0.75, 0.06, and 10% respectively. This technique is repeated for a φ that varies in the interval [0°; 90°]. The switching loss equation P_{sw} was used as a fitness function. The flowchart of Fig.7 describes the GA-based optimisation of φ.

For the calculation of the switching and conductive losses as a function of φ the following has been considered:

- The characteristics of the IGBT-SKM150GB123D module are considered for the calculation of the conductive losses.

- $t_{sw,on} = 1.5\mu s$ and $t_{sw,off} = 3\mu s$.
- The calculations are carried out using MATLAB/Simulink software.
- In order for the loss calculation to be accurate enough, the simulation step size was set to $1\mu s$.
- The simulation model presented in [56] is used.

A plot of the switching and conductive losses as a function of φ is shown in Fig.6.

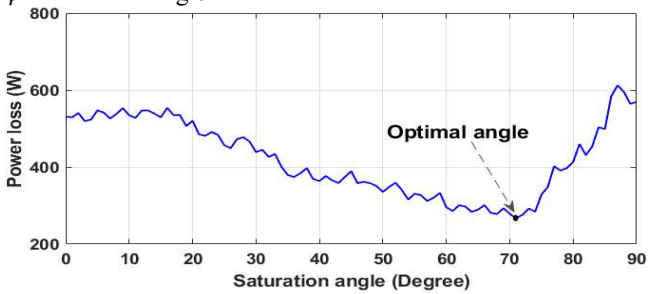


Fig. 6. Dual inverters power losses versus the saturation angle.

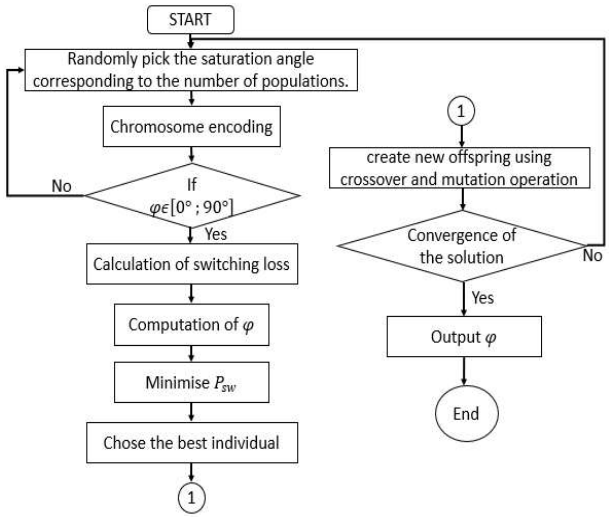


Fig.7. Flowchart for calculating the optimum saturation angle.

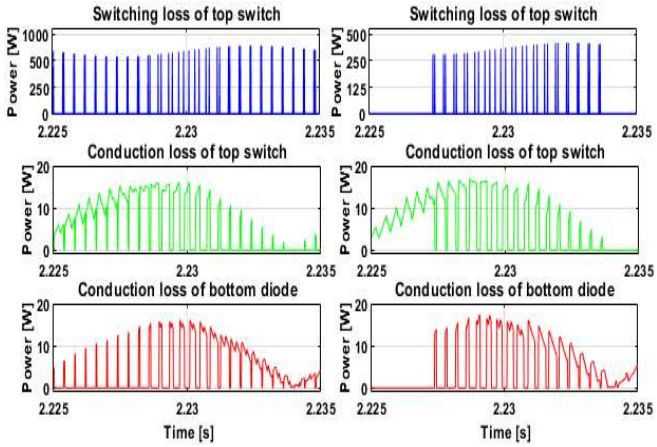


Fig.8. The switching and conduction losses of the top switch and the bottom antiparallel diode of: (a)DSVPWM, (b) ODDPWM.

Using GA under these conditions, it was found that the optimal angle which minimizes the losses is 71° (Fig.6 confirms this result). Finally, the impact of the switching strategies on power losses is illustrated in Fig.8. This figure shows the switching and conduction losses of the top switch and the bottom antiparallel diode for both the DDSVPWM and optimised DDPWM (ODDPWM) approaches.

V. Experimental Results

To assess the impact of different DDPWM techniques on the OEWIM-DI performance, a series of tests were carried out on an experimental test bench. The first test consisted of applying a 50 Hz reference voltage (modulation index $m = v^{ref*}/V_{dc} = 1$) and then measuring the different performances in terms of the THD, ZSV, CMV and losses. The second test consisted of repeating the first test when the OEWIM-DI is operated in open-loop with scalar control (V/f = constant). In this test the modulation index was varied from 0.5 to 1 (25 Hz – 50 Hz). The method used for generating the gate signals from the voltage references is illustrated in Fig.9.(a). The results obtained with the different DDPWM strategies are then compared with those of the DSVPWM technique which is widely used in VSDs.

The experimental setup used in this study consists of a 1.5 kW OEWIM (230V, 50Hz) mechanically coupled with a DC machine used as a mechanical load. This OEWIM is driven by two inverters connected to the same DC bus source (326 V) and without filters. A dSPACE 1104 board was used to generate the control signals with a switching frequency of 2.5 kHz. The sampling frequency was set to 20 kHz. A digital oscilloscope was used to visualize the various signals (voltages and currents waveforms, control signals, CMV and ZSV), and a power analyser was used to measure the THDs of voltages and currents and the energy efficiency of the inverters. The schematic diagram of the experimental setup is depicted in Fig.9.

Figs. 10 and 11 show the voltage and current waveforms, CMV, ZSV, and the switching states respectively obtained in the first test for various DDPWM strategies. The results of this test are summarised in Table IV. The values obtained in the second test are plotted in Figs.12, 13 and 14.

From the results obtained in the first test, the following observations can be given:

- The ZSV is completely eliminated regardless of the control strategy used. This is due to the decoupling control of both inverters created by the 120° phase-shift. These results validate those presented in Section II (Table II).
- The CMV level is reduced by one level with all DDPWM techniques as compared to the DSVPWM technique. These results confirm that they are in a good agreement with the previous results shown in Table. III (Section III).
- The losses in the inverters are also reduced with all DDPWM techniques. The DDPWM Min, DDPWM2, DDPWM3 and DDPWM4 techniques were able to reduce

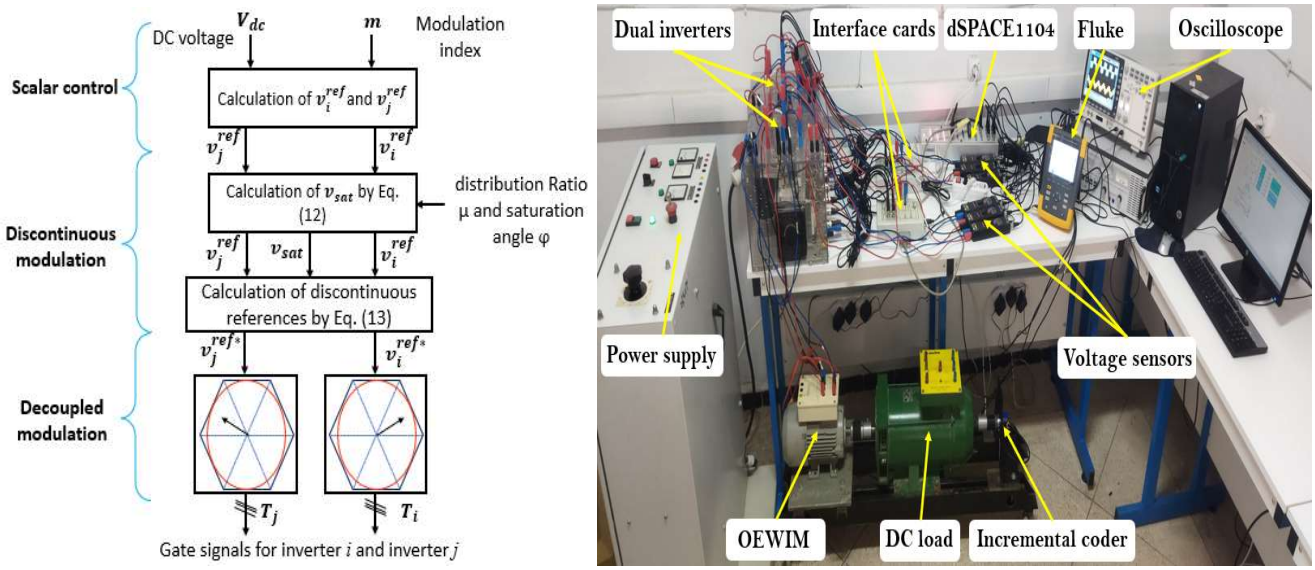


Fig.9. Structure and control scheme of an open-end winding induction motor fed by dual inverters: (a) schematic diagram, (b) Experimental setup.

the inverter losses by 25% compared to the DSVPWM technique. On the other hand, with the DDPWM Max and DDPWM1 techniques, a reduction of 55% in the losses was achieved. However, the ODDPWM achieve a reduction of 58.8 % in the losses. These results confirm that they are in a good agreement with the previous results shown in Fig.6 (Section IV).

- The lowest THD levels (voltage and current) were obtained with the DSVPWM, DDPWM1 and ODDPWM strategies.

Therefore, from the results of the first test, it can be concluded that the DDPWM technique which leads the best performance is the ODDPWM. Where the ODDPWM has been able to reduce the CMV by one level and reduce the losses by approximately 58 %, with the same values for the THD (voltage/current) and ZSV as with the DSVPWM technique.

From the results obtained in the second test, the following conclusions can be drawn:

- When the modulation index is in the range $0.5 \leq m \leq 0.7$, the lowest voltage THD value was obtained with the DDPWM Min and DDPWM Max techniques. Furthermore, the lowest current THD value was obtained with the DPWM Min, DDPWM Max, DDPWM2 and DDPWM4 techniques.
- When $0.7 \leq m \leq 1.0$, the lowest voltage and current THD levels were obtained with the DSVPWM, DDPWM1 and ODDPWM techniques.
- In the range $0.5 \leq m \leq 1.0$, the lowest power losses in the inverters are achieved with the ODDPWM, DDPWM1 and DDPWM Max techniques. Consequently, from the results of the second test it can be concluded that the ODDPWM technique is still the best performing technique although a significant THD degradation can be observed when $0.5 \leq m \leq 0.7$.

TABLE IV. SUMMARY OF DIFFERENT VALUES OBTAINED IN THE FIRST TEST.

PWM type	THD		Power losses in dual inverters (W)
	V %	I %	
DSVPWM	22.1	17.7	790
DPWM Min	31.8	53	580
DDPWMMax	29.2	59.5	340
DDPWM1	23.2	19.2	350
DDPWM2	30.9	25.8	590
DDPWM3	39.5	25.5	580
DDPWM4	32.5	28.8	500
ODDPWM	24.4	20.1	324

VI. CONCLUSION

In this paper, an experimental investigation of various Decoupled Discontinuous PWM (DDPWM) strategies for an Open-End Winding Induction Motor with Dual Inverter (OEWIM-DI) supplied by a single DC source was carried out. This study aimed to determine the control strategy which yields the best performance for the motor drive–in terms of energy efficiency.

From the experimental results, it can be concluded that:

- The control decoupling of the two inverters by an angle of 120° eliminates the Zero -Sequence Voltage (ZSV).
- The DDPWMs techniques reduce Common Mode Voltage (CMV) (compared to DSVPWM) and improve the efficiency by minimising the power losses.
- The DDPWM strategy optimised with the GA is the best performing strategy.

Therefore, given the very encouraging results obtained in this work, we aim to further improve the DDPWM strategies and enhance the performance of the OEWIM-DI. We intend to apply other meta-heuristic optimization techniques to optimize the parameters of DDPWM or use the other techniques such as selective harmonic elimination (SHE) in our future work.

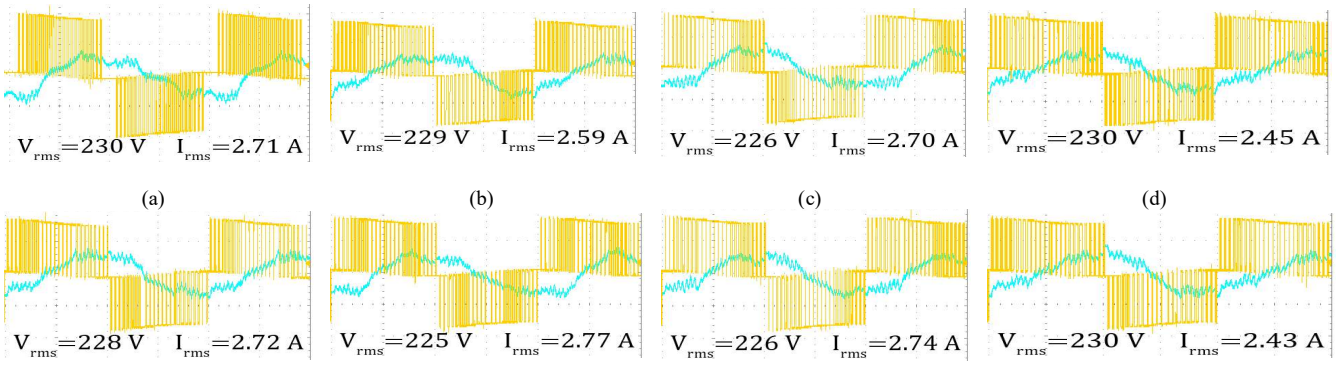


Fig. 10. Experimental voltage and current responses of: (a) DSVPWM, (b) DDPWM Min, (c) DDPWM Max, (d)DDPWM1, (e) DDPWM2, (f) DDPWM3, (g) DDPWM4, (h) ODDPWM.

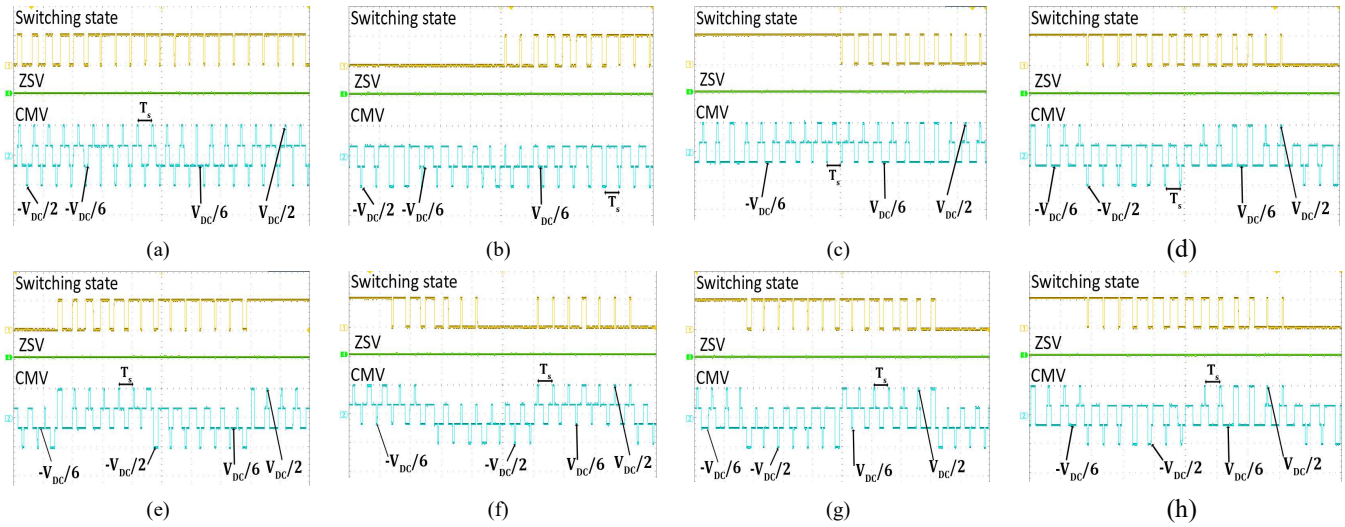


Fig. 11. Experimental response of switching state, CMV and ZSV of: (a) DSVPWM, (b) DDPWM Min, (c) DDPWM Max, (d)DDPWM1, (e) DDPWM2, (f) DDPWM3, (g) DDPWM4, (h) ODDPWM.

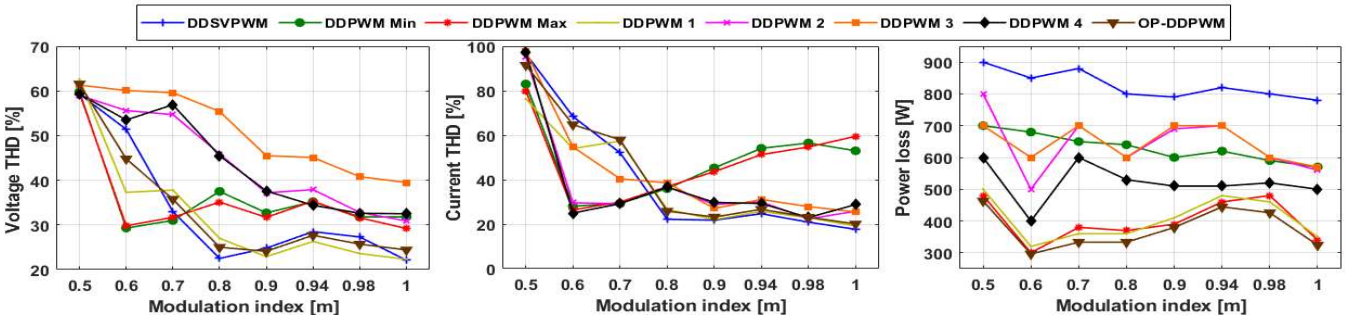


Fig. 12. THD of the voltage with the various strategies.

Fig. 13. THD of the current with the various strategies.

Fig. 14. Power losses in the dual inverters using the various strategies.

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