

Nonvolatile CMOS memristor, reconfigurable array and its application in power load forecasting

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Abstract—The high cost, low yield, and low stability of nano-materials significantly hinder the application and development of memristors. To promote the application of memristors, researchers proposed a variety of memristor emulators to simulate memristor functions and apply them in various fields. However these emulators lack nonvolatile characteristics, limiting their scope of application. This paper proposes an innovative nonvolatile memristor circuit based on complementary metal-oxide-semiconductor (CMOS) technology, expanding the horizons of memristor emulators. The proposed memristor is fabricated in a reconfigurable array architecture using the standard CMOS process, allowing the connection between memristors to be altered by configuring the on-off state of switches. Compared to nano-material memristors, the CMOS nonvolatile memristor circuit proposed in this paper offers advantages of low manufacturing cost and easy mass production, which can promote the application of memristors. The application of the reconfigurable array is further studied by constructing an Echo State Network (ESN) for short-term load forecasting in the power system.

Index Terms—Memristor, reconfigurable array, echo state network, power load forecasting

I. INTRODUCTION

WITH the rise of artificial intelligence era, the ever-increasing amount of calculations challenges the performance of computer hardware. Traditional computers using the von Neumann architecture suffer from the von Neumann bottleneck, which arises from the separation of storage and computation. To overcome this issue, researchers are exploring new computing architectures, and one promising solution is the in-memory computing architecture based on memristors. Memristors possess nonvolatility, nonlinearity, and scalability, which make them suitable for various applications including

neural dynamic systems [1]–[3], neuromorphic systems [4]–[6], and chaotic oscillation circuits [7]–[9]. Accordingly, the memristor array, with the characteristics of computing in memory, has been highly expected by researchers from academia and industry to break through the von Neumann bottleneck.

In the past decade, research into nano-scale materials with resistive switching functions has promoted the epoch-making development of memristors. Notably, these materials encompass a diverse array of innovations, including electrochemical metallization (ECM) memristors, thermochemical memristors, chalcogenide memristors, graphene oxide memristors, and more. These pioneering investigations, grounded in distinct resistive switching mechanisms, have not only enriched our understanding but also invigorated the landscape of memristor-based in-memory computing. However, these memristors continue to face serious challenges in terms of fabrication. Factors such as the limitations of miniaturization in the manufacturing process and the ability to control the uniformity of multiple devices have constrained their scalability. Additionally, issues related to the stability of their resistance states and the reproducibility of their switching characteristics have hindered their reliability. Furthermore, the compatibility of memristor materials with standard microelectronics process has constrained their integration. The significant gap in memristor fabrication severely restricts research and broader application of memristors.

A memristor emulator is an electronic circuit with resistive switching capabilities and constructed using existing electronic components. Its primary purpose is to simulate memristor functions and explore application scenarios based on the resistive switching mechanism. This is particularly valuable given the current limitations surrounding the large-scale deployment of physical memristors. The operational principle of a memristor emulator circuit relies on the assistance of peripheral circuits to store or release the charge in a capacitor, effectively simulating the changes in the resistance state of the memristor. It is crucial to note that this memristor emulator is not dedicated to simulating the resistive switching mechanism of a specific material but rather to capturing the universal characteristics of memristors, namely resistive switching and non-volatility. The motivation behind this article lies in leveraging the existing CMOS process to design a non-volatile memristor circuit, enabling the study of reconfigurable arrays

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based on devices with resistive switching characteristics and their applications in neural networks.

Memristors are expected to break through the von Neumann bottleneck due to the parallel computing capabilities of memristor array units, which utilize the basic voltage-current relationship to complete parallel computing functions [10]. Over the past decade, there has been rapid development in research and applications based on memristor array structures. Kim *et al.* integrated a memristive crossbar array on top of a CMOS chip that can store complex binary and multilevel pixel bitmap images [11]. Hu *et al.* explored the potential of a memristor crossbar array that functions as an auto-associative memory and applied it to brain-state-in-box neural networks. Their proposed training scheme can alleviate or even eliminate the effects of noise [12]. Prezioso *et al.* utilized a metal-oxide memristor array to perform single-layer perception with the delta-learning rule and achieved the classification of 3×3 -pixel black/white images into three classes successfully [13]. Although various types of neural networks, on-chip learning algorithms, and application scenarios have been rapidly developed over the past decade, there is still a drawback that limits the flexible application of memristor arrays. Once the circuit structure is fixed after manufacturing, the connection between the circuit cannot be changed, resulting in a lack of reconfigurability. It is of great value to develop a reconfigurable memristor array. Therefore, this paper proposes a reconfigurable array based on CMOS memristor circuit to facilitate the application of the reconfigurable memristor arrays.

Electricity loads exhibit fluctuations, and the optimal and efficient storage of generated power is not always feasible. Consequently, it becomes imperative to utilize the generated power at the time of production to satisfy the prevailing demand. This necessity underscores the significance of electricity load forecasting for power generation entities as it enables them to estimate the total electricity demand. The need for load forecasting can be fully demonstrated from the following aspects. First and foremost, it plays a pivotal role in ensuring the stability of the electrical grid, benefiting both power utilities and grid operators. Furthermore, load forecasting aids in the optimization of generation resource allocation, which encompasses various sources such as coal, natural gas, wind and solar power. Lastly, as renewable energy sources like wind and solar continue to integrate into the grid, load forecasting becomes indispensable for harmonizing intermittent generation with fluctuating demand. In this work, we are committed to addressing this critical need by harnessing the capabilities of our designed reconfigurable memristor array. This innovation promises to enhance the accuracy and timeliness of load forecasting, thereby benefiting power utilities and contributing to a more efficient and sustainable energy ecosystem.

Power load forecasting is a challenging task due to the nonlinear and complex nature of load data. Conventional forecasting techniques [14] often struggle to capture the intricate patterns effectively. The echo state network (ESN) shows significant promise in addressing such nonlinearity by leveraging a dynamic reservoir of neurons with random connections [15]. This reservoir inherently enables the net-

work to capture complex temporal dependencies in the data. Underpinned by the unique advantages offered by memristor-based in-memory computing technology, ESNs are particularly well-suited for implementation on memristor-based hardware due to their ability to exploit the computational power of recurrent networks while offering ease of training and low energy consumption [16]. However, a prevailing challenge arises in combining ESNs with the memristor array structure. To facilitate hardware implementation, the modified ESN is adopted for deployment on the conventional memristor crossbars. A serious problem is that the stability of the modified ESN has not been strictly proven, which may result in unstable phenomena when using these modified ESN memristor arrays [17]. Benefiting from the reconfigurable property of the designed memristor array in this paper, we can effectively solve this problem by implementing the classical ESN on the reconfigurable memristor array while ensuring that the spectral radius of weight matrix is less than one to maintain the network stability [18].

Herein, a novel CMOS-based voltage differential current conveyor transconductance amplifier (VDCCTA) circuit is proposed. The circuit exhibits the following characteristics: in the absence of an input voltage signal, the output resistance of its Z-port tends to infinity, while in the presence of an input voltage signal, the output resistance of its Z-port approaches a finite value. This unique characteristic ensures that the charge stored in the capacitor is not leaked when the capacitor is connected to the Z-port without an input voltage signal, thereby creating the nonvolatile characteristics of the designed memristor. Based on the proposed VDCCTA, we designed grounded and floating nonvolatile memristor circuits. These designed memristor circuits have the characteristics of simple structures and flexibility. Their hysteresis loop characteristics and nonvolatile characteristics have been verified. Furthermore, using the designed memristor circuit, we developed a reconfigurable memristor array with size of 64×64 , designed and fabricated in the Semiconductor Manufacturing International Corporation (SMIC) $0.18 \mu m$ CMOS process. By programming the switches turning on and off in the memristor array, the memristor connection structure within the array can be configured, making the memristor array structure more flexible. Finally, a memristive ESN hardware implementation was performed and applied to the short-term power load forecasting. By constructing the classical ESN on the reconfigurable memristor array, the stability of the network can be ensured by setting the spectral radius of weight matrix in the proper range [18].

The remaining sections of this article are as follows. Section II proposes a CMOS VDCCTA circuit and constructs a nonvolatile memristor based on the VDCCTA. The pinched loops and the nonvolatile characteristics of the designed memristor are verified in this section. Section III constructs a reconfigurable memristor array. In this section the principles of the reconfigurable array configuration and the measured hardware results are displayed. Integrated circuit implementation and verification of the reconfigurable memristor array are depicted in Section IV. The application of the reconfigurable memristor array on power load forecasting is explained in Section

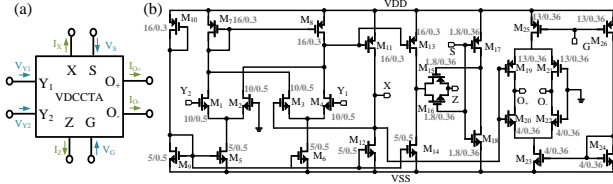


Fig. 1. Circuit symbol of VDCCTA and internal structure of the CMOS based VDCCTA, (a) symbol of the VDCCTA, (b) CMOS circuit of VDCCTA.

V. Section VI summarizes the gap between the memristor emulator and the physical memristors, and compares it with some existing nonvolatile memory devices. Furthermore, the research direction in the task of power load forecasting is discussed. Section VII summarizes the whole paper and looks forward to the future work.

II. VDCCTA BASED NONVOLATILE MEMRISTOR CIRCUIT

A. VDCCTA

The proposed VDCCTA circuit in this work is mainly composed of three parts: the differential voltage input port, current conveyor and transconductance amplifier. The circuit symbol of the VDCCTA is shown in Fig.1(a). The terminal \$Y_1\$ and \$Y_2\$ are the differential voltage input port, which are used to convert the input voltage to current. Output terminals \$X\$ and \$Z\$ transmit current to externally connected passive components. It should be noted that the terminal \$Z\$ will be connected with a capacitor to achieve charge storage and release, which is essential for the nonvolatility of the memristor circuit. In order to ensure that the charge stored in the capacitor will not be released from the \$Z\$-terminal when there is no signal input to the circuit, a bi-directional MOS switch is designed in the VDCCTA to control the charge of capacitor. The voltage input terminal \$S\$ is used to control the conduction and cut-off of the switch. The input terminal \$G\$ is used to control the transconductance of the transconductance amplifier through the input bias voltage. \$O_+\$ and \$O_-\$ are two current output terminals of transconductance amplifier.

The CMOS based implementation of VDCCTA is depicted in Fig.1(b). This CMOS VDCCTA is composed by differential voltage input (\$M_1 - M_8\$), current conveyor (\$M_{11} - M_{14}\$), analog switch (\$M_{15} - M_{18}\$), transconductance amplifier (\$M_{19} - M_{26}\$), and biasing circuit (\$M_9, M_{10}\$). The following expressions can be obtained according to the schematic shown in Fig.1(b).

$$\begin{aligned} V_X &= V_{Y1} - V_{Y2} \\ I_Z &= \begin{cases} I_X & \text{if S is on} \\ 0 & \text{if S is off} \end{cases} \\ I_{O+} &= -I_{O-} = g_m V_X \end{aligned} \quad (1)$$

where \$g_m\$ is the gain of transconductance amplifier. All of the transistors in Fig.1(b) are working in the saturation region.

B. VDCCTA based memristor circuit

The memristor circuits with grounded structure and floating structure are designed using the proposed VDCCTA circuit. Firstly, let us consider the grounded type memristor circuit

as shown in Fig.2(a). It contains only one capacitor (\$C\$), two resistors (\$R_1\$ and \$R_2\$) and the proposed VDCCTA. The double input single output switch \$K\$ is used to control the form of incremental and decremental changes of the memconductance.

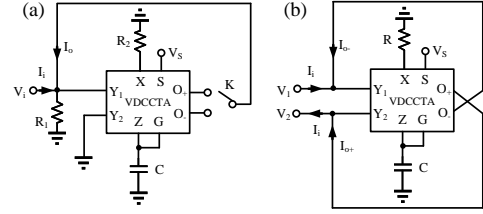


Fig. 2. (a) Grounded type memristor constructed by the VDCCTA, (b) floating type memristor constructed by the VDCCTA.

From the terminal equation of the VDCCTA, we can get the relationship between input voltage \$V_i\$ and current \$I_i\$ of the memristor emulator in Fig.2(a) as

$$V_i = (I_i \pm I_o)R_1 = (I_i \pm K(V_{DD} - V_G + |V_{TP}|)V_i)R_1. \quad (2)$$

The positive and negative of the current \$I_o\$ in (2) depends on the terminal of the switch \$K\$. When the switch selects the \$O_+\$ terminal, the current \$I_o\$ takes a positive sign, and when the switch selects the \$O_-\$ terminal, the current \$I_o\$ takes a negative sign. Owing to the connection of the terminal \$G\$ and terminal \$Z\$ to the capacitor, the transconductance control voltage \$V_G\$ can be expressed as

$$V_G = V_C = \frac{1}{C} \int \frac{V_i}{R_2} dt = \frac{1}{R_2 C} Q_i. \quad (3)$$

Substituting (3) into (2) we can get

$$V_i = (I_i \pm K(V_{DD} - \frac{1}{R_2 C} Q_i + |V_{TP}|)V_i)R_1. \quad (4)$$

Therefore, the memconductance of the proposed circuit is found as

$$W = \frac{I_i}{V_i} = \frac{1}{R_1} \pm K(\frac{1}{R_2 C} Q_i - V_{DD} - |V_{TP}|). \quad (5)$$

where the positive sign is achieved by selecting the \$O_+\$ feedback to the input terminal, corresponding to the incremental memconductance memristor, and the negative is achieved by selecting the \$O_-\$ feedback to the input terminal, corresponding to the decremental memconductance memristor.

The floating type memristor circuit is composed by only one resistor (\$R\$), one capacitor (\$C\$), and the proposed VDCCTA as shown in Fig.2(b). According to the terminal characteristics of the VDCCTA we can get the output current of the \$O_+\$ and \$O_-\$ terminals as

$$I_{O+} = -I_{O-} = K(V_{DD} - V_G + |V_{TP}|)(V_1 - V_2) \quad (6)$$

where \$V_1\$ and \$V_2\$ are the differential input voltage of the memristor circuit.

Similarly to (3), the expression of \$V_G\$ can be written as

$$V_G = V_C = \frac{1}{C} \int i_z dt = \frac{1}{C} \int \frac{V_1 - V_2}{R} dt = \frac{1}{RC} Q_i. \quad (7)$$

Noting that the gate current of MOS transistor is almost zero, we can get \$I_i = I_{O+} = -I_{O-}\$.

Therefore, the memconductance of the floating type memristor circuit can be expressed as

$$W = \frac{I_i}{V_1 - V_2} = K(V_{DD} + |V_{TP}| - \frac{1}{RC}Q_i). \quad (8)$$

C. Simulation of the proposed memristor

To verify the function of the proposed VDCCTA based memristor circuits in Fig.2, simulations are performed by using Virtuoso Analog Design Environment in Cadence software. Throughout simulations, SMIC 0.18- μm CMOS process is used and supply voltages are chosen as $V_{DD} = -V_{SS} = 1V$. The capacitance value of the capacitor is selected as 1nF. The dimensions of transistors are marked in Fig.1. The selection of the 0.18- μm CMOS process, while not representative of the cutting-edge nano-scale process nodes, merits elucidation within the context of our research. It is important to point out that this process was chosen as a foundational platform to illustrate the viability and efficacy of our memristor circuit prototype. It is important to underscore that the adoption of a process featuring smaller feature sizes can potentially give rise to non-ideal effects that can impact circuit performance. To assuage this concern, a meticulous and exacting examination of transistor parameters, involving precise calculations and rigorous adjustments must be carried out to safeguard the integrity and functionality of the underlying circuit typologies. The memristive characteristics have been verified by applying a 1V sinusoidal input signal to the presented memristor circuits. Figs.3 (a) and (b) show the frequency dependent hysteresis loops for the grounded and floating memristor circuits. The correctness of the designed grounded and floating memristor can be demonstrated by Fig.3 in which the lobe areas of the hysteresis loops decrease with the increase of the frequency [19].

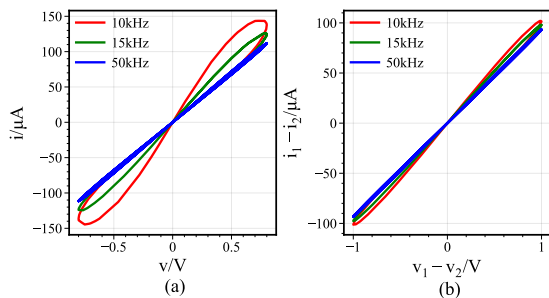


Fig. 3. Frequency dependent pinched hysteresis loops of the memristor for the (a) grounded memristor circuit, (b) floating memristor circuit.

To demonstrate the functional correctness while considering the impact of device variation, the process corner simulations are conducted. Fig.4 illustrates the pinched hysteresis loops under various processing corners, encompassing Typical-Typical (TT), Fast-Fast (FF) and Slow-Slow (SS) scenarios. Notably, it is evident that the proposed memristor maintains its operation even though there is slight variation in its hysteresis loop. It is worth noting that in the FF process corner, a higher current flows, whereas in the SS process corner, a lower current is observed.

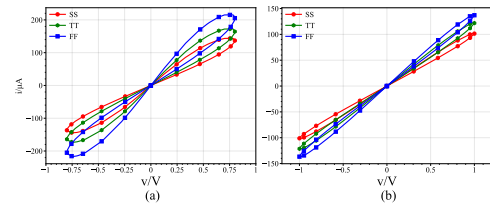


Fig. 4. Processing corner for pinched hysteresis loop of (a) grounded memristor under 10 kHz sinusoidal voltage input, (b) floating memristor under 10 kHz sinusoidal voltage input.

The nonvolatile characteristic of the proposed memristor emulator circuit is verified by considering a train of pulses at the input of the circuit. Voltage pulses with amplitude 0.5V, having the same pulse width of 10 μs and time period of 20 μs have been applied at the input. Figs.5(a) and (b) show the results of the memconductance for both of the grounded incremental and decremental memristors and Figs.5(c) and (d) show the results of the memconductance for both of the floating incremental and decremental memristors. The nonvolatility of the memristor was assessed by applying a pulse signal to one port of the memristor emulator circuit and carefully examining the resulting output current. It is worth noting that in some conventional memristor emulators incapable of achieving nonvolatility, their resistance state tends to disappear during the off state of the pulse train. This phenomenon is typically attributed to charge leakage in the capacitor component when power is turned off. As illustrated by the simulation results depicted in Fig.5, we can observe that the resistance state remains stable during the off state of the voltage pulse. This critical observation serves as compelling evidence supporting the nonvolatile behavior of the designed memristor emulator.

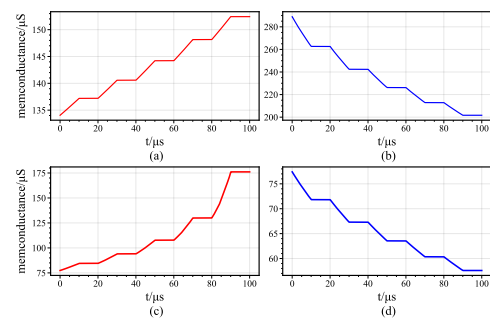


Fig. 5. Variation of memconductance when a pulse train is applied across the memristor emulator, (a) memconductance variation of the grounded incremental emulator, (b) memconductance variation of the grounded decremental memristor, (c) memconductance variation of the floating incremental emulator, (d) memconductance variation of the floating decremental memristor.

It should be pointed out that after long-term operation, memristor circuit may have some performance degradation phenomena, such as shorter retention time of the resistance value, changes in the range of resistance values and changes in the nonlinear characteristics of the memristor circuit. These non-ideal variations are mainly affected by the inevitable CMOS device aging problems in electronic systems.

Table I provides the comparison of performances between

TABLE I
COMPARISON OF THE PROPOSED MEMRISTOR EMULATOR WITH
REPORTED WORKS

Ref.	Components	Technology Node	Transistor Count	Power Consumption	nonvolatile
[20]	DDCC	0.35 μm	50	74.5mW	no
[21]	CCTA	0.25 μm	30	7.5mW	no
[22]	Subtractor	0.25 μm	12	4.51mW	no
[23]	CCII-OTA	0.18 μm	23	9.567mW	no
This work	VDCCTA	0.18 μm	26	1.16mW	yes

the proposed memristor circuit and the reported typical CMOS-based memristor circuits. Based on the same or similar process, the circuit we designed uses fewer transistors, and also has significant reduction in power consumption. Compared with the CCII-OTA based memristor circuit, which uses same process and has 23 transistors, the power consumption of our VDCCTA memristor only accounts for 12.12% of that circuit.

III. MEMRISTIVE RECONFIGURABLE ARRAY

Reconfigurable hardware platforms have gained significant attention in the integrated circuit industry due to their inherent flexibility, allowing for customization to meet specific needs. This paper presents a reconfigurable memristor array designed using the proposed nonvolatile memristor circuit, as shown in Fig.6(a). The array comprises Configurable Analogue Blocks (CABs), Current Switch Boxes (ISBs), and Voltage Switch Boxes (VSBs). The output current of each CAB can be reconfigured to different units by programming ISBs, while the VSB is responsible for configuring the input voltage of CAB from different input ports through switch programming. Therefore, configuring the circuit primitives with the analog switch boxes makes it possible to obtain different input-output connection topologies of the memristor array with ease. As the smallest unit of the reconfigurable array, the CAB unit plays an important role. In Fig.6(b), the block diagram illustrates the CAB, featuring two input ports and two output ports. According to Kirchhoff's law, each CAB efficiently converts the input port voltages into corresponding output currents by utilizing the internal memristors. The internal connection structure is visually depicted in Fig.6(c). In Fig.6(c), the memristors are denoted by $G_{11} \dots G_{22}$. V_{Li1} and V_{Li2} represent the i -th row input voltage and I_{Cj1} , I_{Cj2} represent the j -th column output current of the CAB. In each CAB, eight control switches are divided into row control switches and column control switches, labeled as $K_{R1} \dots K_{R4}$ and $K_{C1} \dots K_{C4}$, respectively. The corresponding control voltages of the switches are denoted as $S_{R1} \dots S_{R4}$ and $S_{C1} \dots S_{C4}$.

IV. HARDWARE IMPLEMENTATION OF THE PROPOSED RECONFIGURABLE ARRAY

In the previous section, we discussed the proposed nonvolatile VDCCTA memristor and the reconfigurable memristor array. To enable the practical fabrication of the reconfigurable array using the proposed VDCCTA memristor, we designed the layout based on the SMIC 0.18 μm standard CMOS process. As shown in Fig.7(a), the proposed reconfigurable memristor array layout includes the memristor array and blocks

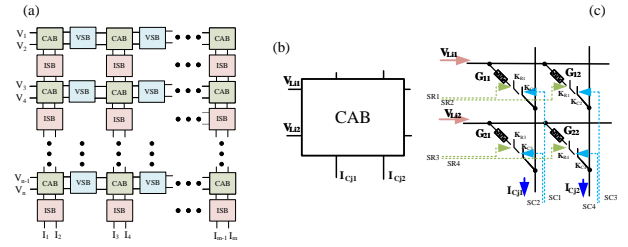


Fig. 6. (a) Block diagram of the proposed reconfigurable memristor array, (b) configurable analog block in the array, (c) internal connection of the configurable analog block.

for control switches. Although the manufacturing process of CMOS is relatively controllable compared to physical memristors, the memristor emulators utilizing CMOS technology are also facing with the issue of device variability. This variability arises from the influence of manufacturing processes, material imperfections, and environmental variations. The incongruity among memristor emulators can detrimentally affect the precision and reliability of application in the task of power load forecasting. To address the challenges of variability among memristor emulators, the layout design is very important to ensure its performance, yield and reliability. In order to deal with this problem in our layout design, we adopt some common key layout techniques such as centroid layouts, interdigitated layouts, guard rings. The overall chip area is 4.851mm \times 4.853mm, with the reconfigurable memristor's area being 3.828mm \times 1.765mm. Due to the limited chip area, the reconfigurable array we fabricated contains 64 \times 64 memristors. The fabricated chip packaged on Printed Circuit Board (PCB) of the proposed reconfigurable memristor array is shown in Fig.7(b).

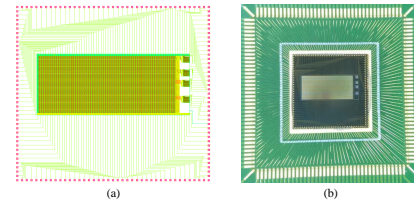


Fig. 7. Layout and packaged chip of the reconfigurable memristor array.

To test the functionality of the fabricated memristor array, we systematically evaluated each individual memristor by subjecting it to a sinusoidal voltage input to measure the hysteresis loop. Figs.8(a) to (c) display the hysteresis loops in V-I plane obtained from the memristor located in the 23rd row and 42nd column (for the convenience of demonstration, we randomly select one of the cases for explanation) by setting the frequency of voltage source as 1kHz, 1.5kHz and 5kHz. The results are consistent with our previous simulations, as illustrated in the figure. Specifically, the memristor can effectively generate a hysteresis loop that passes through the origin of the V-I plane under a periodic voltage source, and the lobe area of the hysteresis loop correspondingly decreases with increasing input frequency. Notably, while we only describe one example here, similar results have been obtained for all tested memristors in the array. To verify the functionality of

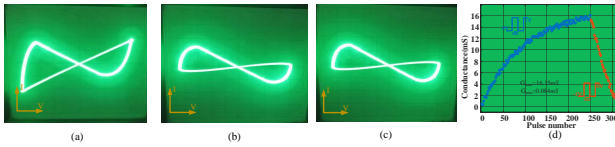


Fig. 8. The frequency dependent hysteresis loops in V-I plane captured by the oscilloscope (a) input frequency is 1kHz, (b) input frequency is 1.5kHz, (c) input frequency is 5kHz, (d) the conductance variation process under pulse signal.

the fabricated memristor, we tested the hysteresis loop of each memristor in the array. Subsequently, we utilized a pulse signal with an amplitude of 1V, a width of 1ms, and a period of 2ms as the excitation input to facilitate subsequent verification of the nonvolatility. The output current of the memristor reflected an increase in the conductance value under the positive pulse, while a decrease in the conductance was obtained under the pulse signal with an amplitude of -1V, width of 1ms, and period of 2ms. Fig.8(d) illustrates the conductance variation process of the memristor under the positive and negative pulses.

Fig.8(d) indicates that the memristor has a conductance of about 0.084mS to 16.15mS and the transconductance ratio $G_{max}/G_{min}=192$. This suggests that the designed memristor has a wide range of conductance values. Additionally, we observe that the memristor conductance reduction occurs approximately twice as fast as the conductance increase. As shown in the figure, it takes roughly 252 pulses to increase the conductance from its initial value to the maximum conductance, whereas it takes only about 60 pulses to reduce the maximum conductance to its original state.

V. APPLICATION OF THE RECONFIGURABLE MEMRISTOR ARRAY ON POWER LOAD FORECASTING

A. Framework of reconfigurable array based ESN

To leverage the measured characteristics of the memristor, we have applied the proposed reconfigurable memristor array to the ESN for the purpose of short-term power load forecasting. The ESN structure is composed of an input layer, a reservoir (hidden layer), and an output layer. The relationship between the input and output of the network can be described by

$$y(t) = W_{out}u(t) = W_{out}f(W_{res}u(t-1) + W_{in}x(t)) \quad (9)$$

where $x(t)$, $u(t)$ and $y(t)$ are the input, reservoir state, and output of the network at time t . W_{in} , W_{res} and W_{out} are the synaptic matrix representing the connection from the input neuron to the reservoir, the self-connection in the reservoir and the connection from the reservoir to the output, respectively. The function $f(\cdot)$ denotes the activation function of the network. Compared with the recurrent neural networks, the most significant feature of ESN is that the input weight matrix W_{in} and the reservoir weight matrix W_{res} are randomly generated and fixed, and only the output matrix W_{out} needs to be trained.

Updating only the weight matrix of the output layer with the traditional ESN training method overcomes issues of local minimum and reduces training complexity. However,

random neural connections in the reservoir can hinder ESN hardware design. We propose to use reconfigurable memristor arrays selectively connecting working memristors to match task requirements, making it highly suitable for implementing sparse matrices with random connection characteristics.

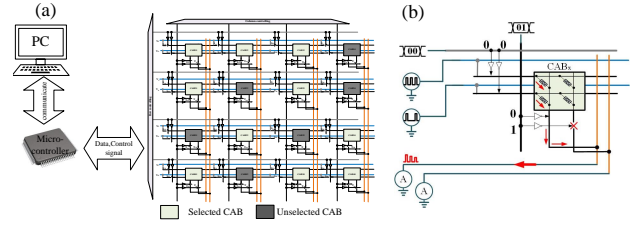


Fig. 9. Hardware experimental flow chart, (a) the overall workflow, (b) mapping scheme of a CAB.

Fig.9(a) shows the process of the hardware experiment in the application of ESN. Firstly, the input weight matrix and the reservoir weight matrix of the ESN are randomly generated, and the output weight matrix of the ESN is trained offline by the ridge regression algorithm [24].

Then, the state of the reconfigurable switches is obtained based on the reservoir weight matrix. According to the weight matrix, the reconfigurable switch is turned on where there is synaptic connection, and the switch is turned off where there is no synaptic connection.

Next, the reservoir weight values are mapped onto the reconfigurable memristor array, where the weight value is represented by the conductance value of the memristor. It is difficult to represent the negative value of synaptic weights by one memristor, because the actual conductance value is positive. In general, two memristors are used to represent the true synaptic weight with the difference of their conductance values. The minimum unit of the reconfigurable array designed in this paper is 2×2 memristors, which facilitates the use of conductance of two memristors to represent the positive and negative of synaptic weights. Fig.9(b) demonstrated a programming process of an arbitrarily CAB. In this process, the left column memristors are mapped with the synaptic weights of the reservoir, and the right column memristors are not connected into the network.

Memristors exhibit a unique and inherently nonlinear relationship between the applied voltage and the resulting current, presenting challenges when mapping neural network weights to resistance values. Researchers have been actively exploring solutions to this challenge, including calibration, compensation algorithms, and specialized training strategies, as evident in studies [25]–[27]. In this work, we address the issue of nonlinearity by adopting an approach inspired by the methodology discussed in [13]. This method involves initializing memristors within the middle of their conductance range, resulting in a relatively linear voltage-conductance relationship. After measuring the conductance variation range of the memristor circuit, we selected the 2~14 mS interval with a favorable linearity to represent the synaptic weights. While this approach may introduce some reduction in accuracy, it offers the advantage of being more straightforward to implement in the task of power load forecasting. The synaptic weights of

the reservoir are divided into two parts: W_{res}^+ and W_{res}^- . The synaptic weight W_{res} is mapped by the following equation

$$G_{p/n} = \frac{|W_{res}^{+/-}|}{\max(|W_{res}^{+/-}|)} (G_{max} - G_{min}) + G_{min} \quad (10)$$

where $G_{p/n}$ is the conductance value corresponding to the weight value of W_{res}^+ or W_{res}^- counting.

Finally, the reservoir states are collected by the micro-controller and the calculation of the output is performed to obtain the predicted output.

B. Experimental demonstration

We apply memristive reconfigurable array to perform power load forecasting and validate the functionality of our designed circuit. Power load forecasting based on neural networks can be achieved through univariate model [28] and multivariate model [29]. The univariate model is only established based on the historical power load data, while the multivariate model is related to multiple factors such as temperature, sunlight and humidity. In this research, we mainly focus on implementing the univariate ESN to extract intricate patterns from historical data. Consequently, we utilize a single input neuron and a single output neuron in the implementation. For instance, considering a network with 32 reservoir neurons, the synaptic weight matrices denoted as W_{in} , W_{res} and W_{out} have dimensions of 1×32 , 32×32 and 32×1 , respectively.

In this study, we utilize the historical power load data from the EUNITE competition [14]. This dataset comprises power load measurements taken a 30-minute intervals throughout the years 1997 and 1998 in eastern Slovakia. Our analysis focuses on the historical data from the year 1997, which consists of a total of 17520 data points. This data serves as our training set for the task at hand: predicting the power load for the corresponding time period in 1998. Specifically, we engage in short-term load forecasting, aiming to predict the power load one hour ahead, based on the historical information. To prepare the data for our forecasting model, we first normalize the data points to voltage values within the region of $[-1V, 1V]$. Subsequently, these normalized data are transmitted from the host system to the MCU through a communication interface. Within the MCU, each data point undergoes precise voltage conversion under the controlled guidance of the MCU. These converted voltages are then systematically directed into the input port of the reconfigurable array. surrounding equation.

The hardware experiment results measured by an oscilloscope is depicted in Fig.10. The parameters are configured as follows: spectral radius $\rho=0.5$, learning rate $\lambda=0.001$ and reservoir size $R=32$. For the selection of each parameter, we conducted a series of 50 independent experiments, diligently exploring the parameter space. Subsequently, we selected a representative parameter setting based on performance, assessed through the mean square error (MSE). The corresponding MSE variations with respect to these parameters are depicted in Fig.11.:

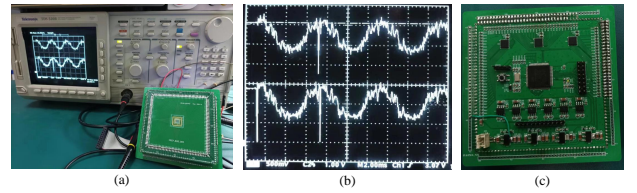


Fig. 10. (a) Hardware experiment of the short-term power load forecasting, (b) oscilloscope captured results of the hardware experiment, (c) control board of the reconfigurable array.

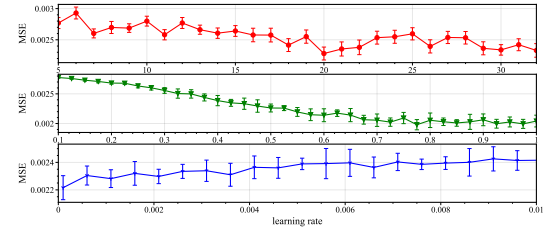


Fig. 11. Mean square errors with respect to parameter (a) R varying in region $[5, 32]$ fixed $\rho=0.5$ and $\lambda=0.001$, (b) ρ varying in region $[0.1, 1]$ fixed $R=32$ and $\lambda=0.001$, (c) λ varying in region $[0.001, 0.01]$ fixed $R=32$ and $\rho=0.5$, in 50 independent experiments.

C. Performance analysis and comparison

Circuit noise phenomena have a significant impact on the electronic systems. Sometimes, the designed circuits may function undesirably under the influence of circuit noise. In the ESN electronic system designed in this work, the noise is also inevitable. Fig.12(a) shows the states of the first 10 reservoirs in the ESN with 32 reservoirs affected by circuit noise within 2ms. Under the influence of noise of different strengths, the states of the reservoirs may deviate from the ideal value, thus affecting the accuracy of the network operation. Fig.12(b) explores the impact of different noise strengths on the MSE of the network to reflect the effects of noise intensity on the accuracy of the circuit. The MSE loss in the figure is calculated by

$$MES\ loss = 10 \log_{10}(m/\tilde{m}) \quad (11)$$

where m and \tilde{m} are the ideal MSE without effects of noise and the actual MSE under noise, respectively. It can be seen from the figure that as the intensity increases, the accuracy of the network drops sharply. When the noise intensity is greater than 5%, the \tilde{m} is around ten times that of m , indicating that the network can no longer complete the prediction accurately.

In the hardware network comprising various reservoir configurations, we present a tabulated overview of chip areas in

TABLE II
HARDWARE AREA AND POWER CONSUMPTION WITH RESPECT TO DIFFERENT RESERVOIR SIZES

Reservoir size /MSE	Used chip area (mm^2)	Power consumption (mW)
$8/2.9 \times 10^{-3}$	0.0256	18.56
$16/2.7 \times 10^{-3}$	0.0512	37.12
$24/2.4 \times 10^{-3}$	0.0768	55.68
$32/2.3 \times 10^{-3}$	0.1024	74.24

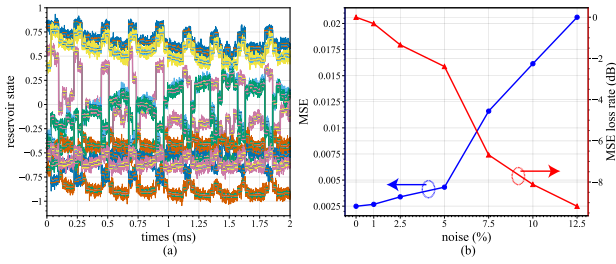


Fig. 12. Noise influence on the neural network, (a) collected the first ten reservoir states within 2ms under different strength of noise, (b) MSE with respect to the strength of noise.

use alongside their corresponding power consumption values, as detailed in Table II. The reported area measure pertains to the utilized portions within the chip layout of the network, while the power consumption data is derived from comprehensive EDA reports. It is noteworthy that power consumption is primarily influenced by the supply, especially in the context of maintaining the functionality of the memristor circuit. Through meticulous voltage supply adjustments, we have the capacity to effectively minimize circuit power consumption while concurrently ensuring the robust operation of the memristor circuit.

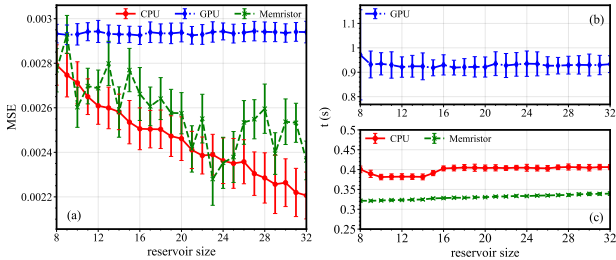


Fig. 13. Performance comparison with CPU and GPU based ESN, (a) MSE variation with different reservoir size, (b) training time consumption with different reservoir size.

Fig.13 presents a performance comparison between the reconfigurable memristor array-based ESN and the traditional Central Processing Unit (CPU) and Graphics Processing Unit (GPU) based ESN. The evaluation considers variations in MSE and training time consumption with respect to the reservoir size. The experimental environment is based on Python 3.8 programming language, using PyTorch 1.11 and CUDA 11.7 for CPU and GPU computing. The hardware setup consisted of an Intel CPU (Core i7-10700k), which served as the CPU computing platform, and an NVIDIA GeForce RTX3080 for GPU acceleration. The results depicted in the figure reveal that the CPU-based approach achieves superior accuracy. In contrast, the GPU-based method is constrained by its architectural separation of storage and computation, resulting in limitations in training time and accuracy performance. The proposed method can achieve comparable accuracy with the CPU-based approach while significantly reducing training time, thanks to its in-memory computing architecture.

In recent years, researchers have introduced a variety of short-term load forecasting algorithms for the power system. The majority of these algorithms rely on either CPU or GPU

TABLE III
COMPARISON OF PROPOSED METHOD WITH SOFTWARE-BASED METHODS

method	MAPE(%)	method	MAPE(%)
SVM-GA [30]	1.93	FOAGRNN [31]	1.25
RBFNN [32]	3.35	LSTM [33]	2.31
SOFNN [34]	1.607	DTW-GRU [35]	1.01
this work (software)	1.16	this work (hardware)	1.85

processing. To assess the accuracy of our work in comparison to these software-based algorithms, we employ the Mean Absolute Percentage Error (MAPE).

Table III display the MAPE values generated through different methods. Notably, our approach, which employs ESN, achieves a low MAPE, signifying superior accuracy. While the precision of the method relying on reconfigurable memristor array has slightly decreased, it still maintains higher accuracy compared to that of literature [30], [32], [33].

VI. DISCUSSION

The fundamental purpose of our circuit design is not aimed at the specific resistive switching mechanisms of any particular nano-material but is instead dedicated to manifesting the typical characteristics inherent to non-volatile memristors: resistive switching and the enduring maintenance of resistance values post power-off. From the results of circuit simulation and physical measurement, we can see that the memristor circuit we designed perfectly realizes the resistive switching function and the non-volatile function. While it is undeniable that there is a big difference between our memristor circuit and the real memristor device, its robust suitability within applications grounded in resistive switching mechanisms is also undeniable. Remarkably, our design capitalizes on the standardized CMOS process, engendering seamless compatibility with the existing tapestry of CMOS-based circuits. This compatibility bestows a litany of advantages: good interoperability between circuits, good design tool support, and low cost. However, the design of CMOS-based memristor circuits is not easy to implement. It requires designers to repeatedly verify according to the design principles to achieve the best performance. It also faces complex circuit structures, low design automation, and challenges in digital-analog mixed signal integrity. Therefore, the design of CMOS-based memristor circuits is also a promising and challenging topic

The memristor circuit designed in this work, employing a capacitor to simulate physical memristor behaviors, exhibits nonvolatile characteristic. In comparison to the other types of nonvolatile memory devices such as flash memory and phase change memory (PCM), the capacitor-based memristor circuit relies on CMOS capacitors designed for long-term reliability, theoretically offering an infinite number of write and erase cycles [36]. In contrast, flash memory has limited endurance, often in the thousands to tens of thousands of cycles, while PCM falls within the moderate endurance range, albeit with improvement over time [37]. In terms of read and write speed, the memristor circuit design similar to dynamic random-access memory grants it faster operation, making it advantageous for speed-sensitive applications [38]. Lastly,

considering cost factors, fabricating the CMOS process based memristor circuit can be cost-effective, leveraging existing infrastructure. Flash memory benefits from economies of scale and a mature manufacturing process, resulting in lower costs [39]. In contrast, PCM's manufacturing can be complex and expensive, especially in advanced materials [40].

In the practical realm of load forecasting, the data privacy and security are essential considerations in the selection of implementation methods. In our presented work, we introduce a prototype of a power load forecasting system built upon a reconfigurable memristor array. Notably, this paper predominantly focuses on a localized deployment approach, where the selected load data and the neural network are utilized without reliance on network communication. Consequently, the paper does not delve into an extensive examination of topics pertaining to data security. However, we recognize the significance of this dimension and its critical relevance in real world applications. As part of our ongoing research, we intend to explore the integration of chaotic data encryption methods into practical power load forecasting scenarios. This endeavor aims to culminate in the development of a comprehensive and pragmatic memristor reconfigurable array-based power load forecasting system that addresses not only forecasting accuracy but also the indispensable aspect of data security.

VII. CONCLUSION AND OUTLOOK

In some current research on memristor emulators, the charge cannot be stored in the capacitor for an extended period, thus impeding their nonvolatility. To address this issue, this paper proposes a CMOS-based VDCCTA circuit, enabling the construction of a nonvolatile memristor circuit. Theoretically, when no input signal is present, the terminal connected to the capacitor exhibits an infinitely large output resistance, resulting in an infinite discharge time constant for the capacitor. This theoretical behavior guarantees that memristor can maintain its resistance state indefinitely. In practical terms, the memristor resistance state can be maintained for a quite long period of time, influenced by the finite cut-off resistance of the MOS transistor. Using the proposed VDCCTA circuit, this work constructs grounded and floating memristors and verifies their validity through the observation of pinched hysteresis loops in V-I plane under variable frequency sinusoidal signals. The nonvolatility of the memristor is verified through pulse voltage input. Based on the designed memristor, a reconfigurable array is constructed, allowing for the modification of memristor connection relationships through switch programming. The reconfigurable array is fabricated using SMIC's standard CMOS process, and its effectiveness is confirmed through circuit testing. Finally, we apply the fabricated reconfigurable array in the power load forecasting task. In the future, our work will focus on exploring more applications of the reconfigurable array. Using reconfigurable memristor arrays to reconstruct and adjust the weight position to realize the memristor array-based multi-task learning, without the need for remapping memristor resistance values, is a potential application scenario.

In practical applications, physical memristors are subject to various variations, such as cycle-to-cycle, device-to-device, or

long-term drift. These variations arise from factors like material imperfections, manufacturing processes, and temperature effects, and they significantly impact the performances of the memristive circuits. Similarly, memristor emulators can also encounter these variations. For example, differences in resistor values, capacitor characteristics or transistor properties can introduce cycle-to-cycle variances in the emulator's behavior. Likewise, variations in component tolerances, manufacturing processes, or component aging can lead to the device-to-device variances. Furthermore, the emulator's behavior may drift over time due to aging effects, temperature fluctuations, and other environmental factors. In our current work, our primary focus was on designing a memristor emulator to realize the nonvolatile functionality. While it is important to address emulator variances, the specific way to solve the variations in memristor emulator has not been discussed in depth in this work. However, it is worth noting that, before the chip's manufacturing phase, we implemented matching design and protection design for the layout, which help mitigate some of the variations encountered during manufacturing. In our future research endeavors, we are committed to exploring technical solutions to address memristor emulator comprehensively. These solutions may include temperature compensation techniques, redundancy circuit design, real-time monitoring and compensation circuits, among others. By doing so, we aim to contribute to the development of more robust and reliable memristor emulators that can find practical applications in a wide range of fields.

In the face of the scalability challenges of the memristor circuit, we adopted a design philosophy that prioritizes simplicity and efficiency. Our circuit architecture is inherently modular, allowing for straightforward replication and integration into larger systems. This modularity is conducive to the scaling of memristor emulator circuits. However, constrained by the chosen CMOS process feature size, achieving higher scalability in the designed circuit scheme presents challenges. In our forthcoming research endeavors, we intend to address this issue by exploring scalable design approaches for memristor circuits, focusing on the reduction of transistor usage and the selection of transistors with smaller feature sizes. Our future work will also extend into the realm of larger-scale memristor emulator circuit chips. Specifically, we aim to apply our research to advanced applications, including but not limited to assisting power grid management in large-scale power systems.

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