A 0.18μm CMOS 300MHz Current–Mode LF Seventh–order Linear Phase Filter for Hard Disk Read Channels

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***Abstract*–A 300MHz CMOS seventh–order linear phase g_m–C filter based on a current–mode multiple loop feedback (MLF) leap–frog (LF) structure is realized. The filter is implemented using a fully–differential linear operational transconductance amplifier (OTA) based on a source degeneration topology. PSpice simulations using a standard TSMC 0.18μm CMOS process with 2.5V power supply have shown that the cut–off frequency of the filter can be tuned from 260MHz to 320MHz and dynamic range is about 66dB. Group delay ripple is approximately 4.5% over the whole tuning range and maximum power consumption is 210mW.**

I. INTRODUCTION

The hard disk drive (HDD) industry is constantly developing read channel electronics to push data rates to higher speeds. The main requirements for continuous–time filters in a HDD read channel are high cut-off frequencies, small group delay variations, good linearity and low power consumption, with implementation in standard CMOS technologies. However, modern CMOS technologies are optimized for digital applications, presenting challenges for the design of analog CMOS–only circuits. Designing high frequency integrated continuous-time filters is a complex task which involves simultaneous optimization of sensitivity, high frequency performance, parasitic effects, dynamic range, and noise and so on. The performance of a filter depends on the filter structure and architecture used as well as the IC technology [1]. Analog signal processing in the current domain can offer advantages for many applications and current-mode continuous-time filters have received much attention. Current-mode filters are based on current integrators with current feedback to summing nodes [1, 2]. In a mixed-signal environment the analog part should be immune to noise from the digital part and power supply. To reduce such noise, fully balanced structures are normally used in integrated filter design [2]. Balanced structures can also reduce even-order harmonic distortion. The multiple loop feedback (MLF) leap–frog (LF) structure is well suited to HDD systems because the MLF LF approach can realize arbitrary transmission zeros, whilst ladder simulation method can only directly realize imaginary zeros, and cascade designs require more components to realize transmission zeros. Voltage–mode MLF LF filter structures have been described in [3, 4].

The current-mode MLF LF filter structure has not been previously applied to HDD filter applications. We therefore present a seventh–order leap-frog linear phase low pass filter design. Note that, in order to optimize the filter impulse response for the HDD read channel application, the filter should have a programmable gain boost function which increases gain around the cut-off frequency to provide amplitude equalization, together with linear phase response to equalize the data pulses and. The amplitude equalization should not affect the group delay. The gain boost function can readily be implemented using the MLF LF structure by adding transmission zeros near the cut-off frequency to the prototype low-pass linear phase response, requiring a minimum of additional circuitry. The amount of boost is defined as the extra gain relative to the low frequency gain at the cut-off frequency. The boost function should not affect the group delay specification of the filter. The group delay ripple should be smaller than 5% for any value of gain boost [5].

Therefore, a 210mW 300MHz seventh-order 0.05° linear phase filter is designed in this paper. 66dB of dynamic range and 4.5% group delay ripple is achieved. The paper is organized into five sections. The design of a fully–balanced two input, four output source degenerated OTA is discussed in Section II. Current-mode filter architecture and synthesis are described in Section III. The simulation results for the complete filter are given in Section IV, and finally Section V contains conclusions.

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II. FULLY–BALANCED OPERATIONAL TRANSCONDUCTANCE AMPLIFIER

Large transconductances are needed for the implementation of high–frequency filters. The implementation of large transconductances requires the use of wider transistors and large bias currents. The use of small transistor lengths pushes the parasitic poles to higher frequencies, but the OTA dc gain is reduced and mobility degradation effects become more severe. The use of large drain currents reduces the transistor dc gain even further and increases the power consumption. Another important design aspect is the effect of excess phase at the filter cut–off frequency, usually determined by the OTA parasitic poles and zeros. Very often, large gate-source bias voltages are required in order to improve OTA linearity, but are limited in low voltage applications. In this section we describe the development of a two input, and four output OTA suited to the current-mode filter application. The linearity of the tranconductor can be improved by employing source degeneration techniques [6–8], as in the design of Figure 1. The OTA small–signal transconductance is tuned by adjusting the gate-source voltage of transistors M_{R1} and M_{R2}, which operate in the triode region. For large source degeneration factors, the OTA transconductance is mainly determined by the small–signal conductance of $MR_{1,2}$. Multiple output OTA (MO–OTA) structures have been described in [9]. However, a drawback of these structures is that greater excess phase occurs due to increased loading of the internal nodes by having multiple output stages connected to the single input stage. Therefore, we add an additional input stage in parallel to reduce excess phase, sharing the same source degeneration transistors.

In Figure 1, the sources of the input devices are connected to their substrate, which is a common P–well to prevent body effects. The circuit uses two parallel differential pairs M_1, M_2 – M_3, M_4 in the input stage. The output stages consist of eight current mirrors. The input stage currents are differentially mirrored through P–type current mirrors $M_{10,12}$ $M_{11,13}$ $M_{14,16}$ $M_{15,17}$ and N–type current mirrors $M_{18,20}$ $M_{19,21}$ $M_{22,24}$ $M_{23,25}$ to the outputs. Assuming ideal matching between transistors, the output differential currents $I_{out} = I_{output1} - I_{output4} = I_{output2} - I_{output3}$. The gate voltages of M_{R1} and M_{R2} are connected to source followers M_9 and M_8 biased with a control current I_1, so that both DC level shifts are identical and tuning is obtained via I_1 without altering the bias current of the input stage. The geometry of the input devices also affects the DC transconductance value, and these are usually designed to be large in order to improve matching of threshold voltage V_T and K between the transconductance stages. The channel length used for all devices is the minimum length allowed by the process and the channel widths are: M_1–M_4, 10μm; M_5 , 20μm; M_6, M_7 , 60μm; M_8, M_9 , 20μm; M_{10}–M_{17} , 50μm; M_{18}, M_{19}, M_{22}, M_{23} , 16.7μm; M_{20}, M_{21}, M_{24}, M_{25} , 20μm; M_{R1}, M_{R2} , 120μm.

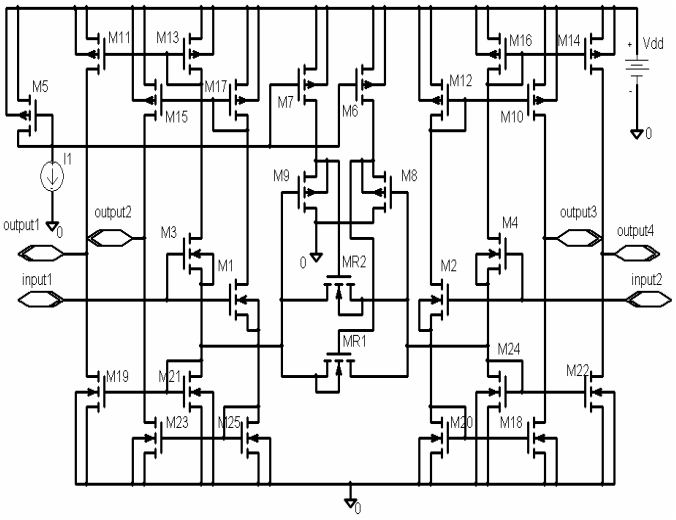

Figure 1 Fully-balanced OTA unit cell

In order to obtain large transconductance, M_{R1} and M_{R2} are connected in parallel. The total drain current $I_{R1,2}$ of M_{R1} and M_{R2} in the triode region is given by:

$$I_{R1,2} = 2K[(V_{GS}-V_T)V_{ds}-1/2V_{ds}^2] \quad (1)$$

Where $K=0.5\mu_n C_{ox}(W/L)$ is the N–type transconductance parameter, and μ_n, C_{ox}, W and L are mobility, oxide capacitance per unit area, and channel width and length respectively. Then:

$$I_{out} = I_{R1,2} - (-I_{R1,2}) = 2I_{R1,2} \quad (2)$$

By substituting (2) into (1) we get:

$$I_{out} = 4K[(V_{GS}-V_T)V_{ds}-1/2V_{ds}^2] \quad (3)$$

Note that $V_{ds} \approx V_{id}$. Therefore, assuming $1/2V_{ds}^2$ is small compared to $(V_{GS}-V_T)V_{ds}$, we get:

$$I_{out} \approx 4K[(V_{GS}-V_T)V_{id}] = g_m \cdot V_{id} \quad (4)$$

Where $V_{id} = V_{input1} - V_{input2}$, V_{id} is the differential input voltage and g_m is the DC transconductance of the MO–OTA given by:

$$g_m = 4K \cdot V_B,\ V_B = V_{GS}-V_T \quad (5)$$

From (2) and (4), we can see that the MO–OTA exhibits a linear V–I characteristic with the assumptions made. However, in practice, second–order effects such as body effects, mobility reduction, and channel length modulation will degrade the linearity of the MO–OTA. Equation (5) shows that the transconductance value can be controlled by varying the bias voltage V_B. Thus, the allowed values of V_B determine the achievable transconductance tuning range. Figure 2 shows the simulated g_m characteristic of the MO-OTA, with the OTA outputs terminated by a short–circuit load for different bias current I_1. The transconductance tuning range is from 1161μs to 1423μs, corresponding to values of I_1 from 20μA to 300μA.

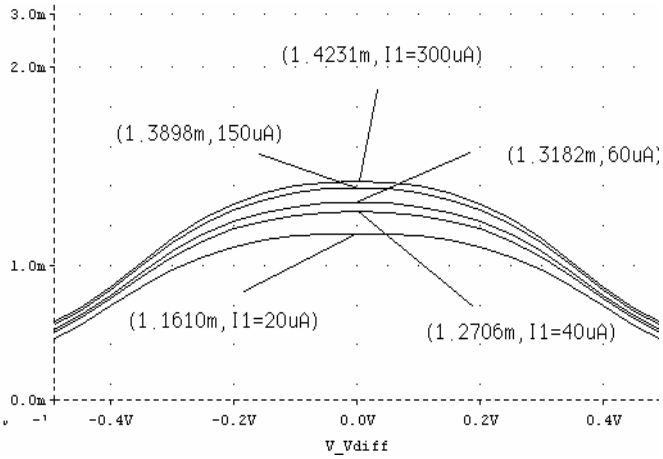

Figure 2 Simulated DC transconductance gain

Simulation of OTA open–circuit response with varying tuning currents is shown in Figure 3. The simulated -3dB cut–off frequencies of the OTA cell are about 360MHz for whole tuning range. The DC gain is around 23dB, which is adequate for low–Q filter applications.

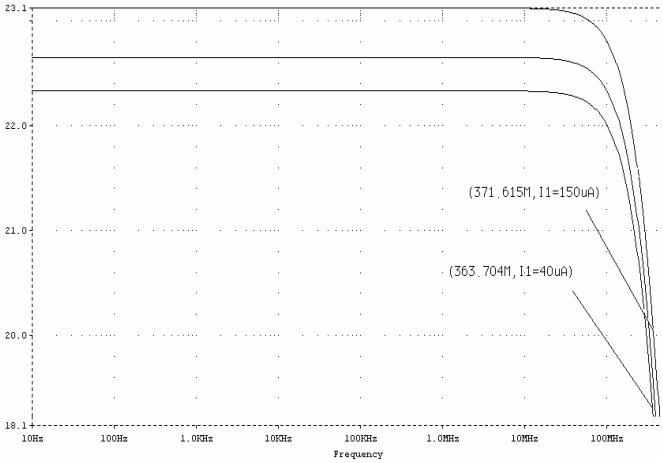

Figure 3 Simulated frequency response of OTA

III. FILTER ARCHITECTURE AND SYNTHESIS

The normalized characteristic of a seventh–order low pass 0.05°equiripple linear phase filter with real zeros (3dB gain boost) at the cut–off frequency is given by:

$$H(s) = (s^2-1)/D(s) \qquad (6)$$

Where:

$$D(s) = 0.055617s^7 + 0.291094s^6 + 1.095656s^5 + 2.554179s^4 + 4.255922s^3 + 4.676709s^2 + 3.176156s + 1$$

The fully balanced realization of the function in (6) using the current–mode LF structure with output summation OTAs is shown in Figure 4. Note that the output of the filter with and without gain boost can be taken from g_{a7} and g_7 OTAs, respectively. The overall transfer function of the circuit with gain boost can be derived as:

$$H(s) = I_{out}/I_{in} = N(s)/D(s) \qquad (7)$$

Where:

$$N(s) = \alpha_5\tau_6\tau_7s^2 + (\alpha_5 + \alpha_7),$$

$$D(s) = \tau_1\tau_2\tau_3\tau_4\tau_5\tau_6\tau_7s^7 + \tau_2\tau_3\tau_4\tau_5\tau_6\tau_7s^6 + (\tau_1\tau_2\tau_3\tau_4\tau_5 + \tau_1\tau_2\tau_3\tau_4\tau_7 + \tau_1\tau_2\tau_3\tau_6\tau_7 + \tau_1\tau_2\tau_5\tau_6\tau_7 + \tau_1\tau_4\tau_5\tau_6\tau_7 + \tau_3\tau_4\tau_5\tau_6\tau_7)s^5 + (\tau_2\tau_3\tau_4\tau_5 + \tau_2\tau_3\tau_4\tau_7 + \tau_2\tau_3\tau_6\tau_7 + \tau_2\tau_5\tau_6\tau_7 + \tau_4\tau_5\tau_6\tau_7)s^4 + (\tau_1\tau_2\tau_3 + \tau_1\tau_2\tau_5 + \tau_1\tau_2\tau_7 + \tau_1\tau_4\tau_5 + \tau_1\tau_4\tau_7 + \tau_1\tau_6\tau_7 + \tau_3\tau_4\tau_5 + \tau_3\tau_4\tau_7 + \tau_3\tau_6\tau_7 + \tau_5\tau_6\tau_7)s^3 + (\tau_2\tau_3 + \tau_2\tau_5 + \tau_2\tau_7 + \tau_4\tau_5 + \tau_4\tau_7 + \tau_6\tau_7)s^2 + (\tau_1 + \tau_3 + \tau_5 + \tau_7)s + 1$$

The design formulae for the equalizer can be obtained by coefficient matching between Equations (6) and (7). The resulting pole and zero parameters τ_i and α_j can be computed as:

$$\tau_1=0.19106, \tau_2=0.47905, \tau_3=0.64409, \tau_4=0.74214, \tau_5=0.84224, \tau_6=1.00706, \tau_7=1.49877, \alpha_5=0.662536, \alpha_7=0.337464. \qquad (8)$$

The equalizer is designed using the CMOS OTA cell in Figure 1, using identical unit OTAs to improve OTA matching and facilitate design automation, with nominal transconductance g_m of 1.35mS. The cut–off frequency of the equalizer is de-normalized to 300 MHz. Using the computed parameter values in (8), the capacitor values can be calculated, but parasitic capacitances associated with the OTA inputs and outputs must also be taken into account. For the circuit of Figure 1, the parasitic capacitance is about 0.1pF, so the actual capacitor values become C1=C8=0.1635pF, C2=C9=0.5608pF, C3=C10=0.7884pF, C4=C11=0.9237pF, C5=C12=1.0617pF, C6=C13=1.2891pF, C7=C14=2.0468pF.

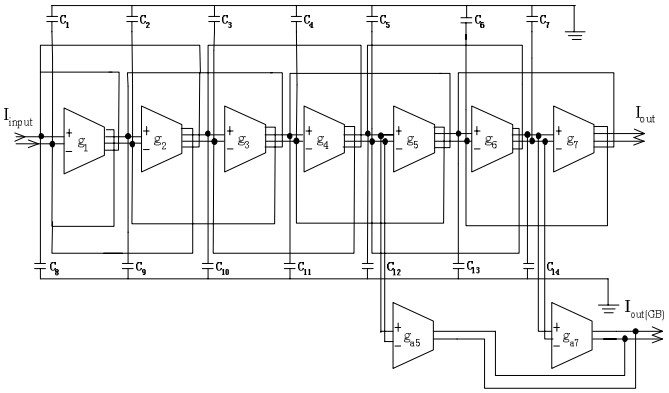

Figure 4 Seventh–order current–mode LF OTA-C equalizer with output summation OTA network

IV. SIMULATION RESULTS

The circuit was designed and simulated using BSIM 3v3 Spice models for a TSMC 0.18µm CMOS process available from MOSIS [10]. Figure 5 shows the magnitude response of the filter with and without gain boost. As seen in Figure 5, the cut–off frequency is 301MHz and the gain boost of the filter is about 5.2 dB. The DC gain of the filter is low, due to low OTA output resistance, but this problem can be solved by increasing the gain of the automatic gain control (AGC) circuit in the HDD read channel circuit. The tuning range of the cut–off frequency without gain boost is 260–320MHz. The total power consumption of the filter is about 210mW at 300MHz for a single 2.5V power supply.

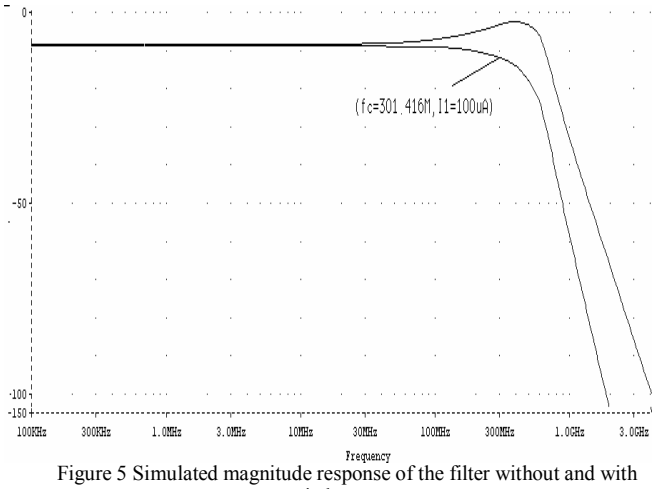

Figure 5 Simulated magnitude response of the filter without and with gain boost

The filter group delay (Figure 6) has little variation up to 1.5 times the cut–off frequency. The group delay ripple for $1/5f_c \le f \le 1.5\ f_c$ is 4.5%, with the group delay variation below ±125ps over the whole tuning range. This is well within the limit of the read channel filter specification. Simulations of the filter show a total harmonic distortion (THD) of less than 1% with a single input tone of 1350µA at 10MHz. The dynamic range is 66dB at f_c=300MHz.

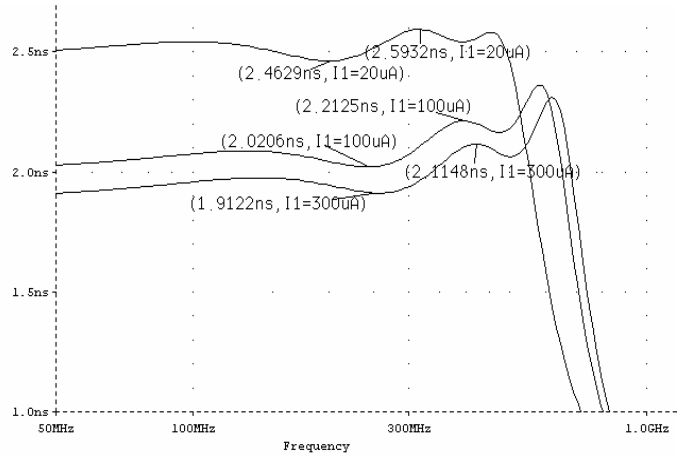

Figure 6 Simulated group delay response at f_c=260MHz, 300MHz 320MHz, respectively.

V. CONCLUSIONS

A CMOS 300MHz current–mode seventh–order 0.05° linear phase leap–frog filter with integral 5dB gain boost has been described. A linear multiple–output OTA based on source degeneration topology with a transconductance of 1.35mS has been used. Simulation results using 0.18µm CMOS technology with 2.5V V_{dd} have yielded a frequency tuning range of 260–320MHz, dynamic range of 66dB, and group delay ripple of 4.5%. The current–mode LF equalizer is suitable for hard disk read channels. The gain of filter is relatively low due to finite output impedance of the OTAs. Output resistances can be improved using negative resistance techniques, at the cost of addition power and chip area. Therefore, a tradeoff exists. Finally, the comparison with pre-published circuits is given in Table 1.

Table 1 COMPARISON WITH OTHER 7TH-ORDER FILTER DESIGNS

Reference	Range MHz	GDR	DR	PC mW
[3]	8-32	7%	55dB	322
[4]	50-150	4%	65dB	216
This work	260-320	4.5%	66dB	210

GDR = group delay ripple; DR = dynamic range; PC = power consumption

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