

A 2V 0.25 μ m CMOS 250MHz Fully-differential Seventh-order Equiripple Linear Phase LF Filter

Masood-ul-Hasan
School of ECEE
University of Hertfordshire,
Hatfield, Herts, AL10 9AB, UK
m.hasan@herts.ac.uk

Yichuang Sun
School of ECEE
University of Hertfordshire,
Hatfield, Herts, AL10 9AB, UK
y.sun@herts.ac.uk

Abstract— A fully-differential seventh-order 0.05° equiripple linear phase low-pass filter based on multiple loop feedback (MLF) leapfrog (LF) topology is presented for read/write channels. The filter is designed and simulated with the proposed fully balanced, highly linear operational transconductance amplifier (OTA). This OTA contains two complementary differential cross-coupled input pairs and a pair of regulated cascode output in order to achieve both low-distortion and wide dynamic range in high-frequency operation. Simulations in 0.25 μ m CMOS show that the cutoff frequency of the low pass filter without and with gain boost ranges from 50 to 150MHz and 65 to 250MHz respectively, dynamic-range is over 65dB and total harmonic distortion is less than 40dB. The group delay ripple is less than 5% for frequencies up to 1.5 times of the cutoff frequency, and for a 2-volt power supply, the maximum power consumption is 216mW.

I. INTRODUCTION

Filters are an important signal processing building block in mixed-signal integrated circuits (ICs). Modern computer and communication systems demand for high performance filters with attractive features. For example, high-performance high-frequency filters are required for read/write channel equalization in computer hard-disk drive systems and intermediate-frequency (IF) filtering for communication systems. Continuous-time operational transconductance amplifier and capacitor (OTA-C) filters have been shown to perform well in high frequency applications [1]. Unlike switched-capacitor filters, OTA-C filters do not suffer from the switching noise problem and do not need pre- or post-filtering. For these reasons OTA-C filters have become the preferred choice for filtering tasks in mixed-signal ICs. In recent years, several integrated continuous-time filters with high frequency range and low power consumption have been realized successfully and used for read/write channels in hard disk drive systems [2-9]. Most of the filters are based on the cascade structure. As is well known, the ladder-based topology has very low sensitivity, but can implement transmission zeros only on imaginary axis. The cascade topology can be used to realize

a filter with arbitrary transfer functions, but sensitivity is higher, in particular, as filter order increases. One of the solutions is to use the multiple loop feedback (MLF) structure [1-3]. The single-ended MLF OTA-C filter based on the leapfrog (LF) configuration for read channel application has been discussed in [3]. However, in mixed-signal SoC environment, digital switching noise signals will be injected into the analog circuitry through chip parasitics, degrading the performance of the analog circuits. To combat this problem, fully-differential, rather than signal-ended, circuitry is normally used [10].

A fully-balanced OTA-C filter design can ensure a completely symmetrical layout such that parasitic injections will couple perfectly equally into both the signal paths and appear as a common-mode signal. Thus, very high common-mode rejection ratio can be achieved and both even-order harmonic distortion components and effects of power supply noise can be reduced. In this paper we therefore present the design of a fully-balanced read/write channel equiripple linear phase OTA-C filter based on the MLF LF architecture. For this a new high performance fully-differential OTA is proposed. The designed filter has potential commercial application in hard disk drive systems. Its most important specification is the linearity on its phase response. Our design is targeted for a cut-off frequency of 250MHz with accurate linear phase and programmable gain boost.

The fully-differential OTA is discussed in Section II. The seventh-order equiripple group delay low-pass filter with finite real-axis zeros is presented in Section III. Filter simulation results are given in Section IV, and finally conclusions are summarized in Section V.

II. OPERATION TRANSCONDUCTANCE AMPLIFIER

For high-frequency operation, large transconductances are needed for the implementation of filter poles. BiCMOS technology based filters have been reported in [5, 6] but they have parasitic poles and high power consumption. To fulfill filter requirements in CMOS technology both parasitic poles and power consumption must be reduced. In this paper, a fully-balanced OTA shown in Fig. 1 is used.

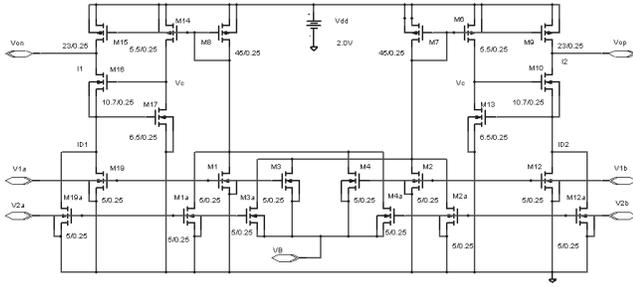


Fig.1 Fully-balanced OTA unit cell with two differential inputs and regulated cascode output stage (RGC).

The OTA is based on dual cross-coupled differential pairs with current tracking regulated cascode output stage. The cross-coupled input pairs enhance the OTA transconductance linearity and overcome the conflict between tuning and common-mode input range as occurred in OTA based on source-coupled pairs. The regulated output stage increases dynamic range and output voltage swing and the cascode stage compensates the GBW product and frequency behavior. Assume that all the input transistor pairs M_1 - M_4 and M_{1a} - M_{4a} are identical and operate in saturation region. Neglecting second-order effects, currents I_1 and I_2 are given by

$$I_1 = I_{1d} + I_{4d} + I_{1da} + I_{4da} \quad (1)$$

$$I_1 = k \left[\begin{aligned} &(V_{gs1} - V_t)^2 + (V_{gs4} - V_t)^2 \\ &+ (V_{gs1a} - V_t)^2 + (V_{gs4a} - V_t)^2 \end{aligned} \right] \quad (2)$$

$$I_1 = k \left[\begin{aligned} &(V_{1a} - V_t)^2 + (V_{1b} - V_B - V_t)^2 + \\ &(V_{2a} - V_t)^2 + (V_{2b} - V_B - V_t)^2 \end{aligned} \right]$$

Similarly,

$$I_2 = k \left[\begin{aligned} &(V_{1b} - V_t)^2 + (V_{1a} - V_B - V_t)^2 \\ &+ (V_{2b} - V_t)^2 + (V_{2a} - V_B - V_t)^2 \end{aligned} \right] \quad (3)$$

where $k = 0.5\mu C_{ox}(W/L)_n$ is the transconductance parameter, and μ , C_{ox} , W and L are the mobility, oxide capacitance per unit area, and channel width and length, respectively.

The final output is taken from the drain of biasing transconductance elements. The current mirror output of I_1 and I_2 is set by the drain voltages of transistor M_{12} and M_{19} . The value of the mirrored current is small enough so that for the range of input gate voltage considered both transistors always operate in their triode region, thus ensuring a reasonably large linear range. The voltage-current relationship is given by

$$I_{D1} = I_{d19} + I_{d19a}$$

$$I_{D1} = k \left[(V_{1a} - V_t)^2 V_C - \frac{1}{2} V_C^2 + (V_{2a} - V_t)^2 V_C - \frac{1}{2} V_C^2 \right] \quad (4)$$

and similarly,

$$I_{D2} = k \left[(V_{1b} - V_t)^2 V_C - \frac{1}{2} V_C^2 + (V_{2b} - V_t)^2 V_C - \frac{1}{2} V_C^2 \right] \quad (5)$$

Note that the positive and negative output currents are given by

$$I_{op} = I_2 - I_{D2} \quad (6)$$

$$I_{on} = I_1 - I_{D1} \quad (7)$$

Using Equations (2)-(7) we can derive the differential output current of the OTA as

$$I_{out} = I_{op} - I_{on} \quad (8)$$

$$I_{out} = k \left[(V_{1a} - V_{1b}) + (V_{2a} - V_{2b}) \right] (V_C - 2V_B)$$

$$I_{out} = k V_A V_{id} = g_m V_{id} \quad (9)$$

where $V_{id} = (V_{1a} - V_{1b}) + (V_{2a} - V_{2b})$ is the differential input voltage, $V_A = V_C - 2V_B$ where V_B is the bias voltage and $g_m = k V_A$ is the transconductance. Equation (9) shows that the transconductance of the proposed OTA is linear and tunable by varying bias voltage.

III. FILTER ARCHITECTURE AND SYNTHESIS

Design of all-pole and transmission zero MLF OTA-C filters have been well investigated in [1, 10]. The seventh-order fully-balanced MLF LF filter structure with input distribution OTA network to realize gain boost zeros is shown in Fig.2.

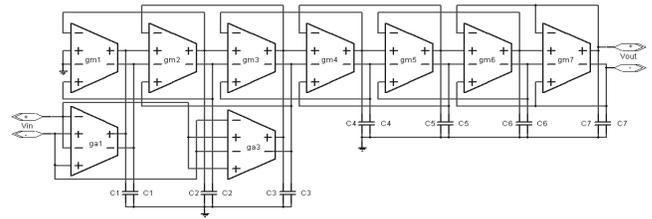


Fig.2 Seventh-order low-pass MLF LF filter structure with gain boost zeros.

The transfer function for the seventh-order LF filter with gain boost in Fig.2 can be derived using nodal equation as

$$H(s) = \frac{V_{out}}{V_{in}} = \frac{N(s)}{D(s)} \quad (10)$$

where

$$N(s) = \beta_3 \tau_1 \tau_2 s^2 + (\beta_3 - \beta_1)$$

and

$$\begin{aligned}
D(s) = & \tau_1\tau_2\tau_3\tau_4\tau_5\tau_6\tau_7 s^7 + \tau_1\tau_2\tau_3\tau_4\tau_5\tau_6 s^6 + \\
& (\tau_1\tau_2\tau_3\tau_4\tau_5 + \tau_1\tau_2\tau_3\tau_4\tau_7 + \tau_1\tau_2\tau_3\tau_6\tau_7 + \\
& \tau_1\tau_2\tau_5\tau_6\tau_7 + \tau_1\tau_4\tau_5\tau_6\tau_7 + \tau_3\tau_4\tau_5\tau_6\tau_7) s^5 + \\
& (\tau_1\tau_2\tau_3\tau_4 + \tau_1\tau_2\tau_3\tau_6 + \tau_1\tau_2\tau_5\tau_6 + \tau_1\tau_4\tau_5\tau_6 + \tau_3\tau_4\tau_5\tau_6) s^4 \\
& + (\tau_1\tau_2\tau_3 + \tau_1\tau_2\tau_5 + \tau_1\tau_2\tau_7 + \tau_1\tau_4\tau_7 + \tau_1\tau_6\tau_7 \\
& + \tau_3\tau_4\tau_5 + \tau_3\tau_4\tau_7 + \tau_3\tau_6\tau_7 + \tau_5\tau_6\tau_7) s^3 + \\
& (\tau_1\tau_2 + \tau_1\tau_4 + \tau_1\tau_6 + \tau_3\tau_4 + \tau_3\tau_6 + \tau_5\tau_6) s + \\
& (\tau_1 + \tau_3 + \tau_5 + \tau_7) s + 1
\end{aligned}$$

where $\beta_j = g_{aj}/g_{mj}$ and $\tau_j = C_j/g_{mj}$ are the zero and pole parameters respectively. The values of time constants τ_j and gain boost coefficients β_j can be determined by comparing the coefficients in Equation (10) with those of the desired transfer function in Equation (11).

$$H_d(s) = \frac{A_2 s^2 - A_0}{B_7 s^7 + B_6 s^6 + B_5 s^5 + B_4 s^4 + B_3 s^3 + B_2 s^2 + B_1 s + 1} \quad (11)$$

The calculation formulas are derived as

$$\begin{aligned}
\tau_7 = \frac{B_7}{B_6} \quad \tau_6 = \frac{B_6}{B_5 - B_4 \tau_7} \\
\tau_5 = \frac{B_5 - B_4 \tau_7}{B_4 - (B_3 - B_2 \tau_7) \tau_6} \\
\tau_4 = \frac{B_4 - (B_3 - B_2 \tau_7) \tau_6}{B_3 - B_2 \tau_7 - [B_2 - (B_1 - \tau_7) \tau_6] \tau_5} \\
\tau_3 = \frac{B_3 - B_2 \tau_7 - [B_2 - (B_1 - \tau_7) \tau_6] \tau_5}{B_2 - (B_1 - \tau_5 - \tau_7) \tau_4 - (B_1 - \tau_7) \tau_6} \\
\tau_2 = \frac{B_2 - (B_1 - \tau_3 - \tau_5) \tau_7 - (B_1 - \tau_7) \tau_6}{B_1 - \tau_3 - \tau_5 - \tau_7} \\
\tau_1 = B_1 - \tau_3 - \tau_5 - \tau_7 \\
\beta_3 = \frac{A_2}{\tau_1 \tau_2} \quad \beta_1 = A_0 + \beta_3
\end{aligned} \quad (12)$$

The normalized characteristic of a seventh-order low-pass filter with 3-dB gain-boost real zeros at the cut-off frequency is given by [3]

$$H(s) = \frac{(s^2 - 1)}{D(s)} \quad (13)$$

where

$$\begin{aligned}
D(s) = & 0.055617s^7 + 0.291094s^6 + \\
& 1.095656s^5 + 2.554179s^4 + 4.255922s^3 \\
& + 4.676709s^2 + 3.176156s + 1
\end{aligned}$$

To realize the function in Equation (13) for the cut-off frequency of 150MHz, the fully-balanced OTA in Fig.2 are designed with identical transconductance g_m of value of 980 μ S to improve the tracking and performance of transconductance with respect to the tuning voltage. Matching Equations (11) and (13) to find A_j and B_j and using Equation (12), the values of capacitances from C_1 to C_7 for the seventh-order low-pass equiripple linear phase filter with real zeros are calculated as

$$\begin{aligned}
C_1 = 2.25\text{pF} \quad C_2 = 1.49\text{pF} \\
C_3 = 6.49\text{pF} \quad C_4 = 1.07\text{pF} \\
C_5 = 0.93\text{pF} \quad C_6 = 2.91\text{pF} \\
C_7 = 1.11\text{pF} \\
g_{m1,2,4,5} = 980\mu\text{S} \quad g_{m3} = 5 \times 980\mu\text{S} \\
g_{m6,7} = 4 \times 980\mu\text{S} \quad g_{a1} = 328\mu\text{S} \quad g_{a3} = 672\mu\text{S}
\end{aligned} \quad (14)$$

IV. SIMULATION RESULTS

The proposed OTA in Fig.1 was used for simulation of the seventh-order linear phase filter shown in Fig.2. The OTA structure is very simple, therefore there is no need for using common-mode feedback circuitry. Due to the small dimensions of the transistors, parasitic node capacitances are subtracted from the values of C_j 's in Equation (14). The OTA and the filter were simulated with the TSMC 0.25 μ m CMOS process model using the following key model parameters, $V_{no} = 0.407736\text{V}$, $V_{tpo} = -0.587912\text{V}$, $K_n = 121.9\mu\text{A}/\text{V}^2$ and $K_p = -23.2\mu\text{A}/\text{V}^2$ provided by the MOSIS. The total power consumption (PC) of the seventh-order low pass filter is only 216mW for a single 2V supply. Fig.3 shows the tuning ranges of the cutoff frequencies without and with gain boost are 50-150 MHz and 65 - 250 MHz, respectively.

The boosted gain has been maintained throughout the tuning range with the tolerance of $\pm 0.25\text{dB}$. Fig.3 also indicates that the magnitude response of the filter decreases as bias voltage V_B decreases. This is due to the finite output conductance of the OTA.

The filter phase response is fairly linear, as can be seen from Fig.4, the group delay has a very small variation up to about twice the cut-off frequency. The group delay ripple (GDR) is calculated as 4.5% by using the definition given in [7] and this is well within the limit of read/write channel filter specification.

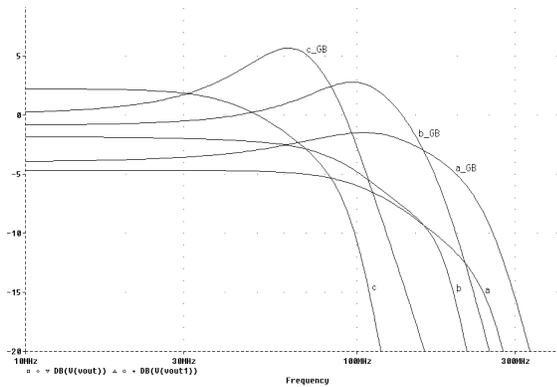


Fig.3 Simulated magnitude response of the filter without and with gain boost. GB stands for gain boost. Curves a, a_GB, b, b_GB and c, c_GB correspond to tuning voltages of $V_B = 50\text{mV}$, 110mV and 130mV , respectively.

Simulation results of the filter have shown a total harmonic distortion (THD) of less than 1% for a single tone of 250mVpp at 10MHz . The overall filter input-referred spectral noise density is around $9.14 \times 10^{-18} \text{ V}^2/\text{Hz}$.

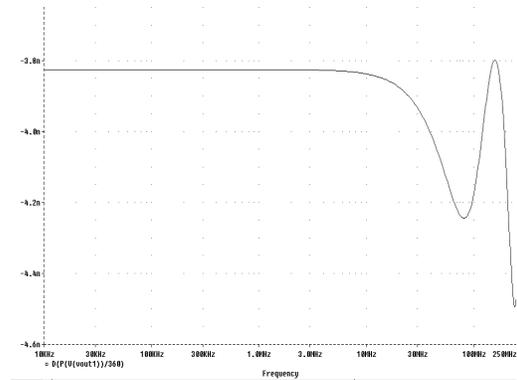


Fig.4 Filter group delay response, the ripple is less than 700ps up to 300MHz .

been used. Simulation results in 2V $0.25\mu\text{m}$ CMOS show that group delay variation is around 4.5% , in-band harmonic distortion is less than -40dB and power consumption of the entire filter system is 216mW . These results have shown that the MLF LF filter is well suitable for hard disk drive read/write channel applications.

TABLE I. COMPARISON WITH OTHER 7TH-ORDER FILTER DESIGNS

Parameters	Specifications				
	[2]	[8]	[9]	[3]	This work
Design By	Eq.Rip	Eq.Rip	L.Phase	Eq.Rip	Eq.Rip
Filter Type	IFLF	-	Cascade	LF	LF
Filter Conf.	IFLF	-	Cascade	LF	LF
Range MHz	5-20	0-100	0-200	8-32	50-150
GBR MHz	10-47	-	-	15-100	65-250
Fc Stability	$\pm 5\%$	$\pm 5\%$	$\pm 5\%$	$\pm 5\%$	$\pm 5\%$
GDR	3-6dB	$< 4.6\%$	$< 4\%$	$\pm 7\%$	$\pm 4.5\%$
NBW MHz	-	-	200	500	1GHz
Input	1Vpp	450mV	500mV	500mV	250mV
SNR	-	-	$> 40\text{dB}$	$> 60\text{dB}$	$> 65\text{dB}$
THD	$< -46\text{dB}$	$< -40\text{dB}$	$< -44\text{dB}$	$< -40\text{dB}$	$< -40\text{dB}$
DR	-	-	50dB	55dB	65dB
PC mW	120	210	60	322	216
P.Supply	5V	-	$\pm 1.5\text{V}$	5V	2V
CMOSTech	2μ	0.25μ	0.35μ	0.25μ	0.25μ

GBR=gain boost range; NBW=noise bandwidth

Results from this work and some previous designs are summarized in Table I. The performances of group delay ripple (GDR), signal to noise ratio (SNR), total harmonic distortion (THD), and dynamic range (DR) of our filter are equal or better than all other realizations. The equalizer described in this work is the only MLF LF equalizer known so far that realizes a cut-off frequency of up to 250MHz . This fully-balanced design has achieved performances all better than the single-ended design [3].

V. CONCLUSIONS

This paper has described a fully-balanced continuous-time seventh-order linear phase filter as required in a hard disk drive read/write channel. The filter is based on a multiple-loop feedback leapfrog structure for lower sensitivities. A dual differential pair OTA with cross-coupled input and a typically larger transconductance has

REFERENCES

- [1] T. Deliyannis, Y. Sun and J. K. Fidler. Continuous-time Active Filter Design, CRC Press, Florida, USA, 1999.
- [2] D. H. Chiang and R. Schaumann, "A CMOS fully-balanced continuous-time IFLF filter design for read/write channels", Proc. IEEE Int. Symp. Circuits and Systems, pp. 167-170, 1996.
- [3] H. W. Su and Y. Sun, "A CMOS 100MHz continuous-time seventh order 0.05° equiripple linear phase leapfrog multiple loop feedback G_m -C filter", IEEE Int. Symp. on Circuits and Systems, vol. 2, pp 17-20, May 2002.
- [4] G. A. De Veirman and R. Yamasaki, "A 27MHz programmable bipolar 0.05° equiripple linear phase low pass filter." in IEEE ISSCC Dig. Tech. paper, pp. 64-65, Feb. 1992.
- [5] B. E. Bloodworth, P. P. Siniscalchi, G. A. De Veirman, A. Jezdic, R. Pierson, and R. Sundaraman, "A 450-Mb/s analog front end for PRML read channels," IEEE Custom Integrated Circuits Conf., pp. 309-316, 1998.
- [6] N. Rao, V. Balan, and R. Contreras, "A 3V 10-100MHz continuous-time seventh-order equiripple linear phase filter," in IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. papers, pp.44-46, Feb. 1999.
- [7] W. Dehaene, M. S. J. Steyaert, and W. Sansen, "A 50-MHz standard CMOS pulse equalizer for hard disk read channels", IEEE J. Solid-State Circuits, vol. 32, No.7, pp.977-988, July 1997.
- [8] V. Gopinathan, M. Tarsia and D. Choi, "Design considerations and implementation of a programmable high-frequency continuous-time filter and variable-gain amplifier in sub micrometer CMOS", IEEE J. Solid-State Circuits, vol. 34, No.12, pp.1698-1707, Dec. 1999.
- [9] J. Silva-Martinez, J. Adut, J.M. Rocha-Perez, M. Robinson and S. Rokhsaz, "A 60-mW 200-MHz continuous-time seventh-order linear phase filter with on-chip automatic tuning system", IEEE J. Solid-State Circuits, vol. 38, No.2, pp.216-225, Feb. 2003.
- [10] Y. Sun and J. K. Fidler, "Fully-balanced structures of continuous-time MLF OTA-C filters", Proc. IEEE Int. Conf. Electronics, Circuits and Systems, pp. 157-160, 1998.