Low Noise, Low Distortion, High Frequency, Fully Differential CMOS Transconductor

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Abstract

This paper describes a CMOS transconductance element based upon two differential pairs whose outputs are summed to give a linear transfer characteristic. The circuit has been simulated using a 2μm process from MOSIS, and results show that with a single 5V supply, bandwidth in excess of 300MHz, THD below 0.7% for a $1V_{pk\text{-}pk}$ differential input signal, and dynamic range in excess of 70dB can be achieved.

I. Introduction

In recent years current-mode circuits have become increasingly important in high speed analogue applications. Fundamental to these circuits is the need for an accurate and tunable voltage to current converter, or transconductor. The transconductor is also a key element in high frequency continuous-time filters [1-3]. The most common transconductor is the source coupled pair. However this suffers from poor linearity, especially at high signal levels. Other problems may also occur such as conflicts between tuning range and common mode input range. Several techniques have been proposed in literature to overcome these problems [4-7], many of which rely on the use of the cross-coupled pair. However these circuits pay a penalty in terms of noise performance, and also may require the use of additional circuitry such as floating voltage sources.

The aim of this paper is to present an alternative structure which can provide a linear, low noise, fully differential transconductor in CMOS technology with a 5V supply. The basic structure described consists of two differential pairs arranged so that each pair has a non-linearity opposite to the other, i.e., one pair exhibits a gain compression whilst the other has a gain expansion [8].

The paper is laid out as follows; section II examines the theoretical aspects of the circuit design, and develops equations describing the DC transfer characteristic of the transconductor. In section III the practical aspects of the design are considered, including headroom, tuning range, and providing the circuit with an active load. Simulation results are presented in section IV and conclusions in section V.

II. Basic Principle, Structure and Analysis

Consider the MOS differential pair of Figure 1(a), whose circuit symbol is given in Figure 1(b). Assuming that all MOS devices have the same dimensions and operate in the saturation region, the transconductance can be derived as

$$g_{m1}=2k_1V_{cm1} \tag{1}$$

where k_1 is the transconductance parameter, which is given by

$$k_1=0.5\mu C_{ox}W/L \tag{2}$$

and V_{cm1} is the common mode bias voltage, given by

$$V_{cm1}=(V_{gs1}+V_{gs2})/2-V_T \tag{3}$$

where C_{ox} is the gate capacitance per unit area, V_{gs} is the gate-source voltage, and V_T is the threshold voltage. Equation (1) shows that the transconductance of the differential pair is determined by the bias voltage V_{cm1}. Unfortunately, when the differential pair is biased by a current source, V_{cm1} is modulated by the input signal in such a way as to produce a gain compression, which becomes worse at high input levels.

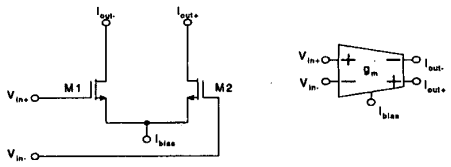

Figure 1. MOS differential pair (a) and its circuit symbol (b).

If another differential pair is added whose bias voltage V_{cm2} is controlled in such a way that

$$V_{cm2}=V_b-V_{cm1} \tag{4}$$

and the output currents of the two pairs are summed in the way of

$$I_{out}=I_{out1}+I_{out2} \tag{5}$$

then the transconductance of the new circuit will be linear and proportional to V_b.

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Such an arrangement is shown in Figure 2. The first differential pair (M1, M2) is biased by a current source and driven by the differential input signal V_{id}, and its outputs buffered by cascode transistors M3 and M4. The voltage gain from the inputs of the first pair to point X is

$$A_v=(k_1/k_3)^{1/2} \quad (6)$$

The second differential pair (M5, M6) is driven by the sources of transistors M3, M4. Hence the bias voltage for the second pair will be

$$V_{cm2}=V_b-(k_1/k_3)^{1/2}V_{cm1}-2V_T \quad (7)$$

Substituting equation (7) into $2k_5V_{cm2}$ gives an expression for the transconductance of the second pair,

$$g_{m2}=2k_5[V_b-(k_1/k_3)^{1/2}V_{cm1}-2V_T] \quad (8)$$

With the transconductance of the first pair given in equation (1), the total transconductance of the circuit in Figure 2 is then

$$g_m=g_{m1}+A_v(g_{m2})=2k_1V_{cm1}+(k_1/k_3)^{1/2}2k_5[V_b-(k_1/k_3)^{1/2}V_{cm1}-2V_T] \quad (9)$$

If $k_3=k_5$ the two terms containing V_{cm1} cancel out and equation (9) reduces to

$$g_m=2k_3(k_1/k_3)^{1/2}(V_b-2V_T) \quad (10)$$

This shows that the transconductance of the circuit as a whole is controlled by the bias voltage, V_b, and that linearity is dependant upon matching of transistors M3, M4, M5, and M6.

Suppose that $k_5=k_3+\Delta k$, where Δk is the mismatch error. From equation (10) we can write the modified transconductance as

$$g_m=2k_3(k_1/k_3)^{1/2}(V_b-2V_t)+2\Delta k(k_1/k_3)^{1/2}[V_b-(k_1/k_3)^{1/2}V_{cm1}-2V_T)] \quad (11)$$

Two effects can be observed. One is the change in g_m due to Δk and the other is the non-linearity caused by the mismatch error. In practice matching should be as close as possible.

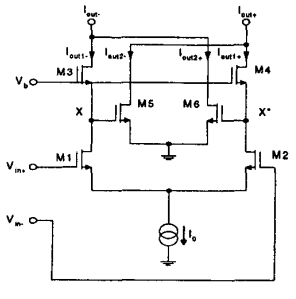

Figure 2. Linearised transconductor and analysis.

III. Complete Transconductor Circuit and Performance Analysis

To implement the circuit of Figure 2 an active load must be added, a common mode feedback circuit is needed for high performance, and some modification is required to accommodate a single 5V supply. The complete circuit is shown in Figure 3, which contains three major parts: input, output and common mode feedback circuits. Analysis of the practical performances is now carried out.

A. Modifications for Low Voltage Operation

The minimum voltage required by the input differential pair in order to operate properly is

$$V_{IS(min)}=V_{id(max)}+V_{ic}+V_T+V_{Io(sat)} \quad (12)$$

where $V_{id(max)}$ is the maximum differential input voltage, V_{ic} is the common mode input range, and $V_{Io(sat)}$ is the saturation voltage of the tail current source. As an example, allowing a differential input range of 1.2V, a common mode input range of 1V, and typical values of V_T and $V_{Io(sat)}$ gives

$$V_{IS(min)}=1.2+1+0.8+0.4=3.4V \quad (13)$$

Similarly the second pair requires

$$V_{OS(min)}=V_{id(max)}(k_1/k_3)^{1/2}+V_T+V_{load(sat)}+\Delta V_b+V_o/2 \quad (14)$$

where $V_{load(sat)}$ is the saturation voltage of the output load, V_o is the required output compliance, and ΔV_b is the voltage required for tuning. This equation remains true whilst $V_o/2<V_T$. With a single supply the voltage available for the output stage will be

$$V_{OS}=V_{DD}-V_{IS} \quad (15)$$

where V_{DD} is the supply voltage. With a 5V supply and the values given in equation (13) the output stage will only have 1.6V of headroom, hence current mirrors comprised of transistors M7-M10 are added. This has the further advantage that P-channel transistors can be chosen for the input pair without unnecessarily increasing the chip area.

B. Common-Mode Feedback Circuit

The transconductor also requires an active load, and in order to obtain a fully differential structure a common mode feedback (CMFB) circuit is required. This is based on a circuit originally due to Whatly [9], and comprises transistors M11-M17. The currents flowing in the output stage are described by equation (5), that is,

$$I_{out}=I_{out1}+I_{out2}$$

I_{out1} is equal to I_0, but I_{out2} is dependent upon the bias voltage V_b, and also varies with the input signal V_{id}. Hence,

$$I_{out2}=k_5V^2_{cm2} \quad (16)$$

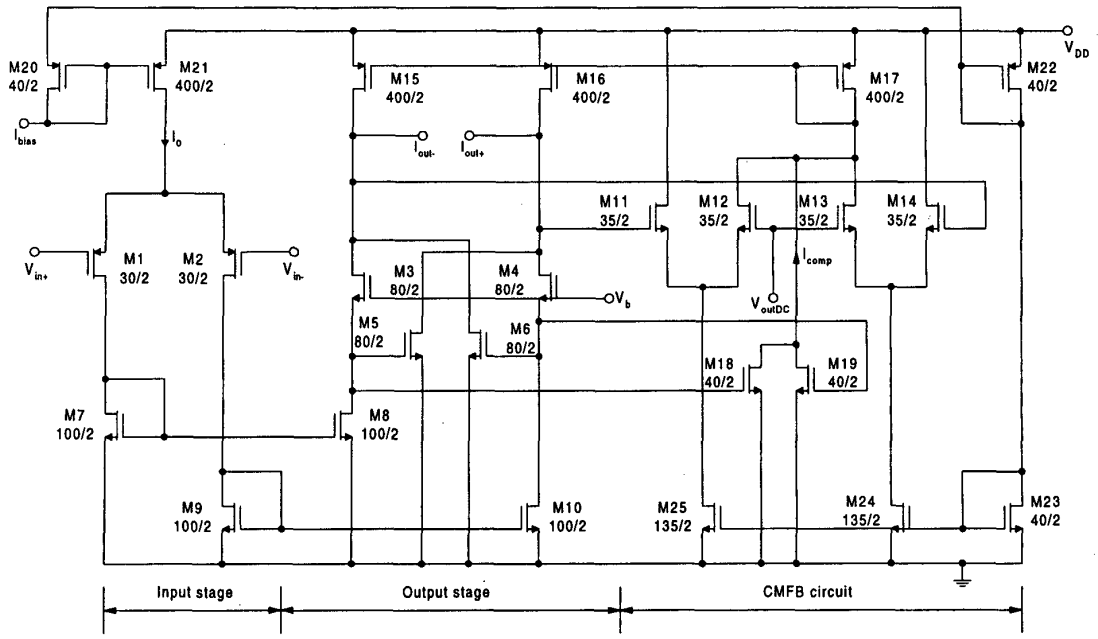

Figure 3. Complete circuit of transconductor.

which implies the addition of a compensating current I_{comp} controlled by V_{cm2}. This is achieved by the addition of transistors M18-M19.

The quiescent voltage present at the output is controlled by the terminal marked V_{outDC}.

C. Tuning Range and Linear Input Range

With the addition of the current mirrors M7-M10 the voltage available for tuning can be defined as

$$\Delta V_b = V_{DD} - V_{id(max)} (k_1/k_3)^{1/2} - 2V_T - V_{load(sat)} - V_o/2 \qquad (17)$$

This shows that for a given input range there are two possible schemes for increasing the tuning range; by reducing the required output compliance, or by adjusting the ratio k_1/k_3. Equation (10) shows there is some degree of freedom in the choice of the ratio k_1/k_3. Making the value of k_1/k_3 less than unity will give an increase in tuning range for a given $V_{id(max)}$, and will also lead to an increase in efficiency since the current in the input stage will be reduced. In practice, however, low values of k_1/k_3 lead to inaccuracies in the CMFB circuit, since the compensating current becomes much larger than I_0.

Conversely k_1/k_3 can be made greater than unity, allowing larger input transistors for a given transconductance, which will lead to an improved noise performance.

It can also be seen from equation (10) that the current source I_0 does not appear in the transfer characteristic of the transconductor. This implies that adjustment of I_0 merely controls the linear input range, an advantage in the sense that the g_m tuning range and input voltage range can be controlled independantly by V_b and I_0 respectively. However the increase in the current through transistors M3 and M4 due to an increase in I_0 will reduce the headroom in the output stage.

D. Frequency Response

Analysis of the circuit of Figure 2 shows that the dominant frequency limitation is due to the capacitances associated with the gates of transistors M5, M6. If the transconductor is driving a short circuit this causes a pole to occur at approximately

$$p_1 = -k_5(V_{gs4} - V_T)/(C_{gs5} + C_{gd5}) \qquad (18)$$

The addition of the current mirrors M7-M10 in the complete circuit of Figure 3 causes another pole to occur at

$$p_2 = -k_7(V_{gs7} - V_T)/\{C_{gs7} + C_{gs8} + [(k_8/k_4)^{1/2} + 1]C_{gd8}\} \qquad (19)$$

IV. Simulation

The circuit of Figure 3 was simulated in PSPICE using level 2 models in 2μm process from MOSIS with V_{Tn}=0.855V, V_{Tp}=-0.8112V, k_{on}=53.6uA/V and k_{op}=21.05uA/V. Transistor dimensions are as shown in Figure 3. Output compliance is chosen as $1V_{pk\text{-}pk}$ and V_{outDC} as 3.7V. Dynamic range is defined as

$$DR = 20\log V_{max}/(V^2_{ni})^{1/2} \qquad (20)$$

where V_{max} is the input level where THD=1% and $(V^2_{ni})^{1/2}$ is the mean-square-root input noise. Since the bias of the input pair is held constant regardless of the transconductance, the noise figure and hence the DR remains fairly constant over the whole tuning range. Simulation results are summarised in Table 1. It can be seen that the transconductor has very low noise of below 250μV and very large dynamic range of over

70dB. The power consumption is less than 40mW. The transconductance can be tuned from 166 to 575μS.

Figure 4 shows the simulation result of the transconductance as a function of the input voltage. From the figure, the input voltage range of 1.2V and the tuning range of 3.5 can be observed.

Table 1 Simulation results.

Transconductance range (V_b=2.0V to 3.6V)	166-575μS
Integrated input noise (1-300MHz) @V_b=2.0V	253μV
Integrated input noise (1-300MHz) @V_b=3.6V	230μV
Dynamic range (THD=-40dB, @10MHz, V_b=2.0V)	74dB
Dynamic range (THD=-40dB, @10MHz, V_b=3.6V)	77dB
Power consumption at V_b=2.0V	8.24mW
Power consumption at V_b=3.6V	41.5mW
-3dB frequency at V_b=2.0V	435MHz
-3dB frequency at V_b=3.6V	373MHz

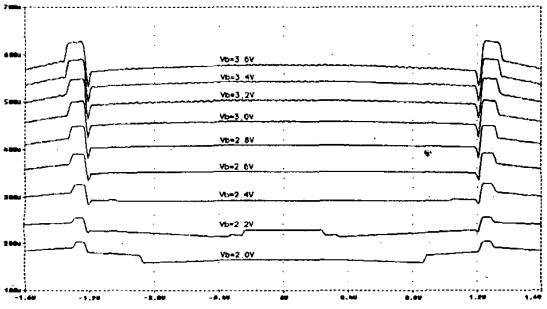

Figure 4. Transconductance (S) as a function of V_{id} (V).

The simulated frequency response is presented in Figure 5, from which we can see that the bandwidth of the transconductor is in excess of 300MHz, and -3dB frequencies vary from 435MHz to 373MHz for V_b=2.0V to V_b=3.6V.

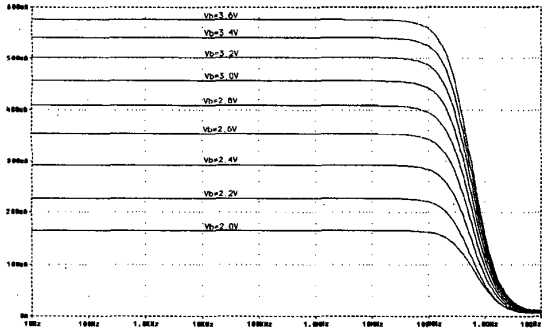

Figure 5. Frequency response: I_{out} against frequency.

The THD as a function of V_b with V_{id}=1$V_{pk\text{-}pk}$ was also simulated and is given in Figure 6. In the whole tuning range of V_b the THD is smaller than 0.7% and for V_b in the range from 2.4V to 2.6V THD is less than 0.4%.

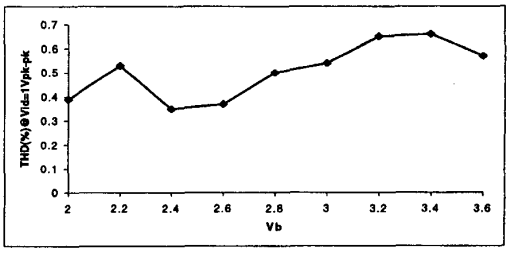

Figure 6. THD as a function of V_b: V_{id}=1$V_{pk\text{-}pk}$.

V. Conclusions

A fully differential transconductor operating from a single 5V supply in 2μm CMOS technology, suitable for high frequency filtering applications has been presented. The transconductor uses a novel linearisation technique to produce low distortion at the output. The use of a single MOS differential pair at the input gives the circuit a superior dynamic range. Simulation results have shown good performance from the transconductor in the megahertz range.

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