Oscillation-Based Test Structure and Method for OTA-C Filters

Masood-ul-Hasan
School of ECEE
University of Hertfordshire,
Hatfield, Herts, AL10 9AB, UK
m.hasan@herts.ac.uk

Yichuang Sun
School of ECEE
University of Hertfordshire,
Hatfield, Herts, AL10 9AB, UK
y.sun@herts.ac.uk

Abstract— **This paper describes a design for testability technique for operational transconductance amplifier and capacitor filters using an oscillation-based test topology. The oscillation-based test structure is a vectorless output test strategy easily extendable to built-in self-test. The proposed methodology converts filter under test into a quadrature oscillator using very simple techniques and measures the output frequency. The oscillation frequency may be considered as a digital signal and it can be evaluated using digital circuitry therefore the test time is very small. These characteristics imply that the proposed method is very suitable for catastrophic and parametric faults testing and also effective in detecting single and multiple faults. The validity of the proposed method has been verified using comparison between faulty and fault-free simulation results of two integrator loop and Tow-Thomas filters. Simulation results in 0.25µm CMOS technology show that the proposed oscillation-based test strategy for OTA-C filters has 87% fault coverage and with a minimum number of extra components, requires a negligible area overhead.**

I. INTRODUCTION

Designs-for-testability techniques for digital systems have been developed for over three decades. Advances in technology, increasing integration and mixed-signal designs demand similar techniques for testing analogue circuitry. DFT for analogue circuits is one of the most challenging jobs in mixed-signal ASIC design [1]. A large portion of test development time and total test time is spent on the analogue circuit because of the broad specifications and the strong dependency of the circuit parameters on component variation [2]. Testing of analogue circuits based on circuit functionality [3] and its specification under typical operational conditions may result in poor fault coverage, long testing time and the requirement for dedicated test equipment [4]. A number of test methods can be found in the literature [5] using functional testing, DC testing, power supply quiescent current monitoring and digital signal processing techniques. All these methods depend on the selection of a suitable test vector. As the complexity of the analogue circuit increases, the problem of generating test vectors assuring high fault coverage and short test time becomes more critical. Therefore an efficient DFT procedure is required which uses a single signal as input or a self-generated input signal and has access to several internal nodes and must contain sufficient information about the circuit under test in the output [6]. The DFT of analogue circuits can be generally divided into two categories; the first deals with controllability and observability of the internal nodes and the second is to convert the circuit under test (CUT) function and generate an output signal which contains the CUT performance to determine its malfunction. Oscillation-based test (OBT) procedures for analogue circuits, based on transformation of the CUT to an oscillator have been recently introduced [7]. The oscillation-based DFT structure uses vectorless output frequency comparison between fault-free and faulty circuits and consequently reduces test time, test cost, test complexity and area overhead. Furthermore, the testing of high frequency filter circuits become easier because no test vector is required for this test method. In this paper we present an easily implemented and low-cost DFT scheme for OTA-C filters based on the oscillation-based test methodology. The proposed strategy shows greatly improved detection and diagnostic capabilities associated with a number of catastrophic and parametric faults. Application of the oscillation-based DFT scheme to two integrator loop and Tow-Thomas biquad is discussed, because these structures are commonly used as building blocks for high order filters. The format of the paper is as follows; Filter to oscillator conversion schemes are briefly discussed in Section 2. Analogue fault modelling is presented in Section 3. Test simulation results are given in Section 4, and Section 5 contains conclusions.

II. CONVERSION OF FILTERS INTO OSCILLATORS FOR TEST

In this section we will present conversion techniques for the filter under test into an oscillator using only MOS (S_n and S_P) switches. The methods for two integrator loop and Tow-Thomas filters are proposed and discussed.

A. Two Integrator Loop Filter

Second or higher order systems for any type of OTA-C filter have the potential for oscillation. This ability can be used to convert the filter under test (FUT) to an oscillator by establishing the oscillation condition in its transfer function using the strategy shown in Fig.1.

In the normal filter mode, switch S_p is closed and both S_n switches are open, the circuit under test behaves as a normal filter with very small performance degradation. The transfer function of the low pass second order filter can be derived as

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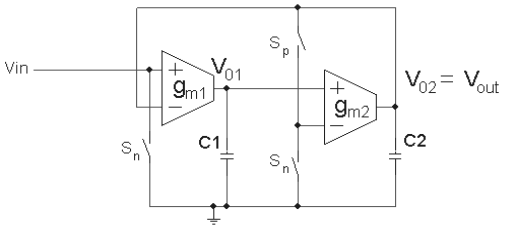

Fig.1. Block diagram of testable two integrator loop filter based on the OBT method

$$H(s) = \frac{Vo}{Vin} = \frac{\frac{g_{m1}g_{m2}}{C_1C_2}}{s^2 + \frac{g_{m2}}{C_2}s + \frac{g_{m1}g_{m2}}{C_1C_2}} \quad (1)$$

where the cut-off frequency ω_0 and the quality factor Q are given by

$$\omega_0 = \sqrt{\frac{g_{m1}g_{m2}}{C_1C_2}} \quad Q = \sqrt{\frac{C_2g_{m1}}{C_1g_{m2}}} \quad (2)$$

To put the network into oscillation with constant amplitude, the pole must be placed at the imaginary $j\omega$ axis. The filter network will convert into an oscillator, as both S_n switches are closed and S_p open. The characteristic equation of the resulting oscillator can be described as

$$s^2 + \frac{g_{m1}g_{m2}}{C_1C_2} = 0 \quad (3)$$

with the poles given by

$$p_{1,2} = \pm j\sqrt{\frac{g_{m1}g_{m2}}{C_1C_2}} \quad (4)$$

B. Tow-Thomas Filter

The Tow-Thomas (TT) second-order OTA-C filter consists of an ideal integrator and a lossy integrator in a single loop. The TT-filter has low sensitivity to parasitic capacitances and is suitable for operation at higher frequencies. The Tow-Thomas biquad is the most popular biquad in practice. It is easily converted into an oscillator using only MOS switches as shown in Fig.2.

For the circuit in Fig.2 when the switch S_n is open and S_p is closed. It will be a normal TT filter. The transfer function of the low pass second order TT-filter can be derived as

$$H(s) = \frac{Vo}{Vin} = \frac{\frac{g_{m1}g_{m2}}{C_1C_2}}{s^2 + s\frac{g_{m3}}{C_2} + \frac{g_{m1}g_{m2}}{C_1C_2}} \quad (5)$$

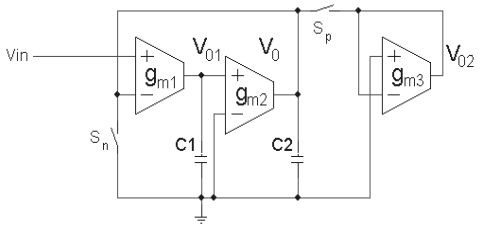

Fig.2. Block diagram of testable Tow-Thomas filter based on the OBT method

where the cut-off frequency ω0 and the quality factor Q are given by

$$\omega_0 = \sqrt{\frac{g_{m1}g_{m2}}{C_1C_2}} \quad Q = \frac{1}{g_{m3}}\sqrt{\frac{g_{m1}g_{m2}C_2}{C_1}} \quad (6)$$

To put the TT filter into oscillation with constant amplitude the quality factor must be sufficiently high. In the other words the network will oscillate with resonant frequency ω0 if quality factor Q→∞. By closing the switch S_n, and opening S_P, the filter network will convert into an oscillator and the poles of the resulting oscillator are given by:

$$p_{1,2} = \pm\sqrt{\frac{g_{m1}g_{m2}}{C_1C_2}} \quad (7)$$

From equation (7) we can see that the condition for oscillation will be satisfied if gm3 =0 without affecting the resonant frequency. In Fig.2 this is realised equivalently by switching off the gm3 OTA

C. Effects of MOS Switches Parasitics

Converting the FUT into an oscillator requires modification of the feedback path of the filter. In the domain of analogue circuit design it is not a simple matter to break loops by inserting MOS switches (S_n and S_p) in metalised track connections. The series resistance of a MOS transistor is several orders of magnitude greater than the resistance of the metal track. The capacitance of the switch is also many times higher than that of the metal track.

The larger aspect ratio will reduce the series resistance. However, the parasitic capacitance is approximately proportional to the product of width and length. Therefore choosing an optimum aspect ratio and a sensible point in signal paths for switch insertion will ensure the minimal impact on performance of the filter.

III. FAULT MODELLING

In order to quantify the fault coverage of the proposed method, an accurate and realistic list of catastrophic and

parametric faults is required. To verify the fault coverage of the proposed test method, we have to define faults. A fault can be either hard (catastrophic) or soft (parametric). The hard faults cause the total failure of the circuit. Hard faults are easy to detect but difficult to locate and correct. Soft faults are caused by deviation in the process parameters and manufacturing process. The parameter deviation faults are more difficult to detect since the circuit can behave in an acceptable manner.

In this paper, we have considered two types of catastrophic fault; the stuck-short fault and stuck-open fault. Several research results show that 90% of the observed hard faults consist of shorts and opens in transistors, diodes, and capacitors. All catastrophic faults are considered to be in transistors, capacitors and interconnections and the list of the fault types is given in Table 1. Each fault type is modelled for PSPICE simulation using either a low impedance (10Ω) or high impedance (100MΩ).

Table 1: Catastrophic Fault Model

Fault	Cap	Trans	Int-con
Stuck-open Fault	C1-2	G,S,D	M1-4,M5-8, M9-10
Stuck-short Fault	C1-2	G,S,D	M1-4,M5-8, M9-10

C1-2=Capacitor terminals, G=Gate, D= Drain S=Source,

Parametric faults are also included in this paper. These faults are inherently more difficult to detect since the FUT can still function. The comprehensive list of parametric faults in Table2 is modelled and simulated in PSPICE for both types of biquad. Faults are determined using comparison between faulty and fault-free oscillation frequencies because various faults within the filter could give rise to the effect observed at the output.

Table2: Parameter Deviation Fault Model

Capacitance	C1 and C2
Transconductance	gm1and gm2
Output Mirrors	Aspect ratio
Channel Widths	W
Channel Lengths	L

IV. Simulation Results

The oscillation-based test method was applied to the two integrator loop and Tow-Thomas filters. The complete CMOS OTA–C filters in Fig.1 and Fig.2 using the OTA circuit of Fig.3 were simulated using 0.25μm CMOS technology and PSPICE level 7 models for verification of the proposed OBT structure. Results confirmed that the self-start stable oscillation of the filters is achieved by the circuit modifications described in section 2.

The filters were designed to have a cut-off frequency of 36MHz with a unity quality factor Q. An equal transconductance design was adopted with g_m =850μs and circuit capacitances C_1 = 5.88pf and C_2 = 2.44pf. The AC responses of the FUT for both modes of operation with the details of their frequencies with and without MOS switches are given in Table 3:

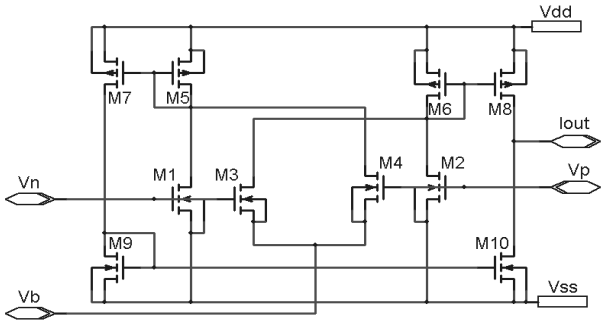

Fig.3. Schematic diagram of a simple OTA

Table 3: Frequency response of Filters

Mode	Connection	TIL Filter	TT Filter
		MHz	MHz
Filter	Without SW	36	34.7
	With SW	35	36
Osc_Test	Without SW	34.6	34.6
	With SW	34	34.8

We choose values of CMOS switch resistance such that they have negligible effects on the pole frequency and the new zeros introduced by the switch are outside the filter bandwidth. The analysis of the data given in Table 3, shows negligible pole frequency movement and insignificant total harmonic distortion introduced due to the nonlinearity of MOS resistance. The simulation results demonstrate that the circuit with MOS switches has similar performance to the original filter. Furthermore, the frequency of oscillation in the test mode with built-in MOS switch shown in Fig.4 is very close to the cut-off frequency of the filter, which provides the basis for the implementation of a consistent OBT in practice.

To quantify the fault coverage and the efficiency of the OBT strategy a number of different faults were inserted into the two filter circuits and their frequency deviations measured. Inserted faults were chosen using the fault-modelling methodology discussed in the previous section. The comprehensive fault-modelling list and fault detection results for the two integrator loop filter (FUT1) and Tow Thomas filter (FUT2) are given in Tables 4 and 5 respectively.
The fault-free oscillation frequency was 34MHz and 34.8MHz for FUT1 and FUT2 respectively. To determine the undetectable tolerance band, a Monte Carlo analysis, considering 5% tolerance for all components was performed.

The Monte Carlo analysis shows that the oscillating signal has lower and upper frequency deviation of -2.35% and 4.12% respectively for FUT1 and -2.30% and 6.22% respectively for FUT2. The faults which produced oscillation frequency deviation outside this tolerance band are considered to be

detectable. Tables 4 and 5 present the effects of the injected catastrophic and parametric faults on the oscillation frequencies and computed deviation from the fault-free frequency.

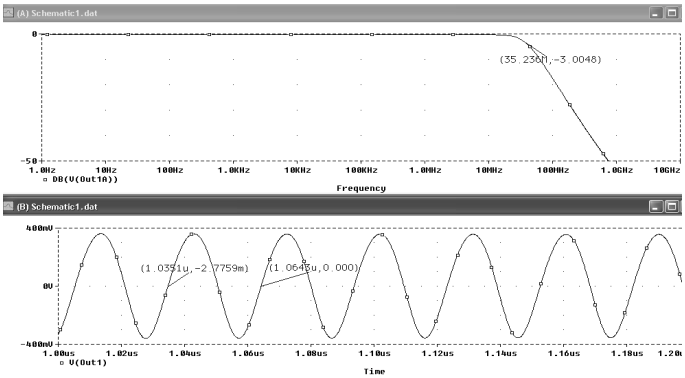

Fig.4. (A) Cut-off frequency of the filter under test and (B) Frequency of oscillation

Table 4: Injected faults in the Two-Integrator Loop Filter

Dev	C1or C2	C1and C2	Input gm
50%	-17.64%	-31.38%	31.38%
40%	-14.70%	-26.47%	25.5%
30%	-10.79%	-20.59%	19.61%
20%	-6.88%	-14.71%	12.74%
10%	-2.94%	-6.88%	5.88%
-10%	2.94%	5.88%	-6.86%
-20%	5.88%	14.71%	-16.68%
-30%	10.76%	25.47%	-26.47%
-40%	16.64%	39.21%	-37.27%
-50%	24.5%	57.82%	-47.06%
SOF	295%	472%	12%[1],8%[2]
SSF	NO	NO	NO

Table 5: Injected faults in the Tow-Thomas Filter

Dev	C_1 or C_2	C_1 and C_2	Input g_m
50%	-16.67%	-30.45%	31.61%
40%	-13.79%	-25.86%	26.44%
30%	-10.91%	-20.69%	20.12%
20%	-7.47%	-14.36%	13.79%
10%	-3.45%	-7.47%	6.89%
-10%	3.45%	8%	-7.47%
-20%	8.62%	18.96%	-16.7%
-30%	14.37%	32.7%	-25.9%
-40%	21.38%	49.4%	-35.6%
-50%	30.45%	60%	45.4%
SOF	285%	623%	8.8%
SSF	NO	NO	NO

Frequency deviation from its fault free frequency in Table 3, 1: SOF in input transistor M_3 2: SOF in input transistor M_4

The sensitivity of frequency deviation with respect to the injected faults depends upon the relationship between the components and the oscillation frequency, given by equation (7). All the catastrophic faults and most of the parametric faults are detectable except a small number of parametric faults in the output mirror transistors.

These faults can not be detected because they exhibit frequency deviation below the tolerance limits. From equation (7) it is obvious that these faults do not affect the frequency of oscillation, as g_m values are only determined by the input differential stage. Overall fault coverage of more than 87% has been obtained for both filters. The overall fault coverage is 87% due to the less fault coverage in TT filter because the faults in the third OTA (g_{m3}) are not detectable.

V. CONCLUSIONS

In this paper, we have proposed a vectorless, dynamic DFT method for OTA-C filters, based on converting the FUT into an oscillator using only MOS switches. The OBT technique has only measurement of the frequency deviation to detect faults, hence requires very small test time and good immunity to noise. The design is easily implemented with little area overhead and has negligible impact on the filter performance. Other advantages include a very simple test procedure, elimination of time consuming specification testing and requirement of only minor circuit modifications. The effectiveness of the proposed OBT strategy has been demonstrated through extensive simulations for two basic types of OTA-C biquad. Fault simulation results have shown that the proposed oscillation-based test technique provides high fault coverage around 87% and is capable of simultaneously detecting single and multiple faults. The OBT technique is very suitable for BIST filter synthesis and can be easily implemented in CAD tools for filter design. Finally, the OBT technique may be readily applied to higher order OTA-C filters and other analogue circuits. All these characteristics make the proposed OBT method very attractive for final production testing as well as wafer-probe testing.

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