A CMOS 750MHz Fifth-Order Continuous-Time Linear Phase Lowpass Filter with Gain Boost

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Abstract—The design and implementation of a CMOS continuous-time multiple loop feedback (MLF) leap frog (LF) filter is described. The filter is implemented using a fully-differential linear, low voltage operational transconductance amplifier (OTA). PSpice simulations using a standard TSMC 0.18μm CMOS process with 1.8V power supply have shown that the cut-off frequency of the filter ranges from 455MHz to 780MHz and dynamic range is about 58dB. The group delay is less than 5% over the whole tuning range; the maximum power consumption of the filter with gain boost is only 240mW.

I. INTRODUCTION

Linear phase lowpass filters have been widely used for hard disk drive (HDD) read channels to equalize the input signals. Among different filter structures, the cascade structure has attracted the most attention [1, 2]. However, the cascade structure has higher sensitivity, compared with multiple loop feedback (MLF) structures. Therefore, research has been conducted on HDD read channels by using MLF structures recently [3-6]. The inverse-follow-the-leader-feedback (IFLF), follow-the-leader-feedback (FLF) and leap frog (LF) structures all have been used for equalizers design. However, none of them can exceed the cut-off frequency of 500MHz. The HDD systems are high performance systems and near real-time applications [7], which continue to develop at a rapid and deterministic pace to meet the emerging demands of high performance computing and peripheral devices. Moreover, the industry is seeking for the solutions for next generation HDD systems, whose data rates can be up to 2Gb/s. We need a filter whose cut-off frequency is at least 700MHz; however, it is a challenge to design a filter at such ultra high frequency using pure CMOS. On the other hand, power consumption needs to be even lower, because more and more digital systems are expected to be integrated on the single chip due to using advanced deep submicron process. The easiest way to reduce the power consumption is reducing the power supply voltage. However, most specifications of a filter rely on the supply voltage strongly. Alternatively, we need to reduce the filter order to fulfill the overall power consumption requirement.

In this paper, our design is targeted at a MLF LF linear phase filter for HDD read channels, which can work at cut-off frequency of 750MHz with accurate linear phase, gain boost, and low power consumption.

The design of a fully-balanced OTA is discussed in Section II. Filter architecture and synthesis are described in Section III. The simulation results are given in Section IV, and finally conclusions are given in Section V.

II. FULLY-BALANCED OPERATIONAL TRANSCONDUCTANCE AMPLIFIER

Source degeneration OTAs have received more attention than any other techniques based OTA due to the tradeoff between linearity and power consumption. However, it has to pay the expense of the reduced overall transconductance. Moreover, the tuning range of the source degeneration OTA relies strongly on the triode region transistors, and thus it is relatively small [1, 5]. An alternative OTA is presented in this section to optimize the linearity and power consumption, which is shown in Figure 1.

DC Response of the OTA

The CMOS OTA in Figure 1 is used for the filter design.

Figure 1 Fully-balanced OTA
In this unit OTA cell, $M_1$ and $M_2$ are the input transistors. $M_3$–$M_6$ act as active biasing circuitry in such a way that the total current drawn by $M_3$–$M_6$ is required for larger signals. The active biasing shares the same bias current source with the differential pair $M_1$ and $M_2$. When the signal amplitude is small, $M_3$ and $M_4$ are in saturation while $M_5$ and $M_6$ are in the triode region. The $M_3$–$M_6$ branches remove some of the bias current. When the signal amplitude is positive and large, $M_6$ will become saturated and $M_5$ will be cut off. A smaller proportion of the total bias current will be drawn by $M_3$–$M_6$. When the signal amplitude is large, all the transistors will be in the triode region.

The OTA meeting the specification of linearity. Therefore, harmonic distortion (HD3). We may have a complete HD3 cancellation as long as the following condition is met,

$$V_{cm} + V_T = V_{cm}', K_{3,4} = X times K_{5,6} then I_D^3 can be expressed as,

$$I_{D3} = I_{D5} = X \cdot K_3 \left(\frac{V_{in}}{2} - V_{ds5} - V_T\right)$$

$$= 2K_5 \left(\frac{V_{in}}{2} + V_{cm} + V_T\right) \cdot \frac{1}{2} \left(V_{ds5}^2 - \frac{1}{2} V_{ds5}^2\right)$$

Let $V_{cm} + V_T = V_{cm}'$, $K_{3,4}$ is $X$ times $K_{5,6}$ then $I_{D3}$ can be expressed as:

$$I_{D3} = K_3 \left(\frac{V_{in}}{2} - V_{ds5} + V_{cm}'\right)^2$$

$$= \frac{K_3}{4(X+1)^2} \left[2V_{in}^2 - \left(1 - 3X\right)V_{in}^2 + 4(X+1)V_{in}V_{cm}' + 4(X+1)V_{cm}'^2 \right]$$

$I_{D4}$ has a similar expression, with $V_{in}$ replaced by $-V_{in}$. Therefore, the output current is then given by

$$I_{out} = I_{D3} \approx K_{1,2} \left(\frac{2}{2} \left(5 - 3X - 4\sqrt{X+1}\right)V_{in}^2 \right)$$

Using Taylor series, then equation (3) can be expanded as follows,

$$I_{out} = K_{1,2} \left(\frac{2}{2} \left(5 - 3X - 4\sqrt{X+1}\right)V_{in}^2 \right) \approx \frac{K_{1,2} \cdot K_{3,4} (3X + 4\sqrt{X+1} - 5)}{2K_{1,2} + (X+1)K_{3,4}} V_{in}$$

Note that the even order harmonic distortions are ideally zero due to the symmetry of fully differential OTA. The total harmonic distortion (THD) is mainly determined by the third harmonic distortion (HD3). We may have a complete HD3 cancellation as long as the following condition is met,

$$K_{1,2} = \frac{K_{1,2} \cdot K_{3,4} (3X + 4\sqrt{X+1} - 5)}{2K_{1,2} + (X+1)K_{3,4}}$$

The above equation gives us an insight into how to design the OTA meeting the specification of linearity. Therefore, the transconductance of OTA can be expressed as,

$$g_m = \frac{K_{1,2}^2 I_B}{2K_{1,2} + (X+1)K_{3,4}}$$

Second-order Effects of the OTA

Second-order effects, such as mobility reduction, body effect causing deviations from the ideal square-law behavior of MOS devices have been neglected in the above analysis. However, high frequency filters require the use of high electric fields, thus the mobility reduction effects must also be taken into account. As a first order approximation, mobility reduction in MOS transistors may be modeled as,

$$\mu = \frac{\mu_0}{1 + \theta(V_{gs} - V_T)}$$

Where $\mu_0$ is the zero-field mobility of carriers, $\theta$ equals to $1/(T_{ox}E_{CR})$ is the coefficient of the effect of the electric field on the mobility, $T_{ox}$ is the gate oxide thickness and $E_{CR}$ is the critical field. On the other hand, the dependence on the bulk-source voltage resulting in body effect is another potential cause of nonlinear behavior in the voltage-to-current conversion of the OTA in Figure 1. If the transistors are not connected to $V_{DD}$ or ground, the bulk-source voltages $V_{BS}$ are not equal to zero and the threshold voltage can be expressed as,

$$V_T = V_{T0} + \gamma(\sqrt{\phi} - V_{BS} - \sqrt{\phi})$$

Where $V_{T0}$ is the threshold voltages for $V_{BS}$ equal to zero, $\gamma$ is the bulk threshold parameter, and $\phi$ is the strong-inversion surface potential. Including equation (7) and equation (8), equation (6) can be approximated by equation (9),

$$g_m = \frac{K_{1,2}^2 I_B}{4(X+1)^2 V_{in}^2 \left[1 + \theta(V_{gs} - V_{T0}) + \theta(V_{gs} - V_{T0})^2\right]}$$

Thus, the mobility reduction limits the transconductance of the OTA.

Frequency Response of the OTA

Owing to the absence of internal nodes, the OTA in Figure 1 has excellent high-frequency performance. Figure 2 shows the small-signal model of the equivalent half-circuit of the OTA in Figure 1 with capacitive loads for frequency analysis. Using this model, the voltage transfer function of the OTA-C integrator can be shown as

$$A_c(s) = \frac{V_{out}(s)}{V_{in}(s)} = \frac{g_m}{s(C_L + C_p) + G_{out}}$$

Where $C_L$ and $C_p$ are the load capacitance and parasitic output capacitance of the OTA, respectively, and $G_{out}$ is the OTA’s output conductance. The two parameters: $C_p$ and $G_{out}$ of the model are given by

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\[ C_p = C_{DS1} + C_{DS11} + C_{GD1} + C_{GD11} \]  
\[ G_{out} = g_{ol} + g_{ol1} \]  
(11)

Where \( g_{ol} \) is the output conductance of the MOS transistors of the OTA.

\[ H_d(s) = \frac{(s^2 - 1)}{D(s)} \]  
(16)

With
\[ D(s) = 0.201926s^5 + 0.822285s^4 + 2.075924s^3 + 3.033116s^2 + 2.604527s + 1 \]

The fully balanced realization of the function in equation (16) using the current-mode LF structure with output summation OTAs is shown in Figure 3.

\[ f_d = \frac{G_{out}}{2\pi(C_L + C_p)} \]  
(13)

Where \( f_d \) is the dominant pole frequency of the OTA. Thus, the open-loop gain-bandwidth product of the OTA is the multiplication of equations (12) and (13)

\[ GBW = \frac{g_m}{2\pi(C_L + C_p)} \]  
(14)

Note that BW can be written as a function of GBW as

\[ BW = \frac{GBW}{A_{ol}} \]  
(15)

It is crucial to note that there is a tradeoff between BW and \( A_{ol} \) as can be seen from equation (15). In other words, high bandwidth can be obtained at the expense of reduced DC gain and vice versa.

### III. Filter Architecture and Synthesis

The normalized characteristic of a fifth-order lowpass 0.05° equiripple linear phase filter with real zeros at the cutoff frequency is given by:
capacitance must also be taken into account. For the circuit of Figure 1, the parasitic capacitance is about 0.2pF. The capacitance values are recalculated below:

\[ C_1 = 1.0748 \text{pF}, \quad C_2 = 2.7038 \text{pF}, \quad C_3 = 3.697 \text{pF}, \quad C_4 = 4.5549 \text{pF}, \quad C_5 = 6.6276 \text{pF}. \]

### IV. SIMULATION RESULTS

The circuit was designed and simulated using BSIM 3v3 Spice models for a TSMC 0.18μm CMOS process available from MOSIS [10]. Figure 4 shows the magnitude response of the filter with and without gain boost. As can be seen from Figure 4, the gain boost of the filter is about 5dB. By varying the bias voltage of the unit OTA cell, the tuning range of cut-off frequency without gain boost is 455−780MHz. The maximum total power consumption of the filter is about 240mW at 780MHz cut-off frequency for a single 1.8V power supply.

![Figure 4 Simulated magnitude response of the filter with and without gain boost](image)

The dynamic range is about 58dB at \( f_c = 750 \text{MHz} \). The performance of the filter offers significant improvements; especially the power consumption is much smaller than other designs, making the presented filter well suitable for portable electronics products. To compare the proposed solution with previous publications, the Figure of Merit (FOM) is defined; all of the parameters such as bandwidth in MHz, geometry in μm, gain boost (GB) coefficient 1.5, and power consumption per pole in mW are taken into account.

\[
FOM = \frac{GB \cdot [\text{Bandwidth}]^2 \cdot \text{Geometry}}{\text{Power}} \quad \text{[19]}
\]

The proposed filter has 3164 of FOM, which is much higher than any other MLF structures based filters in the literature.

### V. CONCLUSIONS

This paper has described a 750MHz current-mode fully-balanced fifth-order linear phase low-pass filter based on the MLF LF structure, applied to a HDD read channel. A linear single stage OTA with a typically large transconductance has been used. Simulation results using 1.8V 0.18μm CMOS show that group delay ripple is around 4% with and without gain boost; the power consumption of the proposed filter is about 240mW with gain boost at \( f_c = 750 \text{MHz} \). The frequency tuning range is from 455MHz to 780MHz. These results have shown that the MLF LF filter can achieve good performance and may become one of the filtering solutions for next generation HDD systems.

### VI. REFERENCES


