Guest Editorial: Memristive electronic circuits, neural networks and neuromorphic computing

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Introduction: The theoretical concept of memristor was first proposed as the fourth basic circuit element by Chua in 1971. It defines the relationship between electric charge and magnetic flux. The first physical implementation of memristor was realised by HP Labs in 2008. It was fabricated in advanced nano technology. Intensive research has since been conducted on the development of memristors across the whole world and wide applications of memristors have also been explored. Since they are smaller nano device, consume less power, and have both memory and processing functions, memristors have been widely recognised to be the future of electronics, computing and AI. For example, they will play a key role in emerging edge computing and brain-like computing.

The aim of the Special Issue is to follow the state of the arts of memristor-based circuits and systems, with particular focus on memristive electronic circuits, neural networks and neuromorphic computing, publish original technical papers reflecting the most recent research and application results, and identify new challenges and ways forward for future research and applications in this emerging fast-growing field.

Papers in the special issue: A good number of submissions have been received. After rigorous review, six papers have been selected for publication in the Special Issue. These papers cover a wide range of topics in memristive electronic circuits, neural networks and neuromorphic computing.

The paper entitled Drift of Invariant Manifolds and Transient Chaos in Memristor Chua's Circuit by Di Marco et al. studies non-linear dynamics of Chua's circuit with a memristor. Transient chaos phenomena are observed in a generalized memristor Chua's circuit where a non-linear resistor is connected in parallel with the memristor to better model a real memristor behaviour. Through the flux-charge analysis method the authors find that the origin of transient chaos is due to the drift of the index of the memristor circuit invariant manifolds caused by the charge flowing into the non-linear resistor.

The paper Design of Chaotic Circuit based on Knowm Memristor by Wang et al. presents the model and the corresponding parameter identification of the Knowm memristor and designs a non-linear chaotic circuit based on the Knowm memristor. The authors analyse equilibrium points and stability of the Knowm memristor chaotic circuit and present nonlinear dynamic behaviour by using the bifurcation diagram and Lyapunov exponents. The designed Knowm memristor chaotic circuit is implemented and tested with the experimental results confirming the theoretical predictions.

In the paper entitled Dynamic Symmetrization in a Memristive HR Neuron, Huang et al. introduce a memristor as a synapse in the HR neuron to form a memristive HR neuron. The constructed memristive HR neuron with the aid of the absolute value and signum function exhibits attractor doubling and complex coexisting symmetrical firing patterns. The process of attractor doubling or symmetric firing can effectively simulate the discharge phenomena of neuronal polarization and hyperpolarization, providing a useful approach for future research into the diversity of the brain.

In the paper entitled Initial State-Dependent Implementation of Logic Gates with Memristive Neurons, Rajki et al. introduce a novel and simple Memristor Cellular Neural Network (M-CNN), consisting of a suitable connection between just two analogue electronics cells, which, exploiting the rich and unique non-linear dynamics of a pair of non-volatile memristors, described through the highly-reliable and predictive physics-based TaOx model from Strachan et al., is capable to carry out the AND, OR, and XOR Boolean logic operations between two binary inputs. The work provides evidence for the add-on functionalities, which memristors endow traditional cellular neural networks (CNNs) with. In fact, while a standard CNN should be re-programmed for each computing task, it were supposed to fulfil, the proposed M-CNN may switch operating mode depending solely upon the resistance states preliminarily written into the respective memristors. Machine learning algorithms are employed to optimize the circuit parameters of the proposed M-CNN so as to turn it into an adaptable logic gate, in which the initial conditions for its memristors determine which Boolean operation from a triplet of options it eventually executes. Taking into account that memristors may also be used to store the intermediate or final results of a computation, besides contributing significantly to the data processing operations, as demonstrated in this work, where they allow multi-tasking in an otherwise single-purpose two-cell array, their use in novel CNN designs promises to pave the way toward the realization of in-memory-computing platforms, which, co-integrated with matrices of sensor elements, form light-weight, low-power and high-spatial resolution visual microprocessors for Edge Computing applications.

In the paper 256-Level Honey Memristor Based In-Memory Neuromorphic System by Uppaluru et al., a 256-level honey memristor-based neuromorphic system is proposed and experimentally evaluated for image recognition. The honey memristor-based system is built, and its non-linearity and variation are investigated. Experimental results indicate that the inference accuracy of the system is greater than 88% and 87% without and with cycle-to-cycle variation respectively for different optimization algorithms. The energy and latency performances of optimization algorithms with and without variation are also compared, with the momentum algorithm consistently outperforming the other algorithms.

In the paper Nanoscale Ni/Mo/MoO3/Ni Memristor for Synaptic Applications, Praveen et al. propose a physics-based modelling of a nanoscale Ni/Mo/MoO3/Ni memristor. The proposed memristor has stable hysteresis *I–V* characteristics as well as a significant reduction in forming voltage to 0.75 V. The simulated resistive switching responses show a consistently low coefficient of variability with 14.31% and 14.85% for SET and RESET, respectively during cycle-to-cycle variations along with a low compliance current of 193 μA. In addition to observing synaptic plasticity, how ramprates impact 'Potentiation' and 'Depression' is also examined as memristor conductance closely relates to synaptic weights.

Conclusion: As one of the most important enabling technologies, memristive electronic circuits, neural networks and neuromorphic computing will play a crucial role in the development of future electronics, computing and AI and receive continued focus of research from world-wide academia and industry. We hope that this special issue will stimulate further interest and be useful for those readers who may want to pursue further research in this exciting and fasting growing area.

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Yichuang Sun received the B.Sc. and M.Sc. degrees from Dalian Maritime University, Dalian, China, in 1982 and 1985, respectively, and the Ph.D. degree from the University of York, York, U.K., in 1996, all in communications and electronics engineering. Dr. Sun is currently a Professor of Communications and Electronics and the Head of Electrical and Electronic Engineering in the School of Physics, Engineering and Computer Science of the University of Hertfordshire, UK. He has published some 450 papers and contributed 10 chapters in edited books. He has also published four text and research books: Continuous-time Active Filter Design (CRC Press, USA, 1999), Design of High-frequency Integrated Analogue Filters (IEE Press, UK, 2002), Wireless Communication Circuits and Systems (IET Press, 2004), and Test and Diagnosis of Analogue, Mixed-Signal and RF Integrated Circuits - The Systems on Chip Approach (IET Press, 2008). His research interests are in the areas of wireless and mobile communications, microelectronic circuits and systems, machine learning and neuromorphic computing. Professor Sun was a series editor of IEE Circuits, Devices and Systems Book Series (2003–2008). He was Associate Editor of IEEE Transactions on Circuits and Systems I: Regular Papers (2010–2011, 2016–2017, 2018–2019). He has also been editor for several other journals, including ETRI Journal, Journal of Sensor and Actuator Networks, Frontiers in Communications and Networks, etc. He was sole or lead Guest Editor of 10 IEEE, IEE/IET and other journal special issues/topics: High-frequency Integrated Analogue Filters in IEE Proc. Circuits, Devices and Systems (2000), RF Circuits and Systems for Wireless Communications in IEE Proc. Circuits, Devices and Systems (2002), Analogue and Mixed-Signal Test for Systems on Chip in IEE Proc. Circuits, Devices and Systems (2004), MIMO Wireless and Mobile Communications in IEE Proc. Communications (2006), Advanced Signal Processing for Wireless and Mobile Communications in IET Signal Processing (2009), Cooperative Wireless and Mobile Communications in IET Communications (2013), Software-Defined Radio Transceivers and Circuits for 5G Wireless Communications in IEEE Transactions on Circuits and Systems-II (2016), Cognitive and AI-enabled Wireless and Mobile Communications in IET Communications (2020), Machine Learning in Communication Systems and Networks in MDPI journals of Applied Sciences, Sensors, Electronics, Photonics, JSAN, and Telecom (2022-24), and Memristive Electronic Circuits, Neural Networks and Neuromorphic Computing in IET Electronics Letters (2023-24). He has also been widely involved in various IEEE Communications and Circuits and System Society technical committee and international conference activities. Professor Sun has been among the World's Top 2% Scientists named by Stanford University in both single year and career lists every year since beginning.

Shahar Kvatinsky is a full professor at the Andrew and Erna Viterbi Faculty of Electrical and Computer Engineering, Technion—Israel Institute of Technology and a visiting professor at the Edward S. Rogers Sr. Department of Electrical & Computer Engineering, University of Toronto. Shahar received the B.Sc. degree in Computer Engineering and Applied Physics and an MBA degree in 2009 and 2010, respectively, both from the Hebrew University of Jerusalem, and the Ph.D. degree in Electrical Engineering from the Technion—Israel Institute of Technology in 2014. From 2006 to 2009, he worked as a circuit designer at Intel. From 2014 to 2015, he was a post-doctoral research fellow at Stanford University. Kvatinsky is a member of the Israel Young Academy. He is the head of the Architecture and Circuits Research Center at the Technion, chair of the IEEE Circuits and Systems in Israel, and an editor of Microelectronics Journal and Array. Kvatinsky has been the recipient of numerous awards: the 2023 Uzi & Michal Halevy Award for Innovative Applied Engineering, the 2021 Norman Seiden Prize for Academic Excellence, the 2020 MDPI Electronics Young Investigator Award, the 2019 Wolf Foundation's Krill Prize for Excellence in Scientific Research, the 2015 IEEE Guillemin-Cauer Best Paper Award, the 2015 Best Paper of Computer Architecture Letters, Viterbi Fellowship, Jacobs Fellowship, an ERC starting grant, the 2017 Pazy Memorial Award, 2014, 2017 and 2021 Hershel Rich Technion Innovation Awards, the 2013 Sanford Kaplan Prize for Creative Management in High Tech, 2010 Benin prize, and seven Technion excellence teaching awards. His current research is focused on circuits and architectures with emerging memory technologies and the design of energy-efficient architectures.

Georgios Ch. Sirakoulis received the M.Eng. and the Ph.D. degrees in electrical and computer engineering from the Department of Electrical and Computer Engineering, Democritus University of Thrace, Thrace, Greece, in 1996 and 2001, respectively. Since 2018, he has been a professor with the Department of Electrical and Computer Engineering, where he is also serving as head of department from 2020. He has also been a visiting researcher/professor with UWE, U.K., since 2014. Prior to his academic appointment, he was with private sector as a co-founder and research associate of Ulysses Ltd. (1999–2002). He is the author or co-author of more than 160 peer reviewed articles in prestigious international scientific journals and more than 190 peer-reviewed articles in proceedings of international scientific conferences. He has coauthored and co-edited thirteen scientific books (twelve international and one national book) and is the author of 36 chapters in international scientific books. He is an associate editor for well-known magazines in the field of circuits and systems, such as the IEEE Transactions on Nanotechnology (senior editor), IEEE Nanotechnology Magazine, IEEE Trans. On Agrifood Electronics, and in the past IEEE TCAS II, and the IEEE Transactions on Computer, as well as other publishing houses (including Springer Nature, Elsevier, World Scientific, Taylor & Francis, Old House Publishing) and an elected Member of many international and national scientific associations. He has supervised and is supervising 18 doctoral dissertations, 34 postgraduate master theses, and 105 diploma theses, while some of the above dissertations and theses have been awarded by the department, as well as by domestic and international bodies. He was a Coordinator, Principal Investigator, or Scientific Officer/Researcher for more than 35 research projects funded by GSRT, European Union, HFRI, and also by institutions and private companies in Greece and abroad, in research topics related to nanoelectronics, future and emergent electronic-nanoelectronic devices, circuits and architecture, novel computational architecture, applications of complex and intelligent electronic systems in robotics, energy, building evacuation, etc. He has organized many international conferences and workshops, such as IEEE CAFÉ 2024, CNNA 2023, NANOARCH 2019, NANOARCH 2018, PACET 2017, etc. and has delivered invited talks at more than 45 international conferences, workshops, and universities abroad over the last five years. His research interests include future and emergent electronic devices, circuits, models, and architectures including memristors and quantum cellular automata, beyond CMOS computing devices and circuits and non von Neumann computing architectures, unconventional and bioinspired computation/biocomputation, and cellular automata. He is the Vice Chair of the IEEE Task Force on

Unconventional Computing, Chair of the IEEE CAS Nano-Giga TC, and Secretary of IEEE CAS CNNAC TC as well VP for Publications for IEEE NTC and IEEE Greece Section Treasurer.

Jingru Sun received the B.Sc. degree in Computer Science and Technology from the Department of Computer Science of Changchun University, China, in 2000, the M.Sc. degree in Computer Software and Theory from the Department of Computer Science of Northeastern University, China, in 2004, and the Ph.D. degree in Computer Science and Technology from the College of Computer Science and Electronic Engineering, Hunan University, China, in 2014. Since 2004 she has been with the College of Computer Science and Electronic Engineering, Hunan University, China and is currently an associate professor and a Ph.D. supervisor. From March 2016 to March 2017, she was a visiting scholar in the School of Engineering and Technology at the University of Hertfordshire in the UK. Her research interests include memristive neural networks, brain-like computing, image encryption, and intelligent transportation systems. She has led a team of some ten researchers conducting active research in these areas. Her research projects have been funded by various funding bodies in China including the project on memristor crossbar array based high efficiency in-memory computing logic circuits funded by the National Science Foundation of China. She has published more than 30 papers (two papers are highly cited) in conferences such as IEEE International Symposium on Circuits and Systems and journals including the prestigious IEEE Transactions on Circuits and Systems–I: Regular Papers, IEEE Transactions on Industrial Informatics, IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, IEEE Transactions on Consumer Electronics, and IEEE Internet of Things Journal. She is a member of the IEEE, the Chinese Computer Society, the Chinese Electronics Society, an executive director of the Hunan Electronics Society in China, and the secretary of the Chaos and Nonlinear Circuit Special Committee of the Chinese Electronics Society.

Alon Ascoli (Senior Member, IEEE) received the Italian Habilitation as full professor in Electrical Circuit Theory from the Italian Ministry of Education in 2023, the German Habilitation as full professor in Nonlinear Circuit Theory from Technische Universität Dresden, Dresden, Germany, in 2022, the Italian Habilitation as Associate Professor in Electrical Circuit Theory from the Italian Ministry of Education in 2017, a Ph.D. degree in Electronic Engineering from University College Dublin, Dublin, Ireland, in 2006, and a Master of Science Degree (First Class Honours) in Electronic Engineering from Universita' degli Studi Roma Tre, Rome, Italy, in 2001. He was a Visiting Research Scholar at the University of California Santa Cruz, Santa Cruz, California, USA, in 2019. Since December 2023 he is an Associate Professor at the Department of Electronics and Telecommunications of Politecnico di Torino, Turin, Italy. He was affiliated with Technische Universität Dresden from December 2012 to November 2023, where he held a lifelong position since 2018. He develops theoretical concepts enabling to harness disruptive nanotechnologies to overcome traditional circuits' limitations for applications of interest to the more-than-Moore electronics era as well as to improve our understanding of the complex behaviours of biological systems, including the mechanisms underlying emergent phenomena in neuronal cells. In 2007, Prof. Ascoli was honoured with the International Journal of Circuit Theory and Applications (IJCTA) Best Paper Award for the manuscript "Modelling the dynamics of log-domain circuits." In September 2020 (June 2022), he was conferred the Best Paper Award on Electronics at the International Conference on Modern Circuits and Systems Technologies (MOCAST) for the manuscript "Image mem-processing bio-inspired cellular arrays with bistable and analogue dynamic memristors" ("SPICE compact model for an analog switching niobium oxide memristor"). In 2023, he was awarded the Darlington Best Paper Award from IEEE Transactions on Circuits and Systems for the manuscript "How to Build a Memristive Integrate-and-Fire Model for Spiking Neuronal Signal Generation". He was the Chair of the 7th Memristor and Memristive Symposium, held in Catania, Italy, in 2021. He was one of the Program Chairs at NANOARCH 2023. He has organized Special Sessions on Theory and Applications of Memristor Devices, Circuits, and Systems in IEEE ISCAS editions 2016, 2018, 2019, 2020, 2021, 2022, and 2023, in IEEE ICECS editions 2019, 2021, 2022, and 2023, in ECCTD editions 2017, and 2020, in MOCAST editions 2021, 2022, 2023, and 2024, in IEEE NANO edition 2022, and in IEEE MetroXRAINE editions 2023 and 2024. He has served as Co-Chair for the third IEEE Circuits and Systems Society (CASS) Seasonal On-Line School on "Intelligence in Chips: Memristive Sensing & Bioinspired Computing Systems" from October 16 to October 19, 2024. Over the time span November, 1–7, 2022, he served as a Co-Chair for the second IEEE Circuits and Systems Society (CASS) Seasonal On-Line School on "Intelligence in Chips: Integrated Sensors and Memristive Computing". He served as the President of the IEEE CAS Cellular Nanoscale Networks and Array Computing (CNNAC) TC from 2019 to 2021. He was the President of the IEEE Circuits and Systems Society (CASS) Cellular Nanoscale Networks and Memristor Array Computing (CNN-MAC) Technical Committee (TC) from 2021 to 2023. He has been a member of the Chua Memristor Center since 2016. Since October 2020, he has been a member of the IEEE CASS Nanoelectronics and Gigascale Systems Technical Committee (Nano-Giga TC). Since 2023 he is a member of the Italian Society for Chaos and Complexity, with which he was already affiliated from 2013 to 2016. He has been an associate editor for IEEE TCAS-I since March 2023. Since 2024, he is a member of the IEEE CASS Nonlinear Circuits and Systems (NCAS) TC.

APPENDIX:

Order of papers to appear in the special issue:

1. ELL-2023-07-0545: Drift of Invariant Manifolds and Transient Chaos in Memristor Chua's Circuit; Mauro Di Marco, Mauro Forti, Luca Pancioni, and Alberto Tesi
2. ELL-2024-05-0416: Design of Chaotic Circuit based on Knowm Memristor; Fuping Wang and Faqiang Wang
3. ELL-2024-03-0202: Dynamic Symmetrization in a Memristive HR Neuron; Keyu Huang, Chunbiao Li, Yongxin Li, Tengfei Lei and Haiyan Fu
4. ELL-2023-12-0845: Initial State-Dependent Implementation of Logic Gates with Memristive Neurons; Franciska Rajki, András Horváth, Alon Ascoli, and Ronald Tetzlaff
5. ELL-2024-05-0355: 256-level Honey Memristor Based In-Memory Neuromorphic System;.Harshvardhan Uppaluru, Zoe Templin, Mohammed Rafeeq Khan, Md Omar Faruque, Feng Zhao, and Jinhui Wang
6. ELL-2023-11-0806: Nanoscale Ni/Mo/MoO3/Ni Memristor for Synaptic Applications; Maryala Praveen, Atul Kumar Nishad and Vipul Kumar Nishad