Memristor-based brain emotional learning neural network with attention mechanism and its application

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Abstract—The brain emotional learning network offers several advantages when compared to traditional neural networks. It features a simpler structure, low computational complexity, and fast training speed. These characteristics make it ideal for applications like pattern recognition, data classification, and intelligent control. However, current brain emotional learning networks, including their modified networks, are not capable of recognizing or classifying data in complex environments. To address this issue, this paper proposes a brain emotional learning network with an attention mechanism that strengthens the processing of key information while suppressing interfering information, thereby enabling the network to recognize data within complex environments. Furthermore, software implementation of neural networks often experiences slow computing speeds due to the separation of storage and computation in traditional von Neumann computers. To combat this issue, the paper presents a hardware circuit implementation of the attention mechanism-based brain emotional learning network using memristors. Finally, the designed in-memory computing neural network has been successfully applied to the recognition of traffic signs within complex environments, and has achieved accurate and rapid recognition.

Index Terms—Article submission, IEEE, IEEEtran, journal, Lagerty and the submission of the submiss

I. INTRODUCTION

The design of advanced electronic systems, particularly those incorporating emerging devices such as memristors, is intrinsically dependent on computer-aided design methods [1]–[3]. The integration of computer-aided design techniques with hardware design has become essential for optimizing complex circuit and accelerating the development of memristive circuits. In recent years, with advancement of computer-aided design methods the memristor-based neural network circuit design has been anticipated to surmount the von Neumann bottleneck, garnering widespread attention [4]– [6]. The novel memristor-based architectures offer advantages

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C. Xu is with the School of Computer and Communication Engineering, Changsha University of Science and Technology, Changsha, 410082, China.

H. Lin is with the School of Electronic Information, Central South University, Changsha, 410083, China. such as in-memory computing [7]–[9], high integration density [10]–[12], inherent nonlinear characteristics [13]–[15]. Consequently, memristive neural networks exhibit significant potentials across diverse learning frameworks, including the transformer network [16], Bayesian inference network [17], bio-inspired neural network [18].

In the field of object recognition applications, the memristive neural network have emerged as a research focus. For instance, Zhang et al. constructed a memristive multilayer perceptron and employed the error back propagation (BP) algorithm for network training, achieving successful character recognition [19]. Yao et al. fabricated memristor crossbar arrays to implement convolutional neural networks (CNNs), enhancing parallel-computing efficiency and achieving rapid and highly accurate recognition of MNIST images [20]. Oin et al. developed a memristive binary neural network (BNN) and utilized the BP algorithm for training, achieving high recognition accuracy on the MNIST images [21]. Wen et al. designed a memristor-based sparse compact convolutional neural network capable of maintaining accuracy and reducing the hardware circuit scale during recognition tasks [22]. Zhang et al. constructed a memristor-based gated recurrent unit with full circuit functionality, applying it to the recognition and prediction of handwritten characters [23]. While diverse architectures of neural networks based on memristors have been proposed and applied to recognition tasks, it is noteworthy that most of these networks are trained using gradient descent algorithm for weight optimization. This training method carries the risk of gradient vanishing or explosion, and circuits designed based on gradient descent algorithms exhibit the disadvantage of complex structures.

Emotional learning constitutes a vital component of cognitive systems, and in recent years, the significance of emotional intelligence has been underscored in the era of AI. Research in emotional neuroscience has elucidated the limbic system theory of emotion as an anatomical model of emotional brain [24]. The limbic system is composed of the thalamus, the amygdala, the orbitofrontal cortex (OFC), the hippocampus, the hypothalamus and other associated structures. The brain emotional learning (BEL) model, proposed in [25], emulates the emotional learning mechanism between the OFC and the amygdala, which aims to address the issue of long training times associated with traditional neural networks, making them widely employed in classification [26], prediction [27], and intelligent control tasks [28]. Th implementation of emotional learning using memristor-based circuits has also attracted attention to overcome the limitations of traditional neural networks. Xu et al. introduced a memristive brain emotional learning circuit that incorporates contextual information. They applied this circuit to multi-task classification, achieving high accuracy and fast response speed [29]. Zhou et al. presented a unique memristive circuit that simulates the dual-loop emotional learning process in the human brain. They designed a radiation early warning monitoring system that utilizes this circuit to process radiation signals and generate emotional responses [30]. Zhang et al. proposed an operant conditioning model and memristive circuit implementation based on the neural and psychological mechanisms that influence human behavioral decision-making during interactions with dynamic environments [31]. Zhang et al. simulated the limbic system by a Pleasure-Arousal-Dominance emotion system and designed its memristive circuit applied in the multimodal input based facial emotion generation [32].

Despite the ongoing proposal and application of various emotional learning algorithms and their memristive circuit implementations, there remain unexplored areas. Notably, the attention mechanism, a crucial element in cognitive systems, has not received thorough investigation, particularly in the realm of emotional learning systems. Biologically, the attention mechanism operates at the onset of visual information input, exerting a significant influence on emotional learning [33], [34]. Computationally, introducing attention mechanism into neural networks can effectively enhance the computational efficiency [35]–[37]. Therefore, investigating attention mechanism-based emotional learning networks holds substantial value. In this paper, we propose a novel attention mechanism-based brain emotional learning (AttBEL) model, combining the attention mechanism's capacity to select relevant information and suppress interference with the fast convergence characteristics of brain emotional learning. Subsequently, we implement the hardware circuit of the proposed AttBEL model using memristors and discrete electronic components, enabling in-memory computing. This hardware implementation significantly enhances the network's running speed. Finally, we evaluate the designed memristive AttBEL circuit in the task of traffic sign recognition, achieving superior recognition speed compared to software-based approaches.

The main contributions of this work are summarized as follows.

- 1) A novel visual selective attention-based brain emotional learning model is proposed. Unlike previous research on brain emotional learning models [25]–[27], this work considers the visual attention mechanism.
- 2) An in-memory computing circuit implementation of the attention mechanism-based brain emotional learning model based on memristor is proposed. In contrast to previous memristive BEL circuits [29]–[31], our designed circuit incorporates the attention mechanism, endowing the circuit with enhanced functionality.
- 3) The memristor-based in-memory computing circuit is applied in the task of traffic sign recognition. The experimental results demonstrate that our memristive attention mechanism-based brain emotional learning circuit achieves

The rest of this article consists of the following. In Section II, the saliency-based attention mechanism is reviewed and the attention mechanism-based brain emotional learning model is proposed. Section III introduces the memristive circuit implementation of the visual selective attention model and the brain emotional learning model. Section IV performs the traffic sign recognition task on the memristive attention mechanism-based brain emotional learning circuit. Section V presents the conclusion and outlook of this work.

II. ATTENTION MECHANISM-BASED BRAIN EMOTIONAL LEARNING MODEL

A. Saliency-based visual attention mechanism

The saliency-based visual attention model, derived from Koch and Ullman's selective attention theory [41], is based on two fundamental assumptions. Firstly, human visual processing occurs hierarchically, where lower-level visual features (such as edges and textures) are processed before higherlevel features (such as object identification). Secondly, saliency maps are generated from visual features of a scene to guide attention. To construct saliency maps, a sequence of filters is applied to emphasize various visual features. These filters are designed to highlight specific characteristics, such as regions of high contrast or high orientation selectivity. By combining these filters, a set of saliency maps is obtained, with each map representing the likelihood of a particular location in the image attracting attention. The winner-take-all (WTA) mechanism is then employed to direct attention to the most salient location in the scene for further processing. This chosen location determines subsequent processing, as attention sequentially moves to other salient areas in a serialized manner.



Fig. 1. Architecture of Itti's saliency-based visual attention model.

A diagram describing the main processing stages of the model is shown in Fig.1. A set of topographic feature maps is extracted from the visual input. All feature maps are normalized and combined into a master saliency map, which topographically codes for local saliency over the entire visual scene. Different spatial locations then compete for largest saliency, based on how much they stand out from their surroundings. A WTA circuit selects this most salient location as the focus of attention. The WTA circuit is endowed with internal dynamics, which generate the shifts in attention based on a mechanism named inhibition of return.

B. Proposed attention mechanism-based brain emotional learning model

Although the neural network model based on brain emotional learning has the advantages of simple structure, low computational complexity and fast training speed, however, the existing BEL models has not taken the attention mechanism into consideration. To this end, we propose an attention mechanism-based brain emotional learning model, whose structure is shown in Fig.2. The mechanism of the proposed AttBEL model is as follows.



Fig. 2. Structure of the proposed attention mechanism-based brain emotional learning model.

(1) According to the theory of visual information processing in [33], the data $S=[S_1, S_2, \ldots, S_n]$ processed by visual features is transmitted to the selective attention module through the thalamus and sensory cortex modules. The selective attention module is composed of star-connected leaky-integrateand-fire neurons (LIFN), which realizes the aggregation and transfer of attention through competition and cooperation mechanisms.

Assuming the input to the selective attention model is $S=[S_1, S_2, \ldots, S_n]$, the *i*-th neuron output of the selective attention network can be calculated as

$$Att_i = \begin{cases} S_i & if \ S_i \in k\\ 0 & otherwise \end{cases}$$
(1)

where $Att=[Att_1, Att_2, ..., Att_n]$, and k is a set that contains the largest value and its surrounding neighbors of a.

(2) The selected data Att is used as the input of the amygdala module and the orbitofrontal module. The weight of the amygdala is v, the output of the amygdala is E_A , which can be obtained by

$$E_A = \sum_{i=1}^{n} Att_i \cdot v_i \tag{2}$$

For the OFC block, the output E_O is the sum of the multiplication of the input Att and the weights w, and it can be expressed as

$$E_O = \sum_{i=1}^{n} Att_i \cdot w_i \tag{3}$$

The output of the AttBEL is $E = E_A - E_O$.

(3) Use the errors between the reward signal Rew and the output of amygdala module E_A and orbitofrontal cortex module E_O to regulate the weights of these modules, respectively. The new weight values of amygdala model and OFC model are calculated by the following

$$\begin{cases} v_i(n+1) = v_i(n) + \alpha (Att_i \cdot (Rew - \sum_j E_{Aj})) \\ w_i(n+1) = w_i(n) + \beta (Att_i \cdot (\sum_j E_{Oj} - Rew)) \end{cases}$$
(4)

where v_i , w_i are the weight values of amygdala model and OFC model, respectively, and α , β , and Rew are learning rates for amygdala model and OFC model, and reword signal, respectively.

The design of electronic systems, especially the circuit design of advanced electronic components such as memristors, is essential through computational design assistance. The process of combining the attention mechanism with emotional learning can be described in Algorithm 1. The algorithm describes the first stage in computer-aided circuit design which can be used to verify the correctness of the design system.

| Algorithm | 1 | Attention | mechanism-based | brain | emotional |
|-------------|----|-----------|-----------------|-------|-----------|
| learning mo | de | 1 | | | |

Input: data $S=[S_1, S_2, \dots, S_n]$ and Reward signal R_{ew} ; **Output:** network output E; 1: initialize weights v and w2: while not converge do attention output $Att_i \leftarrow a_i$ 3: amygdala model output $E_{Ai} \leftarrow Att_i \cdot v_i$ 4: OFC model output $E_{Oi} \leftarrow Att_i \cdot w_i$ 5: network output $E = E_A - E_O$ 6: 7: update the weights of v_i and w_i $v_i \leftarrow v_i + \alpha (Att_i \cdot (Rew - \sum_j E_{Aj}))$ $w_i \leftarrow w_i + \beta (Att_i \cdot (\sum_j E_{Oj} - Rew))$ error $e \leftarrow R_{ew} - E$ 8: if e is small enough then break 9: 10: end while

III. MEMRISTIVE CIRCUIT IMPLEMENTATION OF ATTBEL

MODEL

A. Memristor model

Since memristors are nanoscale devices, the use of computer-aided circuit design is of significant importance for memristor application research [42]–[44]. The choice of device model has a crucial impact on the functionality of the designed circuit. Therefore, it is necessary to select a memristor model that meets the circuit requirements when conducting computeraided circuit design. Generally, memristors can be categorized into threshold and non-threshold types. The resistance state of a non-threshold memristor changes immediately upon the application of an external voltage, while a threshold memristor requires the applied voltage to exceed a certain threshold before its resistance state changes. In the subsequent circuit design of this work, the threshold characteristics of memristors need to be utilized. Therefore, the voltage controlled memristor model proposed in [45] is used in all simulations. The relationship between voltage, current and memristance of memristor is described as:

$$\begin{cases} v(t) = R(t)i(t) \\ R(t) = R_{on}\frac{w(t)}{D} + R_{off}(1 - \frac{w(t)}{D}) \end{cases}$$
(5)

where w(t) is the width of doped region, D is the overall width of the memristor device. R_{on} and R_{off} indicate the lowest and highest resistance value of the memristor, respectively.

$$\frac{dw(t)}{dt} = \begin{cases} \mu_v \frac{R_{on}}{i_{on}} \frac{v_{off}}{i_{on}} f(w(t)), \ v(t) \le V_{T-} < 0\\ 0, \ V_{T-} < v(t) < V_{T+} \\ \mu_v \frac{R_{on}}{D} \frac{i_{off}}{i(t) - i_0} f(w(t)), \ v(t) \ge V_{T+} > 0 \end{cases}$$
(6)

where μ_v represents the average ion mobility, i_0, i_{on} and i_{off} are constants, V_{T+} and V_{T-} are positive and negative threshold voltages of memristor, respectively. f(w(t)) is the window function, which is used to increase the authenticity of the model and describe the non-linearity of the ion migration process. The expression of the window function is described as:

$$f(w(t)) = 1 - \left(\frac{2w(t)}{D} - 1\right)^{2p} \tag{7}$$

To verify the resistance change characteristics of the memristor model, the device parameters are set as: D=3nm, $\mu_v =$ $1.6e^{-17}m^2s^{-1}\Omega^{-1}$, $R_{on} = 1k\Omega$, $R_{off} = 200k\Omega$, $i_{on} = 1$ A, $i_{off} = 10\mu A$, $i_0 = 1mA$, $R_{init} = 190k\Omega$ and $V_{T\pm} = \pm 1.2$ V. The gradual memristance tuning property under a positive or a negative voltage pulse is examined through the PSPICE circuit simulation software. Fig.3 depicts the change process of the memristance under the ± 1.5 V pulse voltage. The memristance decreases with the positive voltage from R_{init} to R_{on} within 2ms, and the memristance increases with the negative voltage from R_{on} to R_{off} within 2ms.



Fig. 3. Simulation results of the memristance change corresponding to applied voltage. (a) voltage pulses applied to the memristor, (b) memristance tuning process corresponding to the applied voltage.

B. Memristor-based selective attention circuit

In order to realize the aggregation and transfer of attention, we use a memristor-based competitive neural network. Each neuron of the network is implemented by a LIFN circuit. The traditional circuit schematic of the LIFN is shown in Fig.4, where V_m is the membrane potential, C_m , and R_m are the membrane capacitance and membrane resistance, respectively. The membrane potential V_m will be integrated, and normally it will be increased until meeting the firing threshold V_{th} . When the firing threshold V_{th} is met, a pulse V_p will be generated and the membrane potential will be reset to V_{reset} . The mathematical model of the LIFN can be written as

$$\begin{cases} C_m \frac{dV_m}{dt} = I(t) - \frac{V_m(t) - V_{reset}}{R} & \text{if } V_m(t) < V_{\text{th}} \\ V_m = V_{reset} & \text{if } V_m \ge V_{\text{th}} \end{cases}$$
(8)

For a constant input, the minimum input to reach the threshold



Fig. 4. Circuit schematic of LIFN

is given by $I_{th} = V_{th}/R$. If the input current is lower than I_{th} , the neuron will not generate any pulses. If the input current exceeds I_{th} , the neuron will fire at a constant frequency. It is worth noting that in a competitive network composed of LIFNs, the neuron that wins competition first will have the opportunity for permanent firing, while neurons that do not win initially will never fire a spike. This principle, known as the winner-take-all principle, is beneficial for selecting the most significant input. However, in the context of visual attention, the focus does not always remain fixed on a single part of an object but changes over time. Therefore, we propose a selfinhibition LIFN (SILIFN) circuit to provide an opportunity for other neurons to win the competition. The designed circuit diagram is shown in Fig.5. The design principle of this circuit is to replace the resistor with a memristor. When the membrane potential exceeds the threshold of memristor, it resistance changes, which affects the activity of the neuron firing. In order to facilitate the subsequent design of competitive and cooperative network, control switch circuits are added to the circuit, as shown in Figs.5(b) and (c). These switches release the charge on the capacitor after being turned on, so that the membrane potential of the neuron is reset to the desired value, thus simulating the competition and cooperation mechanism in the network.

In the circuit diagram, the input voltage is first inverted using an analog inverting circuit consisting of Op-AMP1 and then fed into the inverting integrator composed of Op-AMP2. The membrane resistance R in Fig.4, is replaced by the memristor M in our designed circuit. The firing reset voltage V_1 is set within a range not exceeding the lower threshold voltage V_{T-} of the memristor, allowing the neuron to decrease the membrane resistance after each firing process. As mentioned earlier, the minimum input current required to reach the firing threshold V_{ref1} can be calculated as $I_{th} = V_{ref1}/R_M$. Under the fixed input voltage, the increase of I_{th} results in neuron firing more difficult and achieving the self-inhibition mechanism. The firing spike V_{spi} is generated by comparing the membrane potential V_m and the firing threshold V_{ref1} using the the hysteresis comparator COMP1. When $V_m \geq V_{ref1}$,



Fig. 5. Schematic diagram of the SILIF neuron model where (a) is the circuit diagram of neuron model, (b) is the competition inhibition switch block, (c) is the neighbor cooperation switch block.

 V_{spi} is set to a high-level voltage, and when $V_m < V_{ref1}$, V_{spi} remains at a low-level voltage. It should be noted that in general LIFN circuits, the firing pulse is realized using a monostable trigger. However, for the sake of convenience, in subsequent applications, we employ the method of hysteresis comparison between the inverted membrane potential and a fixed voltage V_{ref2} to obtain a wider voltage pulse, as shown by Op-AMP3 and COMP2 in the circuit diagram.

The switch blocks CIS and NCS in the Fig.5 represent the competition inhibition switch and neighbor cooperation switch, respectively. The voltage source V_2 and V_3 correspond to the reset voltages during the competition and cooperation processes. The competitive inhibition in our network follows the winner-first principle, which is similar to the winnertake-all principle. In a network comprising N neurons, when the neuron N_i fires, the membrane potential of the neuron N_i is reset to V_1 and the membrane potential of all other neurons is set to V_2 . This is achieved using the CIS block. The CIS block consists of N-1 control switches composed of transmission gates and the NOT gates. The control ports $V_{inh1} \dots V_{inh_{N-1}}$ of the switches are connected to the V_{spi} ports of the N-1 neurons, enabling pulse coupling control. Through this mechanism, we can select the neuron with the maximum input value. As time progresses, neurons with large inputs become less likely to fire due to the self-inhibition mechanism, and the neuron with the second-largest input gets the opportunity to fire. Over time, all neurons with large inputs will have the opportunity to fire.

Although the competition mechanism mentioned above can select neurons with large inputs, using only the winner output as the input of the subsequent circuit would result in a limited input range. To address this, we introduce the cooperation mechanism in the network. This mechanism in our designed circuit can be explained as follows: if any of the M neighboring

neurons adjacent to the neuron N_i fires, then the neuron N_i will generate firing pulses, even if its membrane potential does not reach the firing threshold V_{ref1} . This is achieved using the NCS block. The control ports $V_{nc1} \dots V_{ncm}$ of the switches are connected to the V_{spi} port of the neighboring M neurons. When any of the M neighbors fires, the membrane potential will be set to V_3 .

Here we should summarize the functions of the voltage sources in Fig.5 to provide a clear understanding of their roles. V_{ref1} represents the firing threshold of the neuron. When the membrane potential V_m exceeds this value, a firing spike is generated. V_{ref2} denotes the threshold for pulse generation. When the inverted membrane potential exceeds this value, a firing pulse is generated. V_1 is the reset of the neuron after firing. To realize the self-inhibition mechanism of the neuron, its value is set within a range not exceeding V_{T-} of the memristor. V_2 is the reset voltage of competitive inhibition. When any neuron in the network fires, the other neurons are reset to this value. To ensure that the inhibited neurons do not fire pulses, V_2 should be set to below V_{ref2} . V_3 represents the reset voltage for neighbor cooperation. To generate pulses without altering the memristance of the neuron, V_3 is set within the region $V_{ref2} \le V_3 < |V_{T-}|$.

Through the further explanation of the SILIFN, we can know the role of it in the competitive neural network. Then, the competitive network is designed as shown in Fig.6, where each neuron is surrounded by eight adjacent neurons except for the neuron located at the edges. Taking the neuron $N_{2,2}$ as an example, its output pulse is assisted by its surrounding eight neurons, that is, any one of these eight neurons winning in the network competition will result in the generation of pulse of $N_{2,2}$. At the same time, the neuron $N_{2,2}$ also acts as a neighbor of other neurons to cooperate with them to form output pulses. The cooperation is a local behavior and the competition is a global behavior. The firing of any winner in the competitors at V_2 to inhibit the firing behavior of competitors.



Fig. 6. Connection structure of the competition and cooperation network.

To assess the network's performance, we selected a road picture as our research object, depicted in Fig.7(a). For consistency, we set the voltage values as $V_{ref1}=0.4$ V, $V_{ref2}=0.5$ V, $V_1=-1.2$ V, $V_2=0$ V and $V_3=-0.6$ V. Initially, we extracted the salient region of the image using the method described in [33],

resulting in Fig.7(b). Subsequently, we utilized the normalized pixel values from Fig.7(b) as the input for the network. For the purpose of analysis, we intercept a 4×4 pixel block from Fig.7(b) and presented it in Fig.7(c). In Fig.7(c), we can observe that different normalized pixel values correspond to pixel blocks with varying brightness levels. To facilitate a clear comparison of the normalized pixel values, we generated a three-dimensional statistical diagram as shown in Fig.7(d), where the height of each bar graph represents the magnitude of the normalized pixel value. The arrows in Fig.7(c) indicate the transformation direction of matrix stretching into a vector, which serves as the input for the network. The stretched pixels and the corresponding values are presented in Fig.7(e). It is evident that the neuron with the largest input is the fifteenth neuron, followed by the third and then the eighth.



Fig. 7. The road image and its saliency map used to test the performance of the network.



Fig. 8. Firing spikes and raster plot of the winners within 2 milliseconds.

The voltages corresponding to the values in Fig.7(e) were inputted into the network. Fig.8 shows the output spikes of the wining competitive neurons within a two-millisecond interval, along with their firing time raster plot. The figure illustrate the intense competition between neurons N_{15} and N_3 during the initial stage, with spikes firing alternately between these two neurons. Over time, neurons N_8 , N_2 , N_{14} and N_{12} subsequently gain the opportunity to fire. According to the design principles of the circuit network, even though only six neurons win the competition within the two milliseconds, their neighboring neurons also exhibit pulse output. The output pulses of network within the two-millisecond interval are displayed in Fig.9, which will serve as the input for the subsequent circuit. The simulation results confirm the competition and cooperation mechanisms of the network, validating that the designed circuit can effectively focus on the maximum input and facilitate the transformation of attention over time.



Fig. 9. Output pluses of the network within 2 milliseconds.

C. Memristor-based brain emotional learning circuit

In the previous section, we presented a design for a memristive competition network that effectively focuses on the maximum saliency region and facilitates attention transformation over time. Additionally, we incorporated a cooperative mechanism into the network, expanding the output beyond just the winner neuron to include its surrounding neurons. In the following, we propose a memristive emotional learning circuit as a subsequent circuit to the attention network, which integrates the attention mechanism and emotional learning mechanism in the cognitive process to form a system.

The memristive brain emotional learning circuit, shown in Fig.10, is designed based on the learning mechanisms of the amygdala and the orbitofrontal cortex (OFC) in the brain. The operation of the memristive BEL circuit involves two main stages:

Feed Forward Stage: In this stage, the input signal is propagated through the amygdala and OFC circuits. Simultaneously, the error between the output signal E and the target signal is calculated, and a feedback control signal is generated in the feedback control block.

Weight Modification Stage: In this stage, the memristance values of the amygdala and OFC modules are adjusted based on the feedback control signals ΔV and ΔW , respectively. To simplify the circuit implementation, we modify the expressions for ΔV and ΔW as follows:



Fig. 10. Memristive circuit diagram of multi-input single-output BEL

$$\begin{cases} \Delta V = \alpha(S\sum_{j}(Rew - E_{Aj}))\\ \Delta W = \beta(S\sum_{j}(E_{Oj} - Rew)) \end{cases}$$
(9)

where α and β are the learning rates. It should be noted that the resistance of the memristor remains unchanged in the feed forward stage, and the memristance changes according to the feedback signal.

In the amygdala and OFC modules, the memristor V_{ip} exhibits opposite polarity to that of V_{in} , while the memristor W_{ip} has opposite polarity to W_{in} . This ensures that the memristance change of these memristors is opposite under the feedback signal, enabling the implementation of positive and negative weights in these modules. In circuit blocks (a) and (b) of the figure, the input signal *S*, as well as the feedback signals f_{vi} and f_{wi} , are fed alternately into the memristors. This process is controlled by the transmission gate switches, as depicted in the circuit block (d) of the figure. The output E_A of the amygdala module can be mathematically expressed as

$$E_{A} = R(\sum_{i=1}^{m} (\frac{1}{V_{ip}} - \frac{1}{V_{in}}) \cdot H_{i})$$

= $R(\sum_{i=1}^{m} (v_{i}H_{i}))$ (10)

where

$$v_{i} = \frac{1}{V_{ip}} - \frac{1}{V_{in}}$$

$$H_{i} = \begin{cases} S_{i} & \text{if } V_{c} > 0\\ f_{vi} & \text{if } V_{c} < 0 \end{cases}$$
(11)

Similarly, the output E_O of the OFC module can be calculated by

$$E_{O} = R(\sum_{i=1}^{m} (\frac{1}{W_{ip}} - \frac{1}{W_{in}}) \cdot N_{i})$$

= $R(\sum_{i=1}^{m} (w_{i}N_{i}))$ (12)

where

$$w_{i} = \frac{1}{W_{ip}} - \frac{1}{W_{in}}$$

$$N_{i} = \begin{cases} S_{i} & \text{if } V_{c} > 0\\ f_{wi} & \text{if } V_{c} < 0 \end{cases}$$
(13)

The feedback signal f_{vi} and f_{wi} are generated according to the error between the output E and the target T, which can be calculated by

$$V_{err} = E - T$$

$$f_{vi} = S_i \cdot \Delta V$$

$$f_{wi} = S_i \cdot \Delta W$$
(14)

where the feedback control voltage ΔW is the inverse of ΔV , which are

$$\Delta W = -\Delta V = \begin{cases} V_{err} + V_{T+} & if \ V_{err} > 0\\ V_{err} + V_{T-} & if \ V_{err} < 0 \end{cases}$$
(15)

Combing the (9) with (10) and (12), we can obtain the circuit weight update as following

$$\begin{cases} V_{ip}^{\text{new}} = V_{ip}^{\text{olde}} + R/2 \cdot \alpha(S \sum_{j} (Rew - E_{Aj})) \\ V_{in}^{\text{new}} = V_{in}^{\text{olde}} - R/2 \cdot \alpha(S \sum_{j} (Rew - E_{Aj})) \\ W_{ip}^{\text{new}} = W_{ip}^{\text{olde}} + R/2 \cdot \beta(S \sum_{j} (E_{Oj} - Rew)) \\ W_{in}^{\text{new}} = W_{in}^{\text{olde}} - R/2 \cdot \beta(S \sum_{j} (E_{Oj} - Rew)) \end{cases}$$
(16)

where R is the value of reference resistance, V_{ip}^{new} and V_{in}^{new} are the new memristor resistance values of the amygdala module, and W_{ip}^{new} and W_{in}^{new} are the new memristor resistance values of the OFC module. V_{ip}^{olde} , V_{in}^{olde} , W_{ip}^{olde} and W_{in}^{olde} are the old memristor resistance values of the amygdala and OFC modules.

In order to verify the functionality of the designed BEL circuit, the training method involving adjusting the memristive weights to make the output approach to the target is explained in the following. The learning process in the amygdala module and OFC module is illustrated in simulated results shown in Fig.11. The forward propagation and feedback adjustments occur alternately, controlled by the signal V_c . In the first cycle (0-0.1ms), during the forward propagation stage (0-0.05ms), the input signal is set to 1V, which is below the memristor threshold, resulting in no change in memristance. The feedback voltage f_{v1} exceeds the positive threshold of memristor, while the feedback voltage f_{w1} is below the negative threshold voltage of memristor. Consequently, in the amygdala module, the memristance of V_{1p} increases while the memristance of V_{1n} decreases from its initial states. Conversely, in the OFC module, the memristance of W_{1p} decreases while the memristance of W_{1n} increases. As a result, the weight v_1 of the amygdala module gradually decreases, while the weight w_1 of the OFC module increases. The output signal approaches the target value at 1.4ms, but does not exactly match it. In the subsequent stage, the feedback signal slightly modifies the output voltage above the target, resulting in over-learning. However, due to the robustness of the designed module, the output value quickly adjusts to equal to the target value. Finally, at 1.8ms the output voltage equals to the target.



Fig. 11. Learning process of the BEL circuit. V_c is the control voltage of the switch. f_{v1} and F_{w1} are the feedback voltages to the amygdala and OFC, respectively. R_{v1p}/R_{v1n} and R_{w1p}/R_{w1n} are resistance value of memristors in amygdala and OFC, respectively. The output of the network E is drawn in blue.

IV. MEMRISTIVE ATTBEL CIRCUIT AND ITS APPLICATION ON TRAFFIC SIGN RECOGNITION

Traffic sign recognition is a challenging task in the field of multi-classification, as it involves identifying various types of signs with distinct shapes, colors, sizes, and orientations against complex backgrounds. The complex background of signs can be defined as visual senses that contain diverse visual features such as multiple objects, textures, and contextual elements. These backgrounds pose challenges for visual processing systems, as the require the model to effectively focus on relevant information while filtering out irrelevant distractions. Due to the high speed of vehicles on the road and complex backgrounds such as buildings, pedestrians, vegetation in the visual scene of traffic sign recognition, it is of great significance to quickly identify traffic signs to ensure driving safety.

Numerous methods have been proposed for traffic sign recognition, including traditional machine learning approaches, such as Support Vector Machine (SVM) [46], nearest neighbors [47], and random forests [48], as well as deep learning-based techniques such as Convolutional Neural Network (CNN) and its variants [49]. Although the gradually matured deep neural networks have achieved high-precision performance in the task of traffic sign recognition in recent years, the complex structures of these methods restricts their deployment primarily to general-purpose processors, which brings a disadvantage that severely limits the operation speed of the network. On the other hand, the model based on brain emotional learning utilizes the fast learning characteristics of the limbic system, has a simple structure and fast convergence characteristics, which is expected to achieve good performance in tasks with high real-time requirements [25]-[27]. Therefore, we applied the designed AttBEL model in the task of traffic sign recognition.

In China, traffic signs conform to international standards and can be categorized into three main classes: warnings (typically depicted as yellow triangles with a black boundary and informational content), prohibitions (usually depicted as white surrounded by a red circle and also possible having a diagonal bar), and mandatory signs (often represented as blue circles with white informational content). Fig.12 provides a visual representation of a selection of traffic signs from each of these three classes.



Fig. 12. Part of Chinese traffic signs, in C1, C2 and C3 are warning, prohibitory and mandatory signs, respectively.

In the preceding sections, we have accomplished the design and verification of the memristor-based visual selective attention circuit and the brain emotional learning circuit, demonstrating their functionality. To further leverage the advantages of these circuits, we propose integration of the selective attention circuit into the overall emotional learning circuit. This integration aims to enhance the hardware-oriented nature of the entire recognition system and fully harness the capabilities of the circuitry. Fig.13 depicts the schematic of the proposed AttBEL circuit implementation for performing the traffic sign recognition task.

A modular design strategy for the circuit in the PSPICE simulation software is adopted. The overall circuit consists of SLIFN and BEL modules, and the internal circuits of each module are shown in Fig.5 and Fig.10. Initially, the original road traffic image P undergoes pre-processing to extract features by computer software according to the method in [33], resulting in a feature map F(P). Subsequently, the feature map F(P) is fed into visual attention circuit, which incorporates competition and cooperation mechanisms to selectively focus on relevant traffic regions and highlight salient areas within the feature map. The output of the visual attention circuit is multiplied with the feature map F(P) to obtain the input S for the emotional circuit. It should be noted that in the visual attention circuit, a competitive winner triggers the generation of output pulses in surrounding neurons, while neurons farther away from the winner produce zero output. Consequently, the output of the visual attention circuit takes the form of a sparse matrix with predominantly zeros and only a small portion being non-zero. The input S for the emotional learning circuit retains non-zero values around the winner determined by the visual attention circuit, while values away from the winner are set to zero. The BEL circuit utilizes the selected portion of the feature map Att=[$Att_1, Att_2, \ldots, Att_n$], as determined by the visual attention circuit, for traffic sign classification. By leveraging the salient information emphasized by the visual attention circuit, the BEL circuit can effectively classify the

traffic signs present in the input image. The integration of the visual attention mechanism and emotional learning circuit enables an efficient and hardware-focused traffic sign recognition process. The visual attention circuit enables selective focusing on salient regions, while the emotional learning circuit utilizes the identified features for accurate classification. This combined approach offers potential benefits in terms of real-time processing, reduced computational complexity, and improved recognition performance.



Fig. 13. Schematic diagram of the memristive visual attention brain emotional learning network performing the traffic sign recognition tasks.

The proposed AttBEL circuit for sign recognition is summarized in Algorithm 2. The algorithm leverages a combination of computer-aided preprocessing and hardware-based memristive circuits to achieve efficient applications [50]–[52]. Specifically, the input image is preprocessed using computer-aided techniques to extract relevant features, resulting in a feature map that is subsequently fed into the memristive circuit system. In the context of electronic system design, the computeraided design plays a crucial role in reducing the complexity of circuit design while enhancing system efficiency. According to the algorithm, the proposed circuit employs computeraided design to implement a visual attention mechanism and brain emotional leading rule, enabling efficient traffic sign recognition through in-memory computing.

To illustrate the learning process, we present the recognition of a warning sign as an example, as depicted in Fig.14. In Fig.14(a), we have a road image P with size of 256×256 . After performing feature extraction, we obtain the feature image F(P) sized at 32×32 , as shown in Fig.14(b). Next, we input F(P) into the visual attention circuit, and the firing time diagram of the two winners and theirs surrounding neurons in the competition is illustrated in Fig.14(c). In this diagram, the red dots represent the winning neurons, while the blue dots represent the neurons surrounding the winners. The selected regions output by the visual attention circuit are displayed in Fig.14(d). Winner 1, winner 2 and their nearest 15 neighbors are alternately input into the BEL circuit, while the other parts are set to 0. The output of the AttBEL circuit is shown in Fig.14(f). We observe that the yellow signal, representing the warning sign, gradually increases and approaches 1V, while the output signals representing the prohibitory and mandatory signs progressively trend toward 0V. This behavior indicates

Algorithm 2 Traffic sign recognition based on AttBEL

Input: traffic sign image P and traffic sign category T; **Output:** recognized traffic sign class E;

- 1: initialize memristor resistance V_{ip} , V_{in} , W_{ip} and W_{in}
- 2: extract feature map F(P) from the image P with computer-aided
- 3: input F(P) into the visual attention circuit
- 4: while not converge do
- 5: attention circuit output $Att_i \leftarrow F(P_i)$
- 6: amygdala circuit output $E_{Ai} \leftarrow R(1/V_{ip} 1/V_{in}) \cdot H_i$
- 7: OFC circuit output $E_{Oi} \leftarrow (1/W_{ip} 1/W_{in}) \cdot H_i$
- 8: network circuit output $E = E_A E_O$
- 9: error voltage $V_{err} = E T$
- 10: update memristor resistance
 - $V_{ip} \leftarrow V_{ip} + R/2 \cdot \alpha(S \sum_{j} (Rew E_{Aj}))$ $V_{in} \leftarrow V_{in} R/2 \cdot \alpha(S \sum_{j} (Rew E_{Aj}))$ $W_{ip} \leftarrow W_{ip} + R/2 \cdot \beta(S \sum_{j} (E_{Oj} Rew))$ $W_{in} \leftarrow W_{in} R/2 \cdot \beta(S \sum_{j} (E_{Oj} Rew))$
- 11: feedback voltage $f_{vi} = S_i \cdot \Delta V, \ f_{wi} = S_i \cdot \Delta W$
- 12: control voltage V_c to switch the forward and feedback stage
- 13: **if** V_{err} is small enough **then** break

14: end while

that the designed circuit successfully identifies and classifies the traffic signs. Through this example, we demonstrate the effectiveness of the designed circuits in accurately recognizing and classifying traffic signs. The integration of visual attention mechanism and emotional learning circuit enables efficient and accurate processing, leading to improved recognition performance in complex classification tasks.



Fig. 14. Example of the learning process of the proposed network. (a) original road image, (b) saliency map of the road image, (c) raster plot of the visual attention circuit, (d) winners and their surroundings of the attention circuit, (e) part of inputs to the brain emotional learning circuit, (f) output voltage of the three classes of the BEL units.

According to the working principle of the AttBEL circuit designed for traffic sign recognition, the resistance value of the memristor in the circuit is continuously adjusted to facilitate network training with different data inputs. Fig.15 illustrates the distribution of memristor resistance values and their corresponding weights w and v in the BEL circuit modules after training. The colors yellow, red, and blue correspond to the C1, C2 and C3 circuit modules, respectively. From the diagram, it

 TABLE I

 Comparison of traffic sign recognition speed

| literature | model | implementation method | time |
|------------|--------|-----------------------|--------|
| [38] | YOLOv2 | software | 0.017s |
| [40] | CNN | software | 4.289s |
| [39] | YOLOv4 | software | 20ms |
| This work | AttBEL | hardware | <2.5ms |

is evident that the designed AttBEL circuit effectively achieves the positive, zero, and neighbor distribution of neural network weights after training.



Fig. 15. Distribution of memristor resistance values and network weights, (a) distribution of resistance values R_w , (b) distribution of resistance values R_v , (c) distribution of weight values w, (d) distribution of weight values v.

In order to facilitate the display of the speed performance of the memristive in-memory computing circuit in the traffic sign recognition task, we have selected 15 pictures after processing and coding for illustration, as shown in Fig.16. The amplitude of the input voltage pulse in the circuit is determined based on the feature value F(P) of the picture. Each picture is encoded into a voltage pulse with an on-time of 2.5ms and an offtime of 0.5ms, resulting in a change of input data every 3ms. Fig.16(a) presents the 15 data inputs of the first neuron within a 45ms time frame. In Figs.16(b) to (d), the solid lines represent the actual output voltages of the circuit, while the dashed lines represent the expected output values. It is evident from the figure that, with different data inputs, the output voltage of the trained circuit rapidly converges to the expected values within 2.5ms. This verifies that the designed circuit can achieve the function pf traffic sign recognition quickly and accurately. Table I compares the speed performance of the traffic sign recognition based on the proposed memristive in-memory computing circuit with the existing software-based approaches. The table clearly demonstrates that the designed circuit significantly reduces the recognition time for traffic signs.

The design of memristor-based emotional circuit design has garnered significant research interest in recent years. Table II compares the proposed memristive emotional learning model with related works. The study in Ref. [29] integrated context information into emotional learning and utilized the memristive BEL circuit for the character classification task. Refs.



Fig. 16. (a) Input voltage pulse of the first neuron in 45ms, (b) voltage pulse corresponding to class C1, (c) voltage pulse corresponding to class C2, (d) voltage pulse corresponding to class C3.

TABLE II COMPARISON OF MEMRISTIVE EMOTIONAL LEARNING MODEL WITH RELATED WORKS

| literature | mechanisms involved | application |
|------------|--------------------------------|--------------------------|
| [29] | BEL model, context information | character classification |
| [53] | BEL model, Big Five model | emotion generation |
| [54] | BEL model, hippocampus memory | emotion generation |
| [55] | BEL model, fear generation | emotion generation |
| This work | BEL model, attention model | traffic sign recognition |

[53]–[55] combined various mechanism within the emotional learning process and designed memristive circuits for emotion generation. This work introduced a model that integrates the visual selective attention mechanism into the emotional learning model, distinguishing it from the existing models. The proposed model is applied to the task of traffic sign recognition, which holds practical significance in electronic circuits.

V. CONCLUSION AND OUTLOOK

Attention and emotion are crucial components of human cognitive process, yet their combination forms have not been adequately explored in existing research. This paper addresses this gap by proposing an emotional learning model that integrates visual selective attention mechanism. The hardware circuit for the visual attention emotional learning is designed using memristors. The visual attention mechanism is established by the competition and cooperation circuit. The dualloop learning mechanism of emotion is designed through memristor circuit. Finally, this circuit is applied to the task of traffic sign recognition, resulting in fast recognition speed for traffic signs. Circuit simulations have demonstrated its superiority in recognition speed. However, there are some issues are worth further study. In the task of traffic sign recognition, the features need to be extracted by software. An overall circuit scheme which including the feature extraction can facilitate the improvement of efficiency. Additionally, the simulation of the attention mechanism is crude, and many influencing factors and biological characteristics are not taken into account. In the future, we will further optimize the circuit

design and explore the integration of the feature extraction process.

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