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A Design of Rectifier with High-Voltage Conversion Gain in 65 nm CMOS Technology for Indoor Light and RF Energy Harvesting

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Abstract

In rectifier design, the key parameters are the voltage–conversion ratio and the power conversion efficiency. A new circuit design approach is presented in which a capacitor-based, cross-coupled, differential-driven topology is used to boost the voltage–conversion ratio. The scheme also integrates an auxiliary current path to raise the power conversion efficiency. To demonstrate its practicality, two three-stage rectifiers were designed and fabricated using standard 65 nm CMOS technology. The designs were tested under various conditions to assess their performance. The first rectifier targets indoor light energy harvesting applications. It achieves a peak voltage conversion ratio of 3.94 and a maximum power conversion efficiency of 58.7% when driving a 600 Ω load, while supplying over 2 mA of output current. The second rectifier is optimized for RF energy harvesting at 2.4 GHz. Experimental results indicate that it can deliver 70 µA to a 50 kΩ load, with a peak voltage conversion ratio of 5 and a power conversion efficiency of 17.5%.

Keywords: CMOS; cross-coupled differential drive rectifier; energy harvesting; indoor light; multi-stage multiplier; RF energy harvesting; wireless sensor networks

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1. Introduction

Over the past two decades, wireless sensor networks (WSNs) have evolved rapidly, and their integration into the Internet of Things (IoT) has expanded their potential applications in smart manufacturing, smart grids, and intelligent surveillance systems [1–3]. These systems rely on a large number of sensor nodes, many of which must operate in remote or inaccessible locations. Ensuring long-term autonomous operation, therefore, requires methods of harvesting energy from the surrounding environment, minimizing the need for wired power or battery replacements.

Various energy harvesting (EH) techniques have been developed, such as indoor light harvesting using photovoltaic (PV) cells [4,5], RF energy scavenging [6–8], thermoelectric generation [9], and piezoelectric conversion [10]. Among these, PV and RF energy sources are particularly suitable for indoor operation, providing complementary functionality for continuous energy availability [11,12]. In this work, both sources are integrated in a hybrid EH system, as illustrated in Figure 1. A custom-designed DC-to-pulsating-signal converter

enables the PV output to share the same rectifier used for RF input, avoiding the need for bulky off-chip inductors or control circuits [13,14]. The rectified DC power is stored in an energy reservoir (battery or supercapacitor) that supplies key WSN subsystems such as the MCU and transceiver.

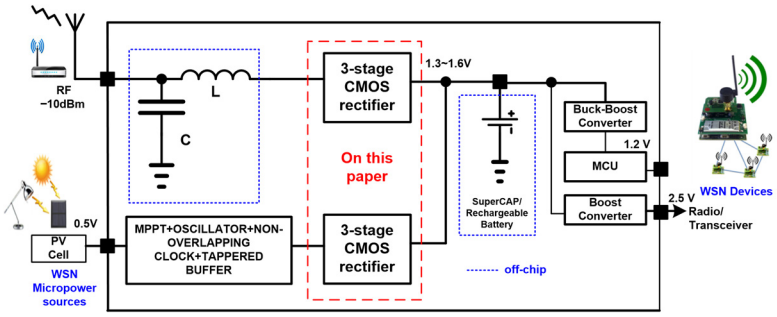


Figure 1. Block diagram of the proposed multi-stage rectifier, including its energy scavenging sources and WSN applications.

The rectifier circuit is the critical block determining the efficiency of the entire EH system. Conventional CMOS rectifiers, however, suffer from several inherent limitations:

(1) Threshold voltage drops across transistors reduce the achievable output voltage and voltage conversion ratio (VCR); (2) leakage and parasitic capacitances lower the power conversion efficiency (PCE); and (3) device mismatch and non-symmetric charge transfer cause efficiency degradation at low input power levels. Cross-coupled differential structures partially mitigate these issues by enhancing gate drive, yet their PCE remains limited under weak input signals and low supply conditions.

To overcome these challenges, this work proposes a capacitor-based, cross-coupled, differential-drive (CCDD) rectifier incorporating an auxiliary PMOS-diode path. The split coupling capacitor increases voltage boosting capability, while the auxiliary conduction path improves charge transfer efficiency and compensates for threshold losses. This combination achieves both higher VCR and PCE under low input amplitude, making it well-suited for compact and energy-constrained IoT sensor nodes.

The remainder of this paper is organized as follows: Section 2 reviews related rectifier topologies. Sections 2.1–2.5 detail the proposed CCDD rectifier and its auxiliary enhancement path. Section 3 presents measurement results and comparisons, and Section 4 concludes the work.

2. Materials and Methods

2.1. Definitions and Notation

Throughout this work, the input signal amplitude V_{IN} refers to the *peak* value of the sinusoidal waveform. When input power is expressed in decibels relative to one milliwatt (dBm) for a 50 Ω system, the corresponding peak and peak-to-peak voltages can be obtained as

$$V_{RMS} = \sqrt{P_{IN} \times R},\ V_P = \sqrt{2P_{IN} \times R},\ V_{PP} = 2\sqrt{2P_{IN} \times R} \quad (1)$$

where P_{IN} is the input power in watts and R = 50 Ω. For example, P_{IN} = 0 dBm (1 mW) corresponds to V_{PP} = 0.632 V across a 50 Ω source.

All simulated and measured waveforms presented in this paper adopt this voltage convention. PCE is defined as

$$\mathrm{PCE} = \frac{P_{OUT,DC}}{P_{IN,AC}} \quad (2)$$

where $P_{OUT,DC}$ is the output DC power delivered to the load, and $P_{IN,AC}$ is the RF power delivered at the rectifier input after de-embedding probe and cable losses. Table 1 provides the list of symbols and abbreviations adopted throughout this work.

Table 1. List of main symbols and abbreviations used in this work.

Symbol	Definition
V_{IN}	Input signal (peak amplitude)
V_{PP}	Peak-to-peak input voltage
V_{DCN}	DC output voltage at the final stage
V_{TH}	Threshold voltage of MOS transistor
V_{DN}, V_{DP}	Voltage drops across NMOS and PMOS devices
V_{DROP}	Total forward voltage drop, V_{DN} + V_{DP}
R_{DS_ON}	ON-state drain–source resistance
C_P, C_S	Pumping and storage capacitors
V_{aux}	Auxiliary voltage generated by the PMOS-diode path
VCR	Voltage Conversion Ratio, V_{OUT}/V_{IN}
PCE	Power Conversion Efficiency, $P_{OUT,DC}/P_{IN,AC}$
β	Transconductance parameter $\mu C_{ox}(W/L)$
m	Device multiplicity (number of parallel fingers)
N	Number of rectifier stages

2.2. Rectifier Architecture and Operation

In the hybrid energy harvesting system discussed earlier, the rectifier plays a central role in converting the low-level AC or pulsating signal from the PV and RF sources into a stable DC output. The performance of the entire energy harvesting module, therefore, depends critically on the rectifier's ability to achieve high VCR and PCE under low input amplitude. Designing such a circuit requires balancing multiple trade-offs, including device sizing, leakage reduction, and voltage boosting capability. To provide a foundation for the proposed design, this section first reviews conventional CMOS rectifier structures, discusses their limitations, and then introduces the improved CCDD rectifier with an auxiliary PMOS path.

CMOS rectifiers rely on transistors that act as switches to turn the AC input into DC. In EH applications, the input signal is weak, so a single-stage rectifier cannot reach the voltage needed to charge a battery. Designers therefore employ multi-stage rectifiers to raise the output voltage. This approach, however, creates a trade-off: increasing voltage often lowers PCE. A higher output voltage can be obtained only by reducing the forward voltage drop V_{DROP} [15,16], which equals the peak output current I_D multiplied by the on-state resistance R_{DS_ON} of each transistor.

To reduce R_{DS_ON}, larger transistors are typically preferred. However, increasing transistor size adversely affects PCE, as it lowers the OFF-state resistance, thereby increasing reverse leakage current [17,18]. This trade-off complicates the design process, since optimizing both output voltage and efficiency simultaneously is challenging. Consequently, developing rectifier circuits that can deliver high output voltage while maintaining high PCE requires innovative and carefully balanced design strategies.

The dependence of the forward voltage drop V_{DROP} on the threshold voltage V_{TH} has prompted numerous threshold-cancelation schemes [19–24]. A widely adopted approach is the capacitor-based, cross-coupled, differential-drive (CCDD) structure [16,17,23,25], which effectively reduces the negative impact of V_{TH} on both VCR and PCE. Among these techniques, the CCDD architecture has become a standard design, illustrated in Figure 2a [23].

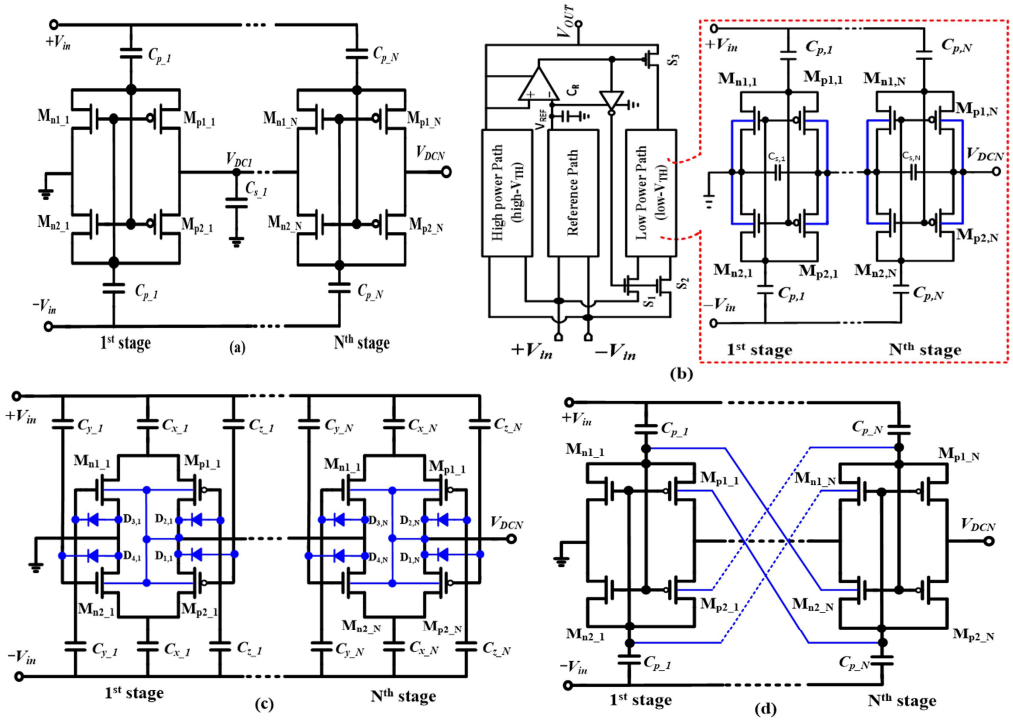


Figure 2. Overview of multi-stage rectifier architectures: (**a**) traditional CCDD configuration [23]; (**b**) dual-path scheme using low- and high-*V*TH transistors [26]; (**c**) self-biased design [17]; and (**d**) body-driven technique [25].

Parallel efforts to enhance rectifier performance have led to several innovative schemes. One design [26], shown in Figure 2b, employs dual-current paths combining low- and high-V_{TH} transistors to improve sensitivity and PCE. Another approach [17], shown in Figure 2c, uses a self-biased structure with feedback through diode-connected transistors to suppress reverse leakage while preserving efficiency. Figure 2d depicts the dynamic threshold control method in [25], which modulates the bulk voltage to vary V_{TH} dynamically, further enhancing sensitivity and efficiency.

The preceding discussion shows that most recent work focuses primarily on improving PCE, while relatively few studies address boosting output voltage, or equivalently, the VCR, which is crucial for efficient battery charging. Cascading multiple stages increases voltage but also adds parasitics and complexity. Therefore, an ideal rectifier should achieve high output voltage with as few stages as possible to maintain simplicity and high efficiency.

2.3. Analysis of Conventional CCDD Circuit Structure

Earlier sections introduced the CCDD topology, one of the most widely used CMOS rectifier schemes. Figure 3 outlines its operation. The discussion that follows examines a single CCDD stage. In this circuit, pumping capacitors C_P move charge in tandem with the NMOS and PMOS switches. Differential inputs, $\pm V_{IN}$, start the rectification process; V_{DN} and V_{DP} mark the drops across the NMOS and PMOS devices, respectively. The first stage produces a DC node V_{DC1} that is stored on capacitor C_{S1} and also feeds the next stage.

For clarity, the subsequent analysis considers only the forward-conduction losses of the NMOS and PMOS switches. Because the CCDD topology is symmetric and operates differentially, studying a single half-cycle is enough to extract the resulting DC output voltage.

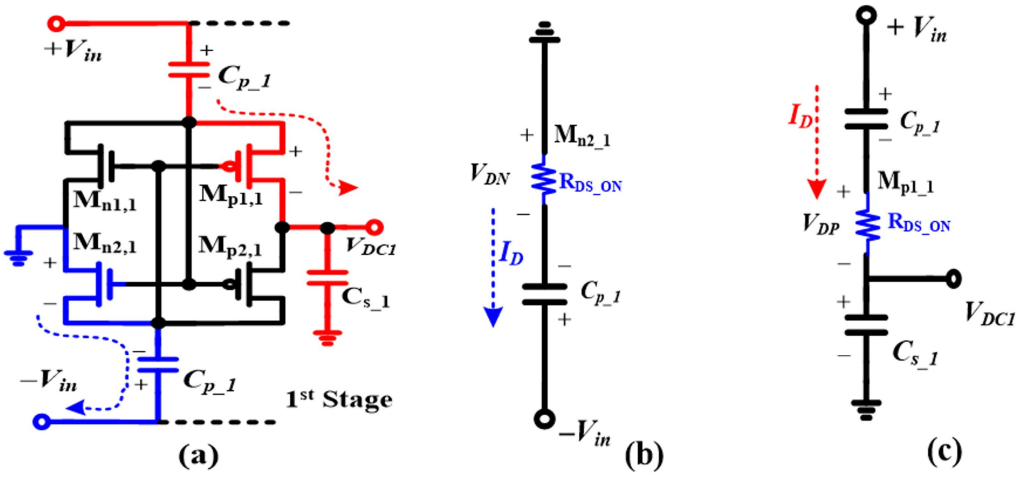


Figure 3. 1st stage bisection of the standard CCDD rectifier: (**a**) biasing profile, (**b**) charge phase, and (**c**) discharge phase.

In the first half-cycle, when $|V_{IN}| > V_{TH}$, the positive input ($+V_{IN}$) switches on NMOS M_{n2_1}. The device then presents its on-state resistance R_{DS_ON}, creating a low-impedance path for current to flow from ground toward $-V_{IN}$. At the same moment, the negative input ($-V_{IN}$) biases PMOS M_{p1_1} into conduction, directing charge from $+V_{IN}$ through the pump capacitor C_{P1} into the storage capacitor C_{S1}.

In the subsequent half-cycle, the roles of the transistors reverse: M_{n1_1} and M_{p2_1} conduct while M_{n2_1} and M_{p1_1} are turned off. By applying KVL during the charging phase, illustrated in Figure 3b, the corresponding voltage relationships and resulting equations for the expected DC output can be derived.

$$-V_{in} - V_{cp\_1} + V_{DN} = 0 \tag{3}$$

Rearranging Equation (3) gives the peak voltage V_{cp_1} across the pumping capacitor C_{p1}, thus we obtain

$$V_{cp}\_1 = -V_{in} + V_{DN} \tag{4}$$

In the discharge half-cycle illustrated in Figure 3c, the peak input signal is given by

$$+V_{in} = V_{cp}\_1 + V_{DP} + V_{DC1} \tag{5}$$

Substituting Equation (4) into Equation (5) yields the following expression for the output DC voltage of a single-stage rectifier,

$$V_{DC1} = 2V_{in} - (V_{DN} + V_{DP}) \tag{6}$$

The first stage's rectified voltage, V_{DC1}, serves as the input supply for the next stage. Because each stage uses the same circuit configuration, the overall DC output of a conventional N-stage CCDD rectifier can be estimated as

$$V_{DCN} = N\,[2V_{in} - (V_{DN} + V_{DP})] \tag{7}$$

As the analysis shows, the anticipated voltage-doubling effect is constrained by the cumulative forward voltage drop ($V_{DROP} = V_{DN} + V_{DP}$) across the conducting NMOS and PMOS transistors. This drop negatively affects both V_{DC1} and the final output voltage V_{DCN}. To achieve a higher output voltage, it is essential to minimize V_{DN} and V_{DP} as much as possible. However, while factors such as the load current (I_L) and the transistor sizing (i.e.,

width-to-length ratio) can significantly influence the rectifier's power-conversion efficiency, their impact on boosting the output voltage remains relatively limited [27,28]. Therefore, mitigating the effects of V_{DROP} requires innovative circuit design strategies, as it cannot be addressed effectively through basic transistor sizing alone.

2.4. Study of the Capacitor-Based CCDD Rectifier Topology

Equation (5) implies that adding an auxiliary voltage V_{aux} can increase the rectifier's output by compensating for the voltage drops in the last two terms. The resulting relationship is given by

$$V_{DCN} = N\,[2V_{in} - (V_{DN} + V_{DP}) + V_{aux}] \tag{8}$$

The V_{aux} in Equation (8) may be derived from on-chip circuitry or fed from an external source. To demonstrate the practical feasibility of this concept, a three-stage prototype rectifier was developed and is depicted schematically in Figure 4. To implement the V_{aux} term, two key modifications were introduced relative to the baseline CCDD architecture, both highlighted in blue within the schematic. The first enhancement involves adopting a capacitor-based CCDD structure, which facilitates voltage boosting by leveraging additional charge transfer paths.

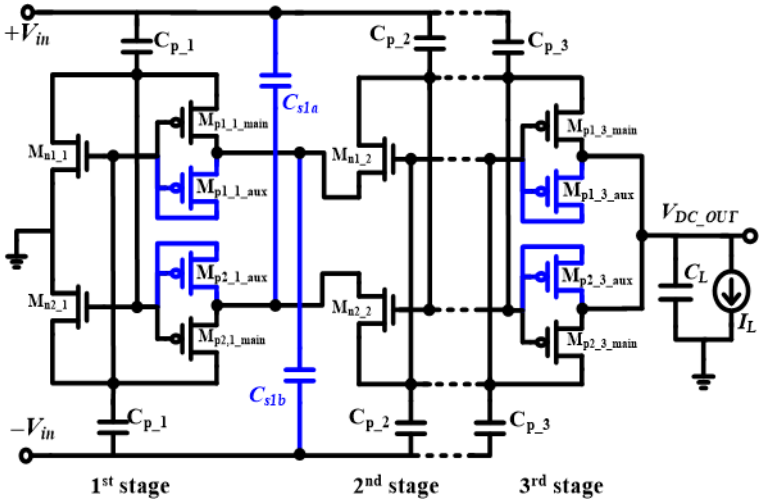


Figure 4. Three-stage CCDD rectifier design featuring capacitor coupling and auxiliary MOS elements.

In contrast to the conventional designs shown in Figures 2a and 3, the storage capacitor C_S, typically placed between the first and second stages, is divided into two separate capacitors, denoted as C_{S1a} and C_{S1b}. Furthermore, two PMOS transistors that are diode-connected are incorporated into the rectifier to counteract and mitigate the efficiency degradation introduced by the additional passive components. The theoretical analysis and operational impact of these two design modifications are discussed in detail in the following subsections.

Due to the differential topology, each split capacitor is set to one-half of the original C_{S_1} value and placed symmetrically, ensuring identical operation in both half-cycles. During the positive half-cycle, C_{S1b} operates with Mp_1 and Mn_2; during the negative half-cycle, C_{S1a} pairs with Mp_2 and Mn_1. Each split capacitor links the complementary input line to its corresponding complementary output node in the stage. As a result, during the discharging phase, the complementary input signal contributes additional voltage, effectively boosting the DC output.

The steady-state charge and discharge behavior of this capacitor-enhanced CCDD rectifier is illustrated in Figures 5a and 5b, respectively. Applying the analytical procedure used for the conventional CCDD rectifier shows that the charging phase follows the same

expressions as Equations (3) and (4). However, analyzing the discharging cycle under this modified structure leads to an updated expression for the voltage across the pumping capacitor V_{cp_1}, given by

$$+V_{in} = V_{cp\_1} + V_{DP} + V_{Cs1b} - V_{in} \tag{9}$$

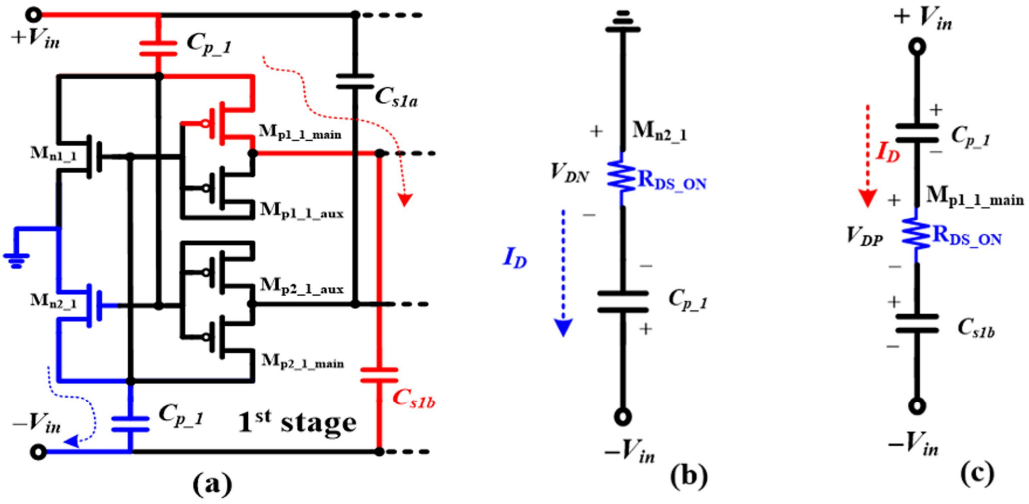


Figure 5. 1st stage bisection of the proposed three-stage CCDD rectifier: (**a**) bias network, (**b**) charge phase, and (**c**) discharge phase.

Substituting Equation (4) into the modified discharge expression in Equation (9), the resulting voltage across the storage capacitor V_{Cs1b} can be expressed as

$$+V_{in} = -V_{in} + V_{DN} + V_{DP} + V_{Cs1b} - V_{in} \tag{10}$$

Rearranging Equation (10) yields the expression for the split storage capacitor C_{s1b} voltage in the proposed rectifier architecture,

$$V_{Cs1b} = 3V_{in} - (V_{DP} + V_{DN}) \tag{11}$$

With the input signal V_{IN} reversed, the split-capacitor voltage V_{Cs1a} behaves identically to that given in Equation (11). It should be noted that the split-capacitor configuration is applied only between stages. As a result, each of these intermediate stages contributes roughly three times the input voltage, compared to two times per stage in the conventional design shown in Equation (7). However, in the final stage, the outputs are directly connected to the load without using split capacitors. This means the last stage contributes only twice the input voltage. With this combination of a differential structure in the intermediate stages and a standard output stage similar to the classical CCDD design, the total DC output voltage of an N-stage rectifier can still be reasonably estimated based on this mixed configuration and expressed as

$$V_{DCN\_NEW} = N\,[3V_{in} - (V_{DN} + V_{DP})] - V_{in} \tag{12}$$

Equations (7) and (12) show that the proposed architecture gains an additional V_{IN} per stage in the rectified output voltage.

2.5. Analysis of the Auxiliary Path Designed to Boost PCE

It is important to recall that both V_{DN} and V_{DP} in Equation (10) are closely linked to the ON-state resistance R_{DS_ON}. Minimizing R_{DS_ON} is desirable for improved performance; however, this comes with several design trade-offs that complicate the overall optimization process. To address this, a novel design strategy is introduced, as illustrated in Figure 6a. Two diode-connected PMOS devices are introduced to create auxiliary current paths. Because the circuit is symmetrical and driven by differential inputs, the discussion is limited to the upper switching branch, shown in Figure 6b.

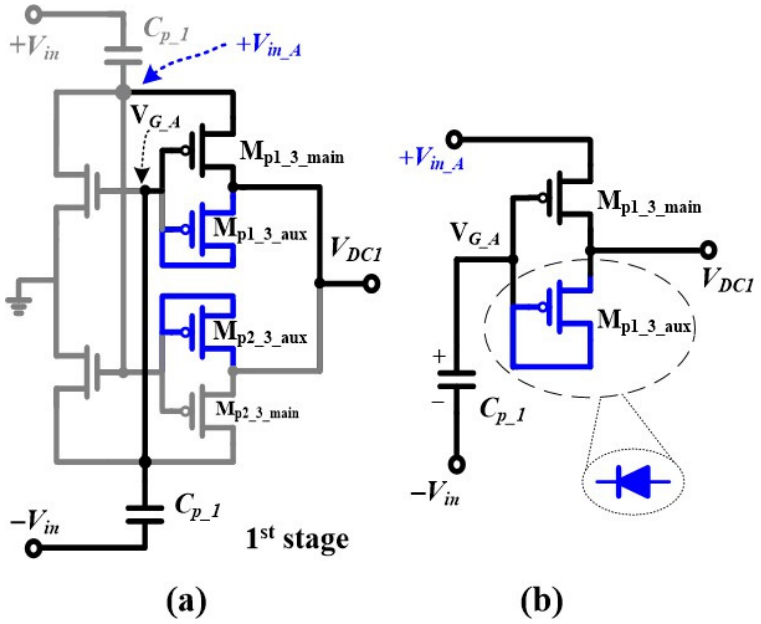


Figure 6. Proposed rectifier featuring auxiliary pathways: (**a**) first stage schematic, (**b**) analysis, including the auxiliary PMOS device.

In the positive half-cycle, $+V_{IN}$ exceeds $-V_{IN}$, and PMOS M_{p_N} conducts once $(+V_{IN\_A} - V_{G\_A}) \geq |V_{THp\_N}|$. A basic diagram is provided in Figure 6b. The gate potential V_{G_A} is limited by the body diode linking the drain and bulk of the auxiliary PMOS $M_{p\_N\_aux}$ and its source-gate voltage V_{SG}. Evaluating the output-node voltages under these constraints yields the relationship that follows

$$V_{DC\_OUT} = V_{SG\_aux} + V_{Cp\_N} - V_{in} \tag{13}$$

The voltage at the $+V_{IN\_A}$ node can be written as

$$V_{in\_A} = V_{SG\_main} + V_{Cp\_N} - V_{in} \tag{14}$$

Here, the source-to-gate voltages of the auxiliary and main PMOS transistors are V_{SG_aux} and V_{SG_main}. Taking away Equation (14) from Equation (13) yields the DC output voltage, V_{DC_OUT}, as

$$V_{DC\_OUT} - V_{in\_A} = V_{SG\_aux} - V_{SG\_main} \tag{15}$$

At this point, the terms V_{CP_N} and V_{in} cancel out, and with additional simplification, the expression can be further reduced to its final form,

$$V_{DC\_OUT} = V_{in\_A} - (V_{SG\_main} - V_{SG\_aux}) \tag{16}$$

When V_{in} falls below the output by roughly one threshold voltage V_{TH}, the auxiliary PMOS transistor $M_{p\_N\_aux}$ operates in weak inversion. As V_{in} rises and exceeds the output by at least V_{TH}, this diode-connected device (V_{DS} = V_{SG}) shifts into strong inversion (saturation) [28]. The main PMOS M_{p_N} stays in the linear (ohmic) region, keeping R_{DS_ON} low and conduction losses small. When the source node sits one V_{TH} above the output, the diode current through $M_{p\_N\_aux}$ can be approximated as follows [28]:

$$I_{SD} \cong \frac{1}{2}\beta V_{SG} - \left|V_{TH\_p}\right| \tag{17}$$

solving V_{SG} at the saturation region as

$$V_{SG} \cong \left|V_{TH\_p}\right| + \frac{2I_{SD}}{\beta} \tag{18}$$

The approximate ohmic current flowing through M_{p_N} in the linear region is given by

$$I_{SD} \cong \beta V_{SG} - \left|V_{TH\_p}\right| - V_{SD} \tag{19}$$

solving V_{SG} at the ohmic region as

$$V_{SG} \cong \left|V_{TH\_p}\right| + \frac{I_{SD}}{\beta V_{SD}} \tag{20}$$

With

$$\beta = \mu_p C_{ox} \frac{W}{L} \tag{21}$$

Here, β is a technology-dependent constant that incorporates the hole mobility (μ_p), the gate oxide capacitance per unit area (C_{ox}), and the geometric parameters of the transistor, namely the gate width (W) and length (L). By substituting Equations (18) and (20) into Equation (16), the resulting expression for V_{DC_OUT} can be derived as

$$V_{DC\_OUT} = V_{in\_A} - \left|V_{TH_{main}}\right| - \left|V_{TH_{aux}}\right| + \frac{I_{SD}}{\beta V_{SD}} - \frac{2I_{SD}}{\beta} \tag{22}$$

Equation (22) indicates that the diode-connected PMOS devices placed in the auxiliary paths serve as V_{TH} compensators for the main PMOS transistors within the rectifier. PCE depends on the threshold voltage offset, the actual V_{TH} of the conducting devices, the rectifier stage count, and the load current I_L. By compensating the threshold drop, the auxiliary network lessens the impact of the equivalent series resistance introduced by the additional passive components, thus improving the total efficiency of the capacitor-enhanced CCDD rectifier. Consequently, the circuit achieves improved DC voltage extraction along with higher conversion efficiency.

To accurately evaluate the effect of this threshold-compensation scheme, all transistors in this work were intentionally designed with long channel lengths ($L > L_{min}$) despite the use of a 65 nm CMOS process. Choosing device lengths substantially longer than the minimum—specifically 0.18 µm and 0.20 µm—suppresses short-channel effects such as velocity saturation and DIBL. This results in device behavior that more closely aligns with classical long-channel MOSFET characteristics, making the analytical square-law model in (17) a reasonable first-order approximation for the operating region of interest.

All simulations were performed using licensed Synopsys HSPICE together with the TSMC 65 nm CMOS PDK, which includes the foundry-supplied BSIM4 transistor models. The use of long-channel devices within a BSIM4-based simulation environment provides a

consistent and practical framework for validating the analytical behavior predicted by the square-law model.

Figure 7 presents schematic-level simulation results (bond-pad and I/O-pad parasitics excluded) that compare several circuit variants. Each variant is evaluated at a 2.4-GHz RF sinusoidal input to highlight the influence of the split capacitors and auxiliary paths.

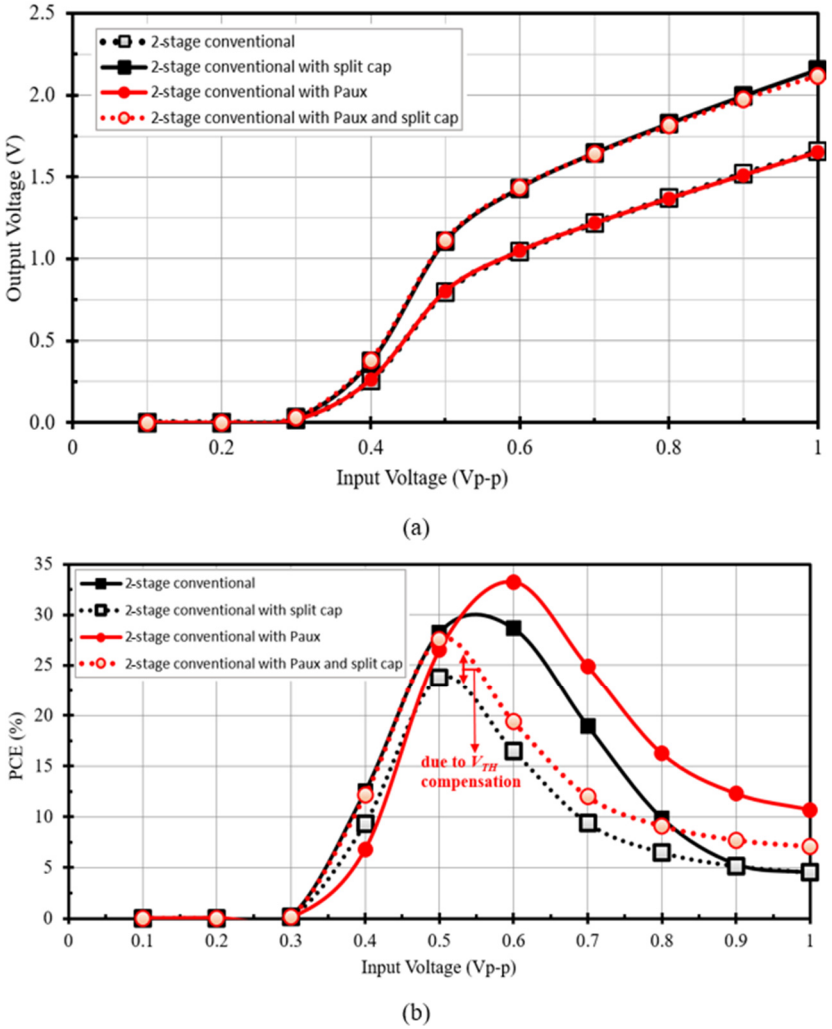


Figure 7. Simulated comparison of alternative two-stage rectifier topologies at 2.4 GHz under a 100 kΩ load: (**a**) output voltage *V*out; (**b**) PCE.

2.6. Indoor Light Energy Harvesting Rectifier Design

A three-stage rectifier based on the proposed technique was built for indoor light EH. Figure 8 presents the full block diagram of this system. As illustrated, a single unit PV cell with a nominal 0.5 V output voltage is used in this design. A ring oscillator is designed to convert the energy from the DC output voltage to AC. The operation frequency of the ring oscillator is selected to be 12.5 MHz so that the undesired switching loss can be minimized, and an optimum loading current can be maintained.

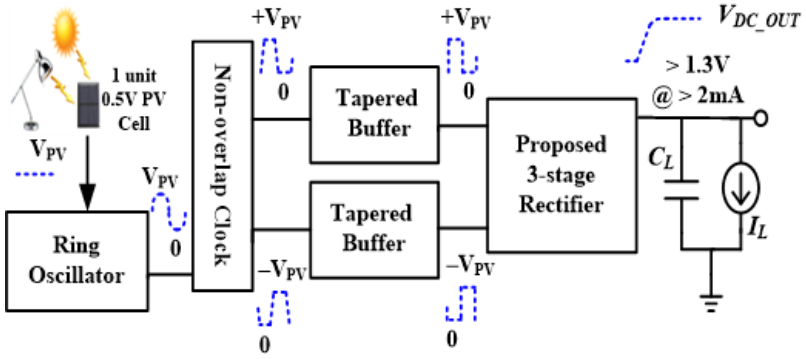


Figure 8. Indoor light energy harvesting unit block diagram [29].

The AC signal generated by the oscillator is then fed to a non-overlapping clock generator. The output of the clock generator provides the required differential AC excitation to the rectifier through a tapered buffer. For consistency with the RF rectifier in the next subsection, the input AC amplitude used for both simulation and measurement of this 12.5 MHz rectifier is also referenced to a 50 Ω source impedance. All voltage and power values reported for this design follow this 50 Ω convention.

Figure 9 presents the schematic diagram along with the corresponding chip-level measurement results of the ring oscillator, non-overlapping clock generator, and output buffer.

The detailed circuit design and operational principles of these three building blocks were thoroughly discussed in our earlier work [29]. The ring oscillator and the non-overlapping clock only consumed a few nanowatts due to their digital switching capabilities. On the other hand, the taper buffer occupied the most significant area in the die to generate a robust pulsating signal and to drive the rectifier's milliampere load requirements. The measured peak efficiency from the PV cell source to the rectifier was only around 35%.

The rectifier was set up according to the following baseline parameters:

1. The capacitor (C_L) and load resistor (R_L) were set to initial values of 1 nF and 100 Ω, respectively.
2. The pump capacitor C_P was chosen to be 15× larger than each storage capacitor (C_{S1a} and C_{S1b}); thus, C_P was set to 10 nF.
3. Initial transistor dimensions were PMOS width W_P = 3 µm, NMOS width W_N = 1 µm, and channel length L = 0.1 µm. Larger widths may later be selected to further lower R_{DS_ON}
4. Device multiplicity was set with multiplier m = 500 and finger count f = 2.

Earlier analysis showed that the DC output voltage of the rectifier depends heavily on the input AC amplitude and the values of capacitors C_{s1a_b} and C_p. To explore this dependency, a simulation study was conducted to examine how the ratio of these capacitors affects the DC output voltage. The results are shown in Figure 10. As shown in Figure 10a, the parametric simulation of the coupling capacitor C_p reveals that the output voltage begins to saturate when C_p = 30 nF and the capacitor ratio $x = C_p/C_{s1a\_b}$ = 5. Beyond this ratio, further increasing C_p does not lead to noticeable improvements in output voltage. A similar trend is observed in the parametric simulation of PCE, as illustrated in Figure 10b. Setting C_p = 30 nF and $C_{s1a} = C_{s1a\_b}$ = 6 nF provides the best trade-off, giving the highest simulated DC output voltage and a PCE of 55.1%. Because the DC level rises with the charge stored on C_p and C_{s1a_b}, efficiency improves up to this point. Beyond these capacitance values, however, additional loading from C_{s1a_b} exceeds the circuit's capability, and PCE begins to fall. Additionally, Figure 10c shows that the rectifier achieves a peak simulated

efficiency of 60.7% when the transistor multiplication factor is increased to m = 1000, as determined through a separate parametric simulation.

The transistor multiplication factor was determined through simulation to achieve optimal power conversion efficiency while providing sufficient current driving capability to support an output load ranging from 2 mA to 8 mA. As a result, an optimized DC output voltage of 1.98 V was achieved from an input voltage of 0.5 V.

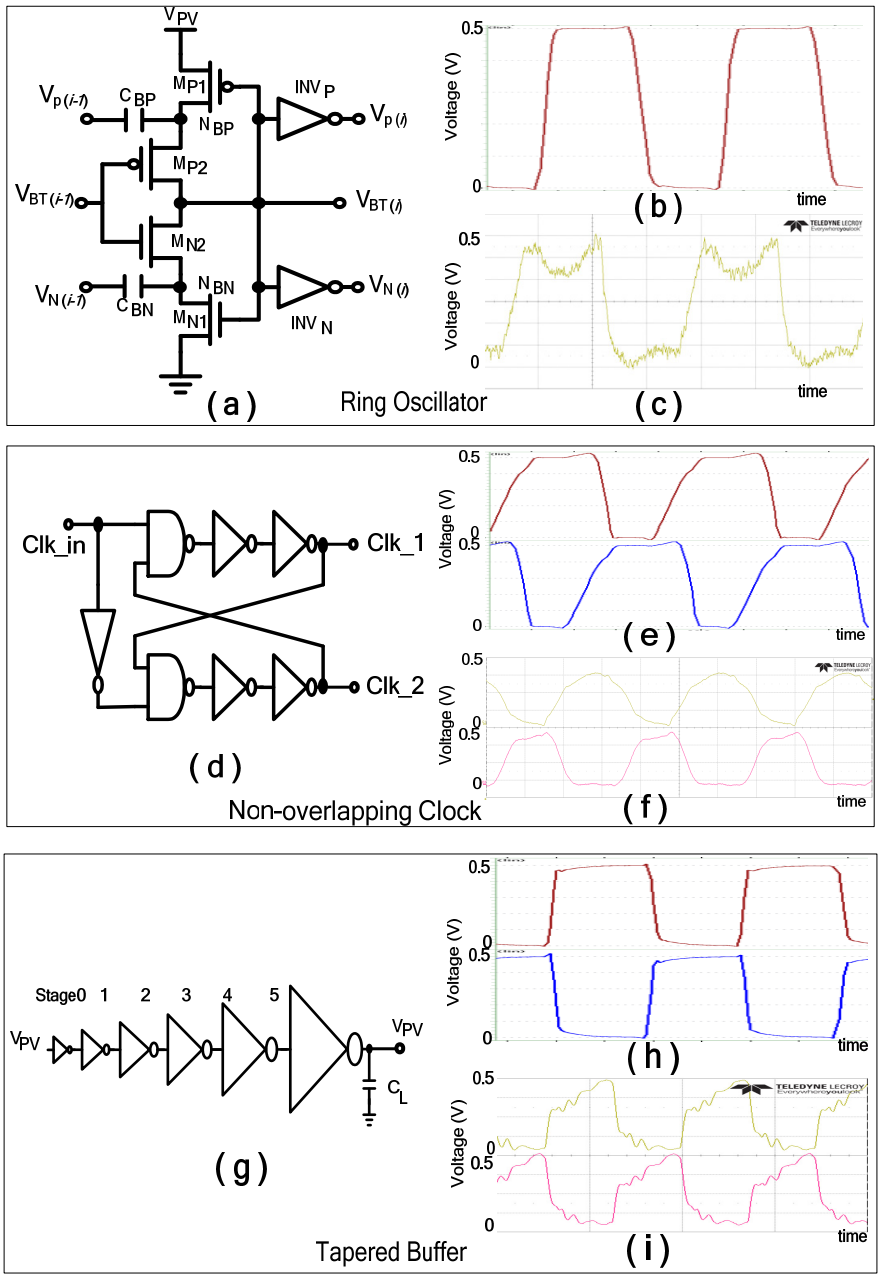


Figure 9. DC-Pulsating signal conversion circuit blocks and waveforms: Bootstrapped ring oscillator, (**a**) schematic, (**b**) post-layout waveform (16 MHz), (**c**) chip measurement waveform (12.5 MHz); Non-overlapping clock: (**d**) schematic, (**e**) post-layout waveform (16 MHz), (**f**) chip measurement waveform (12.5 MHz); Tapered buffer: (**g**) schematic, (**h**) post-layout waveform (16 MHz), (**i**) chip measurement waveform (12.5 MHz).

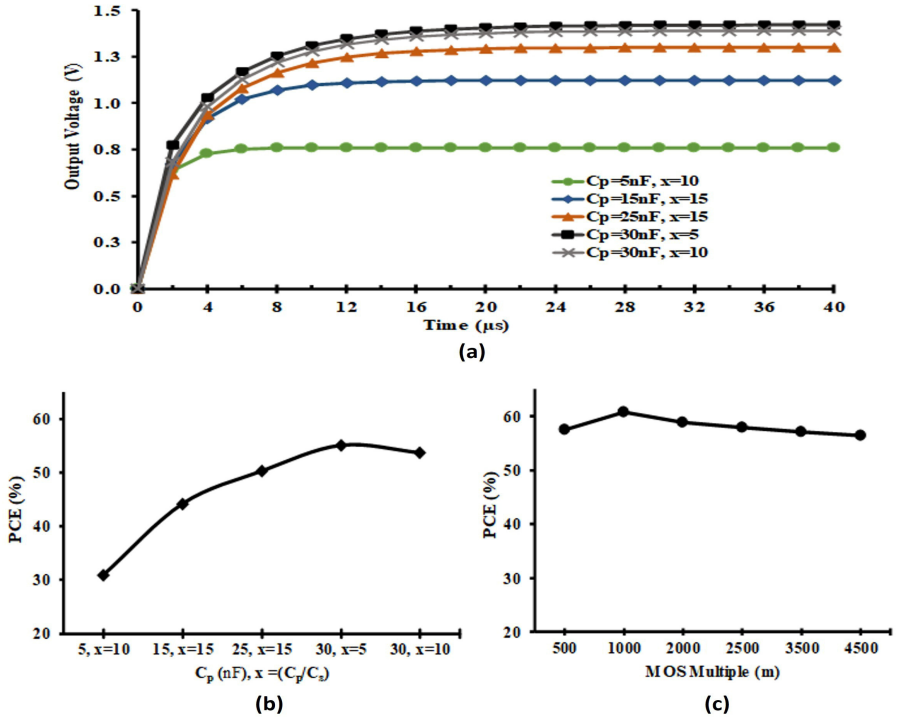


Figure 10. Parametric study of the indoor light EH rectifier: (**a**) output voltage versus capacitance, (**b**) PCE versus capacitance, and (**c**) PCE versus transistor size. Note that x is the ratio between Cp and $Cs1a\_b$, $Cs1a = Cs1b = 6$ nF, $Cp = 30$ nF, $CL = 1$ nF, $(W/L)n = 1.6$ µm/0.2 µm, and $(W/L)p = 4.8$ µm/0.2 µm.

Area–efficiency trade-offs are inherent in CMOS rectifier design. Increasing transistor multiplicity (m) and on-chip capacitor sizes reduces conduction loss and improves the voltage conversion ratio; however, these choices directly increase the silicon area and introduce larger parasitic capacitances, which can reduce the overall power conversion efficiency at higher frequencies. Conversely, reducing the number of rectifier stages or capacitor sizes decreases chip core area but limits the achievable output voltage. In this design, the selected transistor widths, capacitor sizes, and number of stages were chosen to meet the target output voltage and conversion ratio while keeping the chip area moderate and avoiding excessive parasitic-induced power losses.

2.7. Rectifier Design for 2.4 GHz RF Energy Harvesting

Designing the 2.4 GHz RF EH rectifier introduces additional challenges not encountered in the indoor-light version. Harmonic Balance analysis is performed with a CMOS RF model, a 50 Ω source, a 2.4 GHz carrier, and a swept input power range. At this frequency, the rectifier cannot drive large capacitors efficiently. As a result, the pumping capacitor C_p is limited to values between 0.2 pF and 1 pF, while the cross-coupled capacitors C_{s1a_b} are constrained to just a few femtofarads. This limitation significantly restricts the output current driving capability, with simulations indicating a maximum current of only 72.8 µA at the output node.

Using the same design approach as the indoor light EH rectifier, the starting values are set to $C_p = 0.2$ pF and $C_L = 1$ pF, with an initial load resistance of 10 kΩ. Subsequent parametric simulations are performed to optimize key design variables—transistor multiplicity (m), number of fingers (f), and aspect ratio (W/L)—concerning output loading capability and input sensitivity.

Figure 11a presents the simulated output voltage within the range of input power levels. With optimized capacitor and transistor parameters, the load resistance is further

varied to assess the loading performance of the rectifier. The highest output voltage is observed when a load of 50 kΩ is applied, while lower resistance values lead to a degradation in output voltage. Figure 11b plots the rectifier's PCE versus input power, indicating that peak efficiency is obtained with a 50 kΩ load.

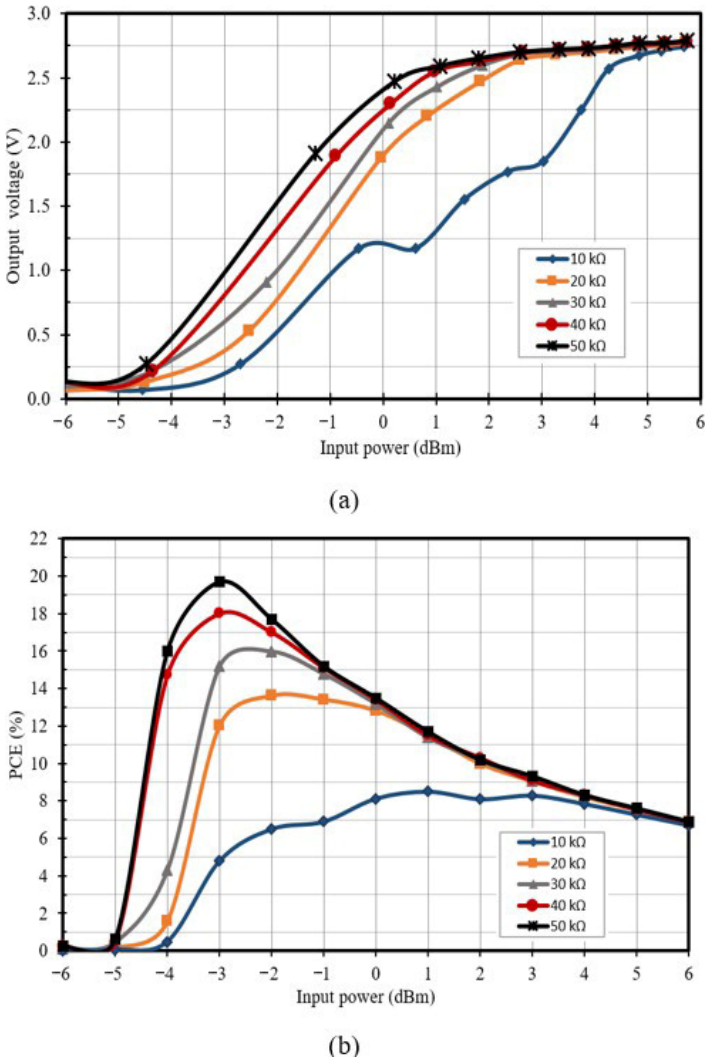


Figure 11. Parametric evaluation of the 2.4 GHz RF energy harvesting rectifier: (**a**) output voltage vs. input power, (**b**) PCE vs. input power. Parameters: $Cs1a\_b$ = 70 fF, Cp = 0.7 pF, CL = 5 pF, $(W/L)p$ = 6 µm/0.2 µm, $(W/L)n$ = 2.2 µm/0.18 µm. Input power is referenced to 50 Ω; voltages denote peak values.

3. Results

3.1. Measurement Setup

To validate the proposed architecture, four rectifier chips were fabricated using 65 nm 1P9M CMOS RF technology. Two units were aimed at indoor light energy harvesting, and two at 2.4 GHz RF harvesting. Figure 12 shows die photographs of all four chips. The indoor light rectifier occupies 0.183 mm^2, while the 2.4 GHz version uses only 0.018 mm^2. Each device is housed in a 44-pin quad flat package (QFP).

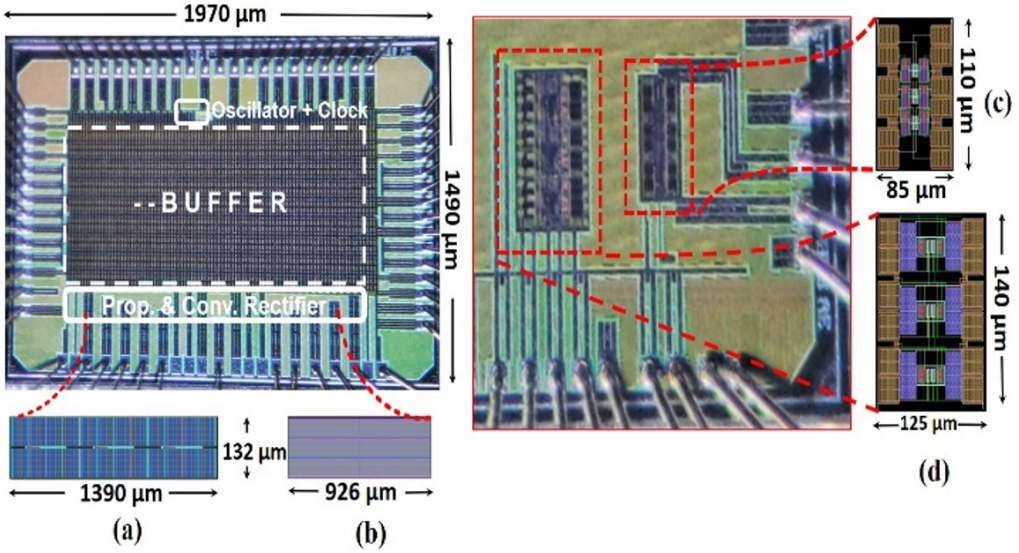


Figure 12. Die micrographs of the fabricated rectifiers: (**a**) proposed indoor light rectifier, (**b**) conventional indoor light version, (**c**) standard 2.4 GHz RF rectifier, and (**d**) proposed 2.4 GHz RF rectifier.

The 2.4 GHz rectifier was characterized using a signal generator (USRP Tx) and a spectrum analyzer (GW Instek) to evaluate its standalone RF-to-DC conversion performance, as shown in Figure 13. Due to the absence of a die-probing station, de-embedding of the measurements was not performed. Instead, pad and package parasitics were accounted for in both simulation and experimental evaluation, ensuring that the results reflect the fabricated device. In this study, the rectifier was intentionally tested without an LC matching network, so that the measured efficiency corresponds solely to the rectifier's intrinsic performance. This setup provides a first-order assessment of the rectifier's behavior at the target frequency. Whereas, to characterize the performance of the designed rectifier for the indoor light PV energy harvesting system, a mixed-domain oscilloscope (Tektronix MDO4104C) and two digital multimeters were used, following the measurement setup shown in Figure 14. Figure 15 presents the time-domain waveform of the indoor light PV-EH rectifier, including a zoomed-in view of the ripple voltage. The measured ripple is approximately 60 mV, with an average output voltage of 1.98 V and a settling time of 28 µs under a 600 Ω load and C_L = 5 nF.

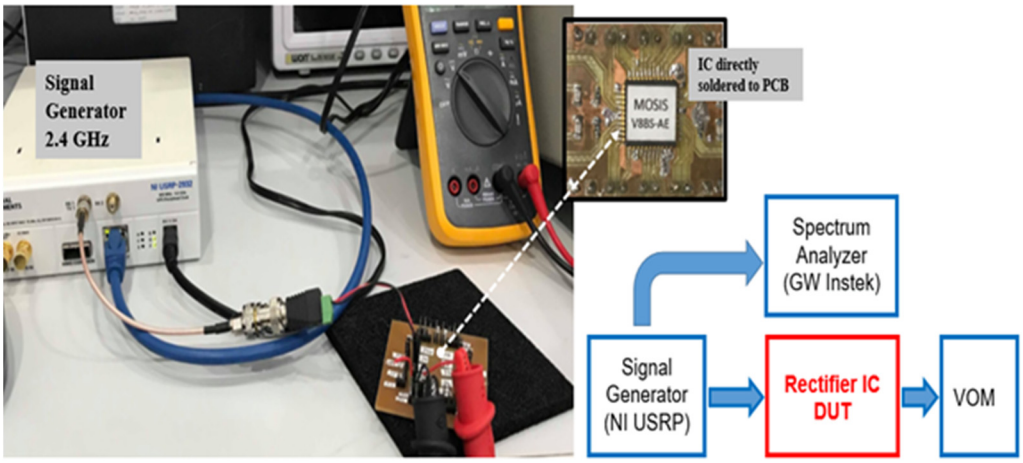


Figure 13. Measurement setup for evaluating the standalone 2.4 GHz rectifier.

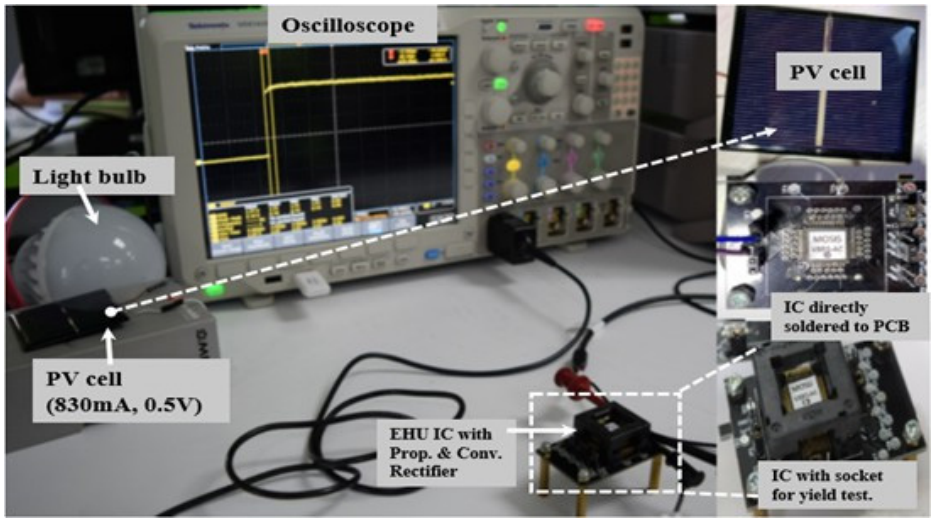


Figure 14. Measurement set-up of the rectifier for the indoor light PV-EHU.

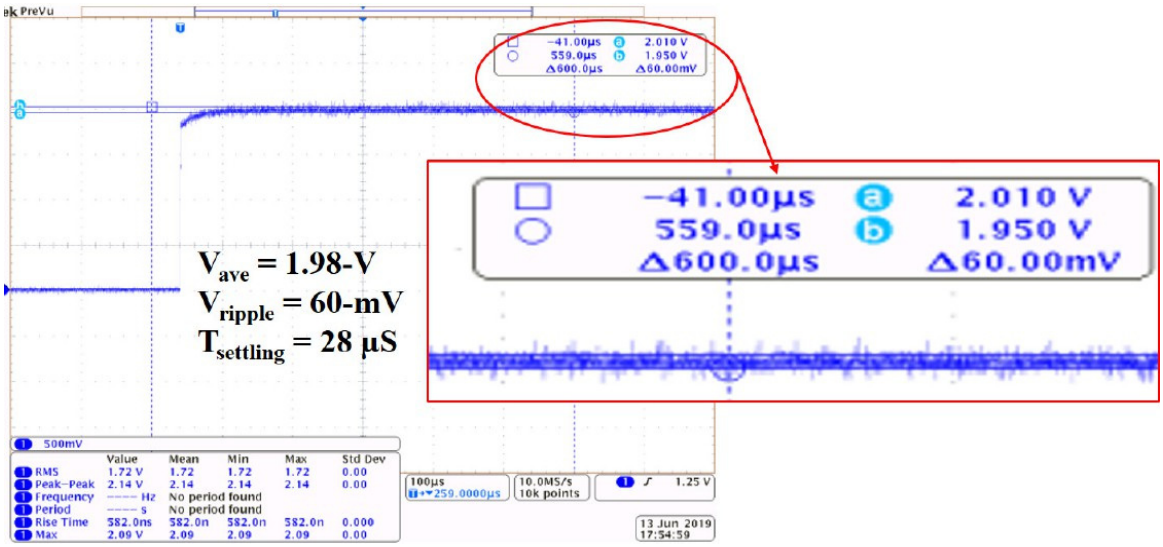


Figure 15. Sample measured ripple voltage snapshot of the proposed indoor light rectifier at 600 Ω. load, *CL* = 5 nF.

Figure 16 shows a snapshot captured from the Teledyne LeCroy oscilloscope by the industry partner, comparing the chip performance of the proposed and conventional rectifiers. The test conditions were set to V_{in} = 0.5 V, R_L = 600 Ω, C_L = 1 nF, and f = 12.5 MHz for the indoor light energy harvesting block. The proposed rectifier achieved an average output voltage of 1.97 V with minimal ripple. Since signal parasitics—including I/O pads, bond pads, bonding wires, and package leads—were modeled in the post-layout simulation, the measured results closely match the simulation. In contrast, the conventional rectifier produced an average voltage of 1.46 V with a 100 mV ripple.

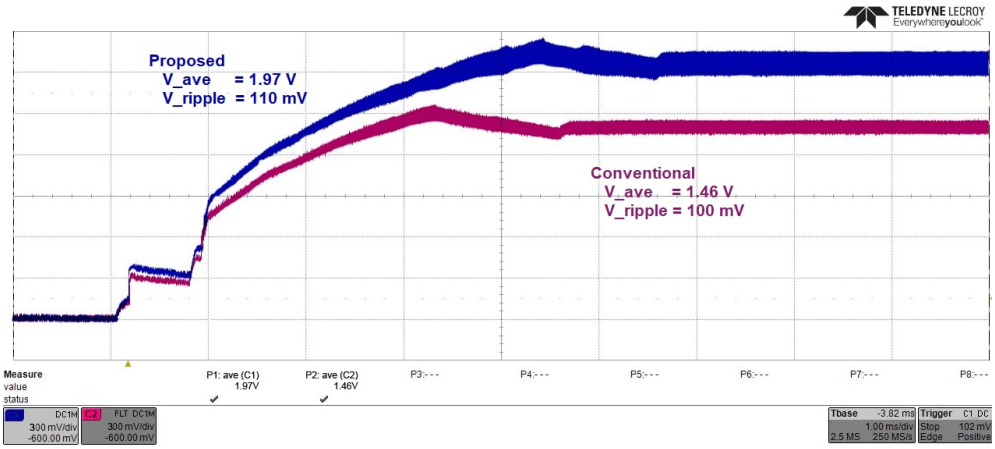
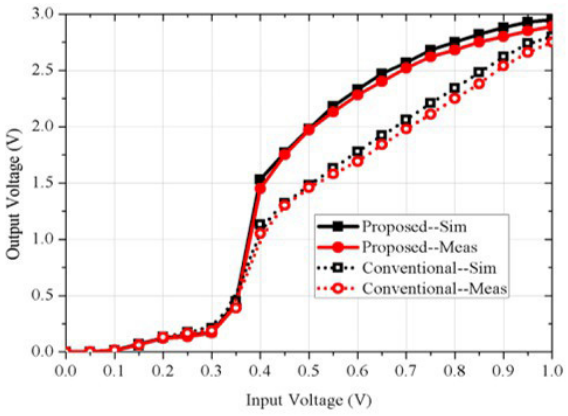


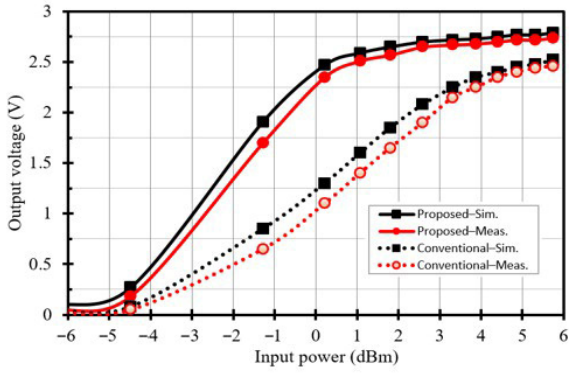
Figure 16. Sample measured snapshot from the instrument of the proposed vs. conventional rectifier at 12.5 MHz indoor light at *V*in = 0.5 V, *RL* = 600 Ω, *CL* = 1 nF, and *f* = 12.5 MHz.

3.2. Measured Versus Simulated Output Waveforms

A comparison of simulated and measured output voltages for the first design is presented in Figure 17a. With the input voltage swept from 0.1 V to 1 V, results indicate that the first design delivers enhanced performance starting from an input threshold of approximately 0.45 V. Figure 17b plots the second design's measured output voltage versus input power, and the data closely match the simulated curve. Across the −2 dBm to 2 dBm input-power range, the second design delivers a higher output voltage than the conventional reference design.



(a)



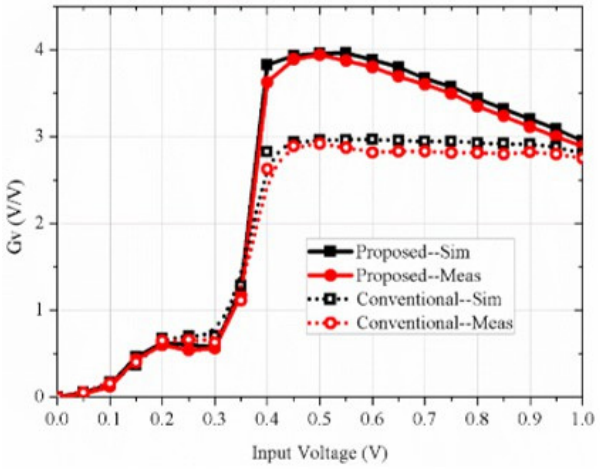
(b)

Figure 17. Measured and simulated output voltage: (**a**) indoor light rectifier with *RL* = 600 Ω and *CL* = 5 nF; (**b**) 2.4 GHz RF rectifier with *RL* = 50 kΩ and *CL* = 5 pF.

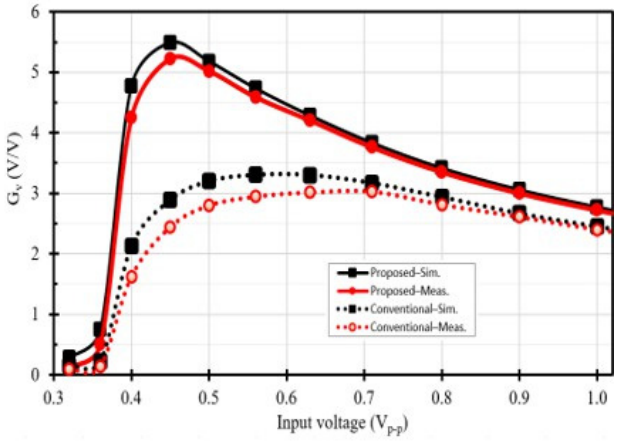
Minor deviations between the measured and simulated values arise from probe and cable insertion losses, RF pad parasitics, and the finite accuracy of the signal generator, vector network analyzer, and digital multimeter used in the bench setup. These measurement-related factors explain the small offsets observed in the indoor light rectifier's results.

3.3. Voltage Conversion Ratio and Power Conversion Efficiency

The calculated VCRs for both designs are presented in Figures 18a and 18b, respectively, alongside those of conventional designs for benchmarking. The first design achieves a VCR of 3.94, compared to 2.92 for the conventional implementation. The second design attains a VCR of 5.02, exceeding the 2.8 measured for the conventional 2.4 GHz RF EH rectifier. For consistency, the input power values were converted from dBm to peak-to-peak voltage.



(a)



(b)

Figure 18. Measured and simulated VCR: (**a**) indoor light rectifier, (**b**) 2.4 GHz RF rectifier.

The measured PCE of the designed rectifiers is presented in Figure 19. It is important to note that different EH applications face distinct design constraints, leading to varying performance targets. Figure 19a plots PCE versus a load resistance sweep spanning 100 Ω to 1 kΩ to determine the optimum operating point for indoor light use. The conventional configuration exhibits a marginally greater maximum PCE compared with the proposed unit. In testing, the new rectifier reaches approximately 58.7% PCE at a 600 Ω load, about 2.1% lower than the reference design. This modest deficit is attributed to the equivalent se-

ries resistance inherent in the cross-coupled capacitors. Even so, the same graph highlights a clear gain in output voltage for the proposed design, confirming its effectiveness.

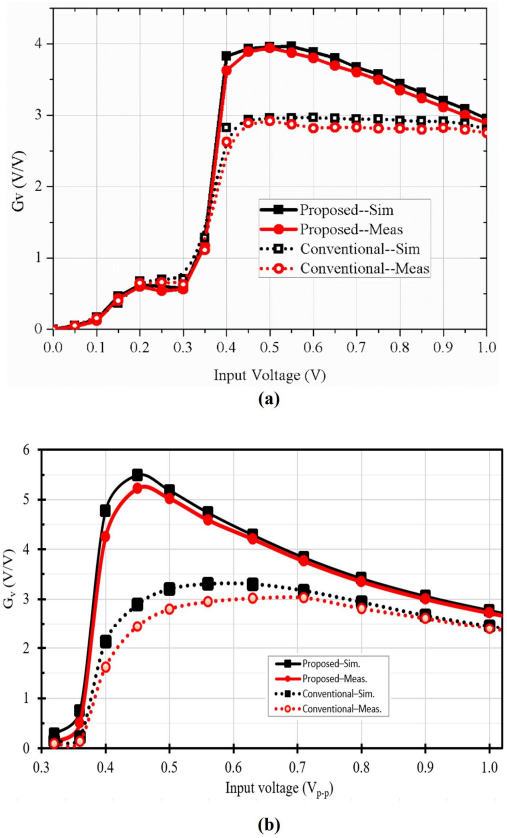


Figure 19. Measured versus simulated PCE and output voltage: (**a**) indoor light rectifier at *V*IN = 0.5 V; (**b**) 2.4 GHz RF rectifier.

Figure 19b shows the 2.4 GHz RF rectifier characterized with a fixed 50 kΩ load while the input power is swept. The peak PCE is 17.5%, around 2.2% below that of the reference circuit; nevertheless, the proposed rectifier delivers a higher output voltage over the entire input-power range.

Across Figures 17–19, the minor discrepancies between the measured and simulated curves can be attributed to typical sources of measurement uncertainty, including probe and cable insertion losses, variation in the RF pad and interconnect parasitics captured during post-layout extraction, and the finite accuracy of the signal generator, vector network analyzer, and digital multimeter used in the laboratory setup. These effects are commonly encountered in CMOS-based rectifier measurements and explain the small offsets observed while confirming the overall consistency between the simulated predictions and the measured chip performance.

3.4. Comparison with Previous Works

Table 2 provides a detailed comparison between the proposed three-stage, capacitor-assisted CCDD rectifier and earlier reported designs. As the table shows, the presented designs achieve improved VCRs for both indoor light and 2.4-GHz RF EH scenarios, despite a slightly lower PCE relative to some state-of-the-art implementations. Notably, the VCR achieved by the second design at 2.4 GHz outperforms those reported in [2–30]. Although the design in [31] reports a higher VCR, it relies on an eight-stage configuration and suffers from a relatively low PCE of just 14%. In contrast, the proposed four-stage rectifier achieves

a VCR exceeding that of [32] while maintaining the same peak efficiency of 17.5%, with a consistent 0.5 V input voltage.

Overall, the proposed capacitor-based CCDD architecture with auxiliary paths enables high output voltage generation while maintaining competitive efficiency, making it well-suited for energy harvesting applications that require both voltage boosting and compact design.

The improved voltage conversion and power efficiency achieved by the proposed rectifier make it a strong candidate for integration in complete energy harvesting systems. To further contextualize its role in practical applications, the following subsection discusses its potential integration with dynamic regulation and energy storage circuits recently explored in the literature.

3.5. Dynamic Regulation and Energy Storage Integration

Dynamic regulation is crucial for maintaining stable energy delivery and improving the long-term reliability of energy harvesting (EH) systems. In practical designs, the rectifier output is connected to a storage component such as a microbattery, supercapacitor, or thin-film capacitor together with a power-management circuit that regulates charging and discharging under variable input conditions. These regulation stages help balance harvested energy, mitigate transient voltage drops, and support the continuous operation of wireless sensor nodes.

Recent work emphasizes dynamically controlled storage and regulation mechanisms for sustainable EH systems. For example, Ref. [33] proposed a dynamically synergistic regulation method for rotation-based energy harvesters and achieved improved output stability through real-time impedance adaptation. In a related contribution, Ref. [34] reviewed intelligent mechanical energy harvesting frameworks that integrate adaptive control to optimize energy flow and enhance storage utilization. At the network level, Ref. [35] showed that distributed real-time regulation strategies for shared energy storage systems can improve voltage balance and frequency regulation in renewable-powered settings.

Table 2. Performance summary and comparison with previous works.

Reference	Circuit Techniques	Operating Frequency	Input Amplitude (V)	Output Voltage (V)	No. of Stages	VCR (*V*/*V*)	Peak PCE (%)	Load Current *RL*, *I*LOAD	CMOS Tech. (µm)
DESIGN 1 [InLight EH] This work	Auxiliary MOS and Capacitor	12.5 MHz	0.5	1.97	3	3.94	58.7	2–8 mA	0.065
[23] Conventional, 2009 °	Conventional	12.5 MHz	0.5	1.46	3	2.92	60.8	2–8 mA	0.065
[17] Chong, 2019 *[a]	CCDM *[a] Shared-capacitor coupling (ICC) *[a]	12.5 MHz	0.5	1.65	3	3.30	[b]	2–8 mA	0.065
[25] Grasso, 2019 *[a]	Body-voltage control scheme *[a]	12.5 MHz	0.5	1.55	3	3.10	[b]	2–8 mA	0.065
[36] Haddad, 2016	Greinacher ULP Diode	13.56 MHz	0.5	1.90	3	3.80	72	0.01 mA	0.25
[30] Guler, 2019	Reconfigurable VM	13.56 MHz	2.4 †	4.92 †	3	2.05	76	2 kΩ	0.35
DESIGN 2 [RF EH] This work	Auxiliary MOS and Capacitor	2.4 GHz	0.5 ‡	2.51	3	5.02	17.5	50 kΩ	0.065
[23] Conventional, 2009 °	Conventional	2.4 GHz	0.5 ‡	1.39	3	2.80	19.7	50 kΩ	0.065
[17] Chong, 2019 *[a]	CCDM *[a] Shared-capacitor coupling (ICC) *[a]	2.4 GHz	0.5 ‡	2.20	3	4.44	[b]	50 kΩ	0.065
[25] Grasso, 2019 *[a]	Body-voltage control scheme *[a]	2.4 GHz	0.5 ‡	2.05	3	4.10	[b]	50 kΩ	0.065
[16] Moghaddam, 2017	CCDM with Lower	2 GHz	0.5 ‡	2.48 †	3	4.96	25 †	50 kΩ	0.13

Table 2. *Cont.*

Reference	Circuit Techniques	Operating Frequency	Input Amplitude (V)	Output Voltage (V)	No. of Stages	VCR (*V*/*V*)	Peak PCE (%)	Load Current *RL*, *ILOAD*	CMOS Tech. (µm)
[31] Lau, 2017	DC Feeding (LDCF)	2 GHz	2.0 ‡	3.5 †	2	1.75	65 †	10 kΩ	0.065
	CCDM with DC-boosted gate bias	2.45 GHz	0.5 ‡	1.35 †		2.7	48 †	5 kΩ	
[20] Lo, 2017	CCDM with HP Path (LVTGP, LVTL_P)	2.45 GHz	0.159 ‡	1.04 †	5	6.54	59.6	29 kΩ	0.065
		900 MHz	0.1 ‡	1.0 †		10.0	36.5	147 kΩ	
[32] Abouzied, 2017	Reconfigurable Greinacher doubler with LC matching	900 MHz	0.45 ‡	2.5 †	2	5.55	26	1 MΩ/PMU	0.18
		915 MHz	0.5 ‡	2.35 †		4.7			
		915 MHz	0.079 ‡	1.0 †	4	4.7	17.5 †		
		915 MHz	0.079 ‡	1.0 †	8	12.66	14 †		

° Measurement results were redesigned/reproduced in this work to operate at 12.5 MHz, 2.4 GHz. *[a] Simulation results are redesigned/reproduced in this work to operate at 12.5 MHz, 2.4 GHz; −2 dBm input ≈ 0.5 $V_{p\text{-}p}$. [b] Simulation result not taken; † data extrapolated/estimated from graph; ‡ data P_{in} (dBm) sensitivity converted to $V_{p\text{-}p}$.

Integrating the proposed capacitor-boosted CCDD rectifier with similar dynamic regulation circuits can further stabilize its DC output, especially under fluctuating illumination or RF conditions. This integration enables efficient hybrid energy harvesting and storage, making the architecture suitable for autonomous and self-sustaining Internet-of-Things (IoT) and wireless sensor network (WSN) nodes that require reliable energy availability even when sources are intermittent.

4. Conclusions

This paper presents novel circuit design techniques for CMOS-based rectifiers that significantly enhance both VCR and PCE. Utilizing these methods, two rectifiers were designed and fabricated using 65 nm CMOS technology. The first design operates at 12.5 MHz, while the second targets 2.4 GHz applications. To validate the proposed techniques, a theoretical analysis was conducted, and a three-stage, capacitor-based, cross-coupled, differential-driven (CCDD) architecture was employed for both designs. Compared to existing state-of-the-art solutions, the proposed rectifiers demonstrate notable improvement. Under a load of 600 Ω, the first rectifier achieves a peak VCR close to 4 and a measured PCE of approximately 58.7%. Moreover, it can deliver more than 2 mA of current, which is sufficient for quickly charging external energy storage components such as batteries or supercapacitors. In the second design, targeting RF energy harvesting, the VCR exceeds 5 with a PCE of 17.5% under a load of 50 kΩ. Although the output current is limited to 70 µA, it remains suitable for typical RF EH scenarios. Overall, the experimental results confirm that the proposed design strategies are highly effective for developing efficient CMOS-based rectifiers. The resulting rectifiers offer a cost-effective power source for battery-less wireless sensors and other emerging energy-autonomous devices.

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Conflicts of Interest: The authors declare no conflicts of interest.

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