

## A Novel High Linearity and Low Power Folded CMOS LNA for UWB Receivers

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This paper presents a high linearity and low power Low-Noise Amplifier (LNA) for Ultra-Wideband (UWB) receivers based on CHRT 0.18 $\mu$ m CMOS technology. In this work, the folded topology is adopted in order to reduce the supply voltage and power consumption. Moreover, a band-pass LC filter is embedded in the folded-cascode circuit to extend bandwidth. The transconductance nonlinearity has a great impact on the whole LNA linearity performance under a low supply voltage. A post-distortion (PD) technique employing an auxiliary transistor is applied in the transconductance stage to improve the linearity. The post-layout simulation results indicate that the proposed LNA achieves a maximum power gain of 12.8dB. The input and output reflection coefficients both are lower than -10.0dB over 2.5~11.5GHz. The input third-order intercept point (IIP3) is 5.6dBm at 8GHz and the noise figure (NF) is lower than 4.0dB. The LNA consumes 5.4mW power under a 1V supply voltage.

*Keywords:* CMOS integrated circuits; UWB; LNA; post-distortion; high linearity; third-order distortion.

### 1. Introduction

Due to the rapid growth of wireless communications technologies, many wireless communication standards, such as Global System for Mobile Communications (GSM), Wideband Code Division Multiple Access (WCDMA), Long Term Evolution (LTE), Bluetooth and 802.11a/b/g/n, have been developed. To accommodate such broad range of services, multi-standard broadband radio receivers have drawn great attention. The Low-Noise Amplifier (LNA) is usually the first on-chip active stage after antenna in almost all

radio frequency (RF) and microwave receivers. As a critical module, LNAs in such receivers need to work for different standards and applications. An Ultra-Wideband (UWB) LNA which can be shared among different standards is preferred to save cost and reduce complexity. Such a LNA must provide good impedance matching, high linearity, low NF, and adequate gain across multi-GHz frequency band.<sup>1</sup> For applications in mobile communication systems, low-voltage, low power and stability requirements are also important for LNA design. Stability is an important indicator to ensure the designed amplifier working properly. In terms of the reflection coefficient, the designed circuit system is stable only the modular of the reflection coefficient is less than one. If the value more than one, it makes reflected voltage larger than incident voltage, the whole system will oscillate because of positive feedback.<sup>2</sup>

Up to now, several topologies have been proposed for UWB LNAs. The distributed amplifier (DA),<sup>3, 4</sup> which absorbs the parasitic capacitance of the input transistor as part of the transmission line, can provide good operating performance over a wide range of frequency. However, the large area makes it less attractive to low cost applications and its relatively high power consumption is a limit to ultra-low power design. The shunt-feedback amplifier,<sup>5, 6</sup> which is a well-known topology used in wideband amplifiers, can provide broadband matching and flat gain over the entire bandwidth. Nevertheless, it is difficult to satisfy gain and noise performance simultaneously. The passive filtering configuration<sup>7</sup> is a good solution to extend bandwidth of amplifier. Inserting the Chebyshev filter in the input matching network can provide good wideband matching and high power gain.<sup>8</sup> However, the NF is degraded by the insertion loss of the filter. Meanwhile, the large number of passive components will occupy a considerable chip area which will increase cost and size. The common-gate (CG) amplifier<sup>9</sup> is popular in broadband LNA design for its excellent performance of wideband input matching and high linearity.

The linearity is of great importance for the UWB LNA design. It should be high enough to suppress interference and maintain high sensitivity. In a multi-standard wideband receiver, a wide range of out-band/in-band interferers may corrupt the signal, resulting in severe blocking, cross-modulation and inter-modulation, which pose a huge challenge to the linearity of the LNA. As the Complementary Metal Oxide Semiconductor (CMOS) technology scales down and supply voltage decreases, it is more difficult to obtain high linearity with a low supply voltage, since the nonlinear output conductance, short-channel and high-field mobility, which are ignored under a high supply voltage, become very important under low-voltage operation. The optimal biasing technique was proposed in Refs. 10, in which the third-order derivative of DC transfer characteristic was adjusted to zero by regulating the biasing voltage  $V_{GS}$ . However, the bias voltage range for IIP3 peak is very narrow, making the linearity boosting very sensitive to the biasing voltage. The derivative superposition (DS) method is based on multiple-gated configuration, which adds the second/third-order derivatives from the main and auxiliary transistors to cancel distortion. It involves MOS transistors working in triode<sup>11</sup> or weak inversion region,<sup>12, 13</sup> therefore the DS method will find difficult

to match the transistors working in different regions, resulting in a linearity improvement highly sensitive to process-voltage-temperature (PVT) variations. The post-distortion (PD) technique<sup>14, 15</sup> is utilized to improve the linearity. Since all transistors are biased in the saturation region and some of them also avoid the input matching degradation, this technique has a robust increase of linearity.

In this paper, a high linearity, low power UWB LNA is introduced and a band-pass LC filter is used to extend bandwidth. The LNA adopts a CG structure of folded topology to provide input matching. In addition, to reduce the drain conductance nonlinearity, the PD technique is applied in the LC folded-cascode configuration. As a result, the UWB LNA has excellent performance even under an extremely low supply voltage.

## 2. Theoretical Analysis of Linearity Improvement

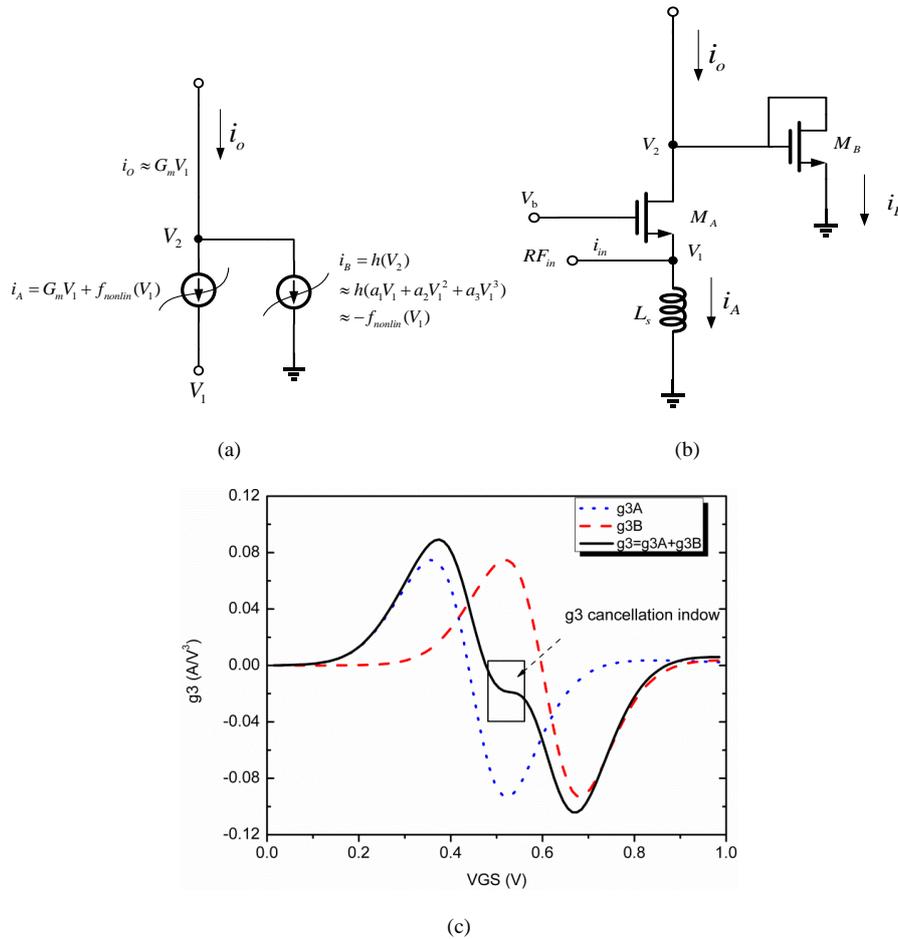


Fig. 1. The post-distortion technique: (a) Concept of the technique; (b) Circuit implementation; (c) Third-order power series coefficient of  $i_o$  at DC.

The drain current of a common-source (CS) Field Effect Transistor (FET) can be expressed in terms of gate–source voltage  $V_{gs}$  using the power series expansion:

$$i_d = g_1 v_{gs} + g_2 v_{gs}^2 + g_3 v_{gs}^3 \quad (1)$$

where  $g_i$  is the  $i$ th-order coefficient of transconductance. The nonlinear current generated in the CS FET is fully transferred to the next stage. If the drain node of the CS FET has an additional current path which selectively absorbs the third-order intermodulation distortion (IMD3) current component, then only the fundamental current component delivers to the next stage. A better linearity can thus be achieved. Here, the PD technique is utilized to design the proposed LNA circuit.

Figure 1(a) shows the PD technique which utilizes an auxiliary transistor ( $M_B$ )'s nonlinearity to cancel that of the main device ( $M_A$ ). Both  $M_B$  and  $M_A$  operate in the saturation region with the same polarity. The transistor  $M_B$  taps voltage  $V_2$  and replicates the nonlinear drain current of the main transistor  $M_A$ , partially canceling second-order/third-order distortion terms in Figs. 1(b)-1(c). The drain currents of  $M_A$  and  $M_B$  can be modeled as Eq. (2) and Eq. (3):

$$i_A = g_{1A} V_1 + \underbrace{g_{2A} V_1^2 + g_{3A} V_1^3}_{f_{nonlin}(V_1)} \quad (2)$$

$$i_B = g_{1B} V_2 + g_{2B} V_2^2 + g_{3B} V_2^3 \quad (3)$$

where  $V_1$ , and  $V_2$  are the source and drain voltages of  $M_A$ , respectively. Suppose  $V_2$  is related to  $V_1$  by:

$$V_2 = -c_1 V_1 - c_2 V_1^2 - c_3 V_1^3 \quad (4)$$

The currents have to satisfy the Kirchhoff's Current Law (KCL), yielding the output current  $i_o$ :

$$\begin{aligned} i_o &= i_A + i_B \\ &= g_{pm1} V_1 + \underbrace{g_{pm2} V_1^2}_{\text{second-order distortion}} + \underbrace{g_{pm3} V_1^3}_{\text{third-order distortion}} \end{aligned} \quad (5)$$

where

$$g_{pm1} = g_{1A} - c_1 g_{1B} \quad (6)$$

$$g_{pm2} = g_{2A} - c_1^2 g_{2B} - c_2 g_{1B} \quad (7)$$

$$g_{pm3} = g_{3A} - c_1^3 g_{3B} - g_{1B} c_3 - 2g_{2B} c_1 c_2 \quad (8)$$

The gate-to-source voltage  $V_{gs}$  and the output drain current  $i_o$  can be expressed in terms of  $i_{in}$  using Volterra series expansion as below:

$$v_{gs}(j\omega) = A_1(j\omega) \circ i_{in} + A_2(j\omega_1, j\omega_2) \circ i_{in}^2 + A_3(j\omega_1, j\omega_2, j\omega_3) \circ i_{in}^3 \quad (9)$$

$$i_o(j\omega) = B_1(j\omega) \circ i_{in} + B_2(j\omega_1, j\omega_2) \circ i_{in}^2 + B_3(j\omega_1, j\omega_2, j\omega_3) \circ i_{in}^3 \quad (10)$$

where “ $\circ$ ” is the Volterra series operator<sup>16</sup>. and for the coefficients  $A_1, A_2, A_3, B_1, B_2$ , and  $B_3$ , the reader can refer to the original paper.<sup>17</sup>  $B_n$  can be calculated from Eqs. (5), (9), and (10) as follows:

$$B_1(j\omega) = g_{pm1}A_1(j\omega) \quad (11)$$

$$B_2(j\omega_1, j\omega_2) = g_{pm1}A_2(j\omega_1, j\omega_2) + g_{pm2}A_1(j\omega_1)A_1(j\omega_2) \quad (12)$$

$$B_3(j\omega_1, j\omega_2, j\omega_3) = g_{pm1}A_3(j\omega_1, j\omega_2, j\omega_3) + 2g_{pm2}\overline{A_1(j\omega_1)A_2(j\omega_1, j\omega_2)} + g_{pm3}A_1(j\omega_1)A_1(j\omega_2)A_1(j\omega_3) \quad (13)$$

where

$$\overline{A_1(j\omega_1)A_2(j\omega_1, j\omega_2)} = \frac{1}{3}(A_1(j\omega_1)A_2(j\omega_2, j\omega_3) + A_1(j\omega_2)A_2(j\omega_1, j\omega_3) + A_1(j\omega_3)A_2(j\omega_1, j\omega_2)) \quad (14)$$

To calculate the two-tone third-order intermodulation distortion (AIP3), a two-tone excitement ( $\omega_a, \omega_b$ ) is applied to the input. The two-tone excitement and IIP3 equations are given by:<sup>8, 18</sup>

$$AIP3(2\omega_b - \omega_a) = \sqrt{\frac{4}{3} \left| \frac{B_1(j\omega_b)}{B_3(j\omega_b, j\omega_b, -j\omega_a)} \right|} \quad (15)$$

$$IIP3(2\omega_b - \omega_a) = \frac{AIP3(2\omega_b - \omega_a)^2}{8} \times R_e \quad (16)$$

From Eqs. (11), (15), and (16), we can derive IIP3 by Volterra series analysis as:

$$IIP3(2\omega_b - \omega_a) = \frac{1}{6R_e} \cdot \frac{1}{\{Z_s(\omega)\} \cdot |H(\omega)| \cdot |A_1(\omega)|^3 \cdot |\mathcal{E}(\Delta\omega, 2\omega)|} \quad (17)$$

$$\mathcal{E}(\Delta\omega, 2\omega) = g_{pm3} - g_{oB} \quad (18)$$

$$Z_s(\omega) = \frac{j\omega/C_{gs1}}{-\omega^2 + j\omega \frac{g_{pm1}}{C_{gs1}} + \frac{1}{L_s C_{gs1}}} \quad (19)$$

where

$$g_{oB} = \frac{2}{3}(g_{pm2})^2 \left\{ \frac{2}{g_{pm1} + A_1(\Delta\omega)} + \frac{1}{g_{pm1} + A_1(2\omega)} \right\} \quad (20)$$

where

$$\Delta(\omega) = \omega_b - \omega_a, \omega \approx \omega_a \approx \omega_b \quad (21)$$

IIP3 is primarily affected by  $\mathcal{E}(\Delta\omega, 2\omega)$ . Equations (17)-(20) implies that the linearity can indeed be improved by reducing  $g_{pm3}$ . On the other hand, increasing  $g_{pm2}$  can increase  $g_{oB}$  and this can further decrease  $\mathcal{E}(\Delta\omega, 2\omega)$ . The post-distortion technique employs an additional folded diode to minimize  $g_{pm3}$ . To obtain a good linearity, the coefficient of the third term in Eq. (5) should be close to zero, by adjusting the gate bias and size of MA and MB.

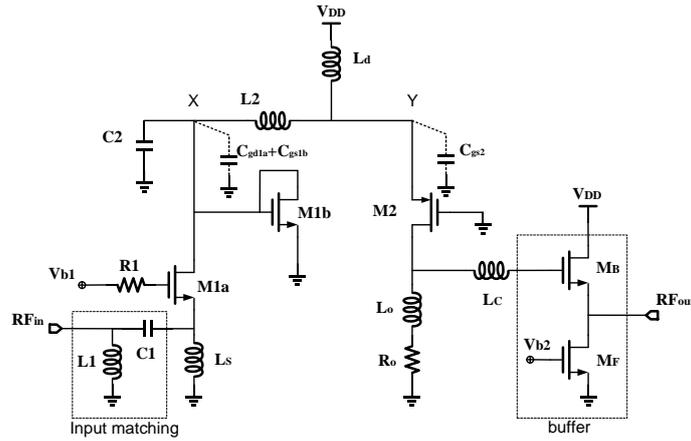


Fig. 2. The complete schematic of the proposed UWB LNA.

To achieve low power operation, the folded structure is a good choice since the transistors are placed in parallel between the supply DC voltage and GND and thus a large voltage can be avoided. Besides, good reverse isolation and stability in low power situation make this configuration more competitive especially in ultra-low power LNA design. Fig. 2 shows the complete circuit schematic of the proposed LNA which is composed of two gain stages. Taking advantage of the superior performance in broadband input matching, linearity, stability, and robustness to PVT variations, common-gate (M1a) structure is utilized as the input stage. Transistor M2 is the main

transistor and M1b is the auxiliary transistor as a post-distortion circuit. All body-terminals of the NMOS transistors are connected to GND in this LNA.

### 3. Circuit Design and Analysis

The design of LNA is based on the CHRT 0.18 $\mu$ m RF CMOS technology and all components are integrated. To take advantage of CG topology and folded structure as mentioned above, a folded CG broadband LNA is proposed. Fig. 2 shows a simplified circuit schematic of the folded cascode LNA where M1a and M2 represent the first and second gain stages, respectively. In the circuit implementation, the impedance matching at the input terminal is achieved by L1, C1 and Ls, while the Lc, Lo and Ro are adopted for output matching. As the inductor Ld resonates with capacitor C2 and inter-stage parasitic capacitor at the frequencies of interest, the bias current for M1a, M1b and M2 is provided without introducing excessive load to the gain stage. In conventional folded topology with RF choke inductor, Ld only ensures to deliver the RF signal current to the output terminal just within the narrow bandwidth of operation frequency.<sup>9</sup> It is because the high impedance seen from the LC network is achieved around the resonant frequency of Ld and parasitic capacitor at the drain of M1a and source of M2/M1b. To improve the input wideband characteristic of CG M1a, the series inductor L2 is inserted at node X to broaden the bandwidth. The post-distortion technique is implemented at the first stage, reducing its influence on noise and IMD3.

#### 3.1. Wideband Matching

##### 3.1.1. Input Matching

Since the body-terminal of the NMOS transistor is connected to GND, the body effects and its parasitic capacitances are ignored in equation. For small signal analysis, the proposed LNA is treated as a two stage amplifier, and its simplified circuit model is illustrated in Fig. 3. From the equivalent circuit, the input impedance can be written as:

$$Z_{in} = \frac{1}{\frac{1}{Z_s(\omega)} + \frac{1 - g_{m1a}Z_{o1a}(\omega)}{R_{o1} + Z_{o1a}(\omega)}} \approx \frac{1}{g_{pm1}} = \frac{1}{g_{m1a} - c_1 g_{m1b}} \quad (22)$$

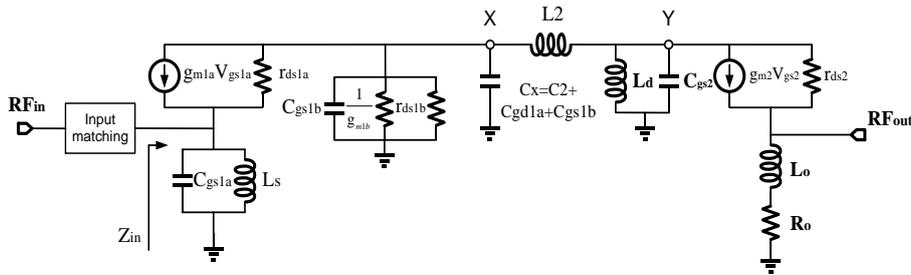


Fig. 3. Small signal model of the UWB LNA.

The input impedance approximates  $1/g_{pm1}$  over the frequency band of interest. Due to the effect of other terms,  $g_{m1a}$  should be set slightly greater than 32mS. Through simulations, we have observed that the good input matching can be obtained when  $g_{m1a}$  approaches to 34 mS.

### 3.1.2. Bandwidth Extension Technique

The LC  $\pi$ -network between X and Y can be redrawn as shown in Fig. 4(a). The  $\pi$ -network can be decomposed into two parts. The first part is constituted by L2 and  $C_X$  as a lowpass filter (LPF) with a high cut-off frequency ( $\omega_L$ ). The second part is formed by Ld and  $C_{gs2}$  as a narrow bandpass filter (BPF) with a lower peaking frequency ( $\omega_B$ ). As seen from Fig. 4(a), the cascade of 2<sup>nd</sup>-order LPFs and 2<sup>nd</sup>-order BPFs, between node X and Y is a fourth-order doubly terminated bandpass filter.

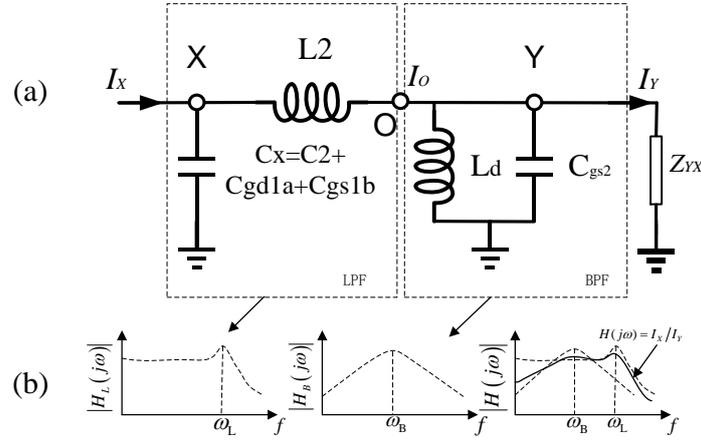


Fig. 4. The bandwidth extension circuit of the LC network between node X and Y.

From Fig. 4(b), we can write the transfer function  $T_1(s) = I_O/I_X$  of 2<sup>nd</sup>-order LPFs and  $T_2(s) = I_Y/I_O$  of 2<sup>nd</sup>-order BPFs equations as:

$$T_1(s) = \frac{I_O}{I_X} = \frac{k_L \omega_L^2}{s^2 + \frac{\omega_L}{Q_L} s + \omega_L^2} = \frac{\frac{1}{C_X L_2}}{s^2 + \frac{Z_{OX}}{L_2} s + \frac{1}{C_X L_2}} \quad (23)$$

$$T_2(s) = \frac{I_Y}{I_O} = \frac{k_B (\omega_B / Q_B) s}{s^2 + \frac{\omega_B}{Q_B} s + \omega_B^2} = \frac{\frac{1}{Z_{YX} C_{gs2}} s}{s^2 + \frac{1}{Z_{YX} C_{gs2}} s + \frac{1}{C_{gs2} L_d}} \quad (24)$$

where the  $Z_{OX}$  denotes impedance seen at O point into the BPF filter. And  $Q_B$  and  $Q_L$  are the pole quality factor of BPF and LPF, respectively. From Eqs. (23) and (24), the closed-form formulas of  $\omega_B$ ,  $\omega_L$ ,  $Q_B$ , and  $Q_L$  can be obtained as Eq. (25):

$$\omega_L = \sqrt{\frac{1}{C_X L_2}}, \quad Q_L = \frac{1}{Z_{OX}} \sqrt{\frac{L_2}{C_X}}, \quad \omega_B = \sqrt{\frac{1}{C_{gs2} L_d}}, \quad Q_B = Z_{YX} \sqrt{\frac{C_{gs2}}{L_d}} \quad (25)$$

From Fig. 4(a), it is clear that the circuit between node X to Y can be seen a cascade connection of 2<sup>nd</sup>-order LPF and BPF. The transfer function from node X to Y ( $H(j\omega) = I_Y/I_X$ ) is derived as follows:

$$\begin{aligned} H(s) = \frac{I_Y}{I_X} &= H_L \cdot H_B = \frac{k_L \omega_L^2}{s^2 + s \frac{\omega_L}{Q_L} + \omega_L^2} \cdot \frac{k_B (\omega_B / Q_B) s}{s^2 + s \frac{\omega_B}{Q_B} + \omega_B^2} \\ &= \frac{\frac{L_d}{Z_{YX}} s}{C_X C_{gs2} L_2 L_d s^4 + \left( \frac{1}{Z_{YX}} C_X L_2 L_d + Z_{OX} C_X C_{gs2} L_d \right) s^3 + \left( \frac{Z_{OX}}{Z_{YX}} C_X L_d + C_X L_2 + C_{gs2} L_d \right) s^2 + \left( \frac{L_d}{Z_{YX}} + Z_{OX} C_X \right) s + 1} \end{aligned} \quad (26)$$

It is clear that Eq. (26) denotes transfer function of 4<sup>th</sup>-order BPF. Fig. 4(b) denotes the ADS simulation of frequency response of 2<sup>nd</sup>-order LPF, 2<sup>nd</sup>-order BPF and their cascade circuit. In the right-side figure of Fig. 4(b), two dotted lines denotes frequency responses of 2<sup>nd</sup>-order LPF, 2<sup>nd</sup>-order BPF, and the solid line denote frequency responses of circuit between node X and Y in Fig. 4(a). It can be seen that frequency bandwidth of circuit between node X and Y became extension. Qualitatively, Input current signal  $I_X$  below this cut-off frequency will be delivered to the output at node Y as  $I_Y$ . The resultant transfer function is a broadband 4<sup>th</sup>-order BPF characteristic as illustrated in Fig. 4(b). Then the wideband output matching is achieved. Taking M1b into account, the reactive resistance decreases and the capacitive reactance increases, due to M1b being placed in parallel with the load of M1a. Therefore we should slightly adjust the values of C2 and L2 to acquire a new wideband output matching. In this paper we use C2 = 0.05pF and L2 = 6.5nH.

### 3.2. Gain Analysis

Since the body-terminal of the NMOS transistor is connected to GND, the body effects and parasitic capacitances are not considered in equation. The voltage transfer function of the first stage can be expressed as:

$$A_1 = \frac{v_{o1}}{v_{in}} = \frac{(g_{pm1} r_{ds1a} + 1)(Z_{d1} // \frac{1}{sC_X})}{(R_s // Z_{s1})(g_{pm1} r_{ds1a} + 1) + (Z_{d1} // \frac{1}{sC_X}) + r_{ds1a}} \quad (27)$$

$$Z_{d1} = Z_{in2} // (R_{d1} + sL_2) + sL_2 \quad (28)$$

$$Z_{s1} = sL_s + 1/sC_{gs1a} \quad (29)$$

$$R_{d1} = r_{ds1b} + 1/g_{mb} \quad (30)$$

The voltage gain of the second stage is given by:

$$A_2 = \frac{v_o}{v_{in2}} = \frac{-g_{m2} + sC_{gd2}}{\frac{1}{r_{ds2} // Z_{d2}} + sC_{gd2}} \quad (31)$$

$$Z_{d2} = (R_o + sL_o) // Z_{buf} \quad (32)$$

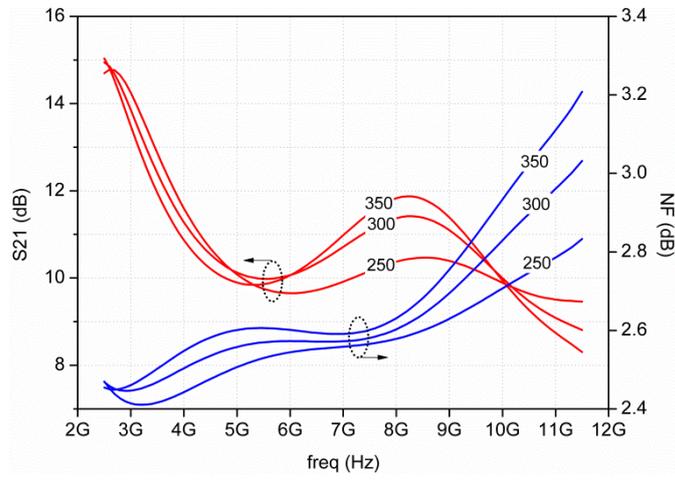


Fig. 5. Simulated gain and NF characteristics with output resistance of 250Ω, 300Ω and 350Ω.

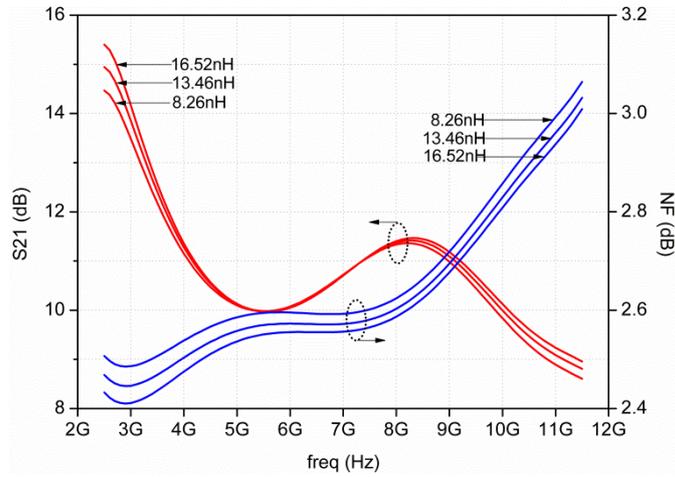


Fig. 6. Simulated gain and NF characteristics with inductance  $L_o$  of 8.26nH, 13.46nH and 16.52nH.

The gain increases with the increase of  $R_o$ , but too large  $R_o$  will worsen output matching. Inductor  $L_2$  improves gain at high frequency resonating with parasitic capacitor at the drain node of M1a. A small capacitor  $C_2$  improves the gain flatness. The addition of M1b decreases the gain slightly, due to the presence of the small  $R_{d1}$ . However, we can increase  $g_{m2}$  and decrease  $g_{m1b}$  to compensate for the degradation of gain. Simulated gain and NF characteristics with different output resistances are shown in Fig. 5. In Fig. 5, the variation of transfer characteristics is demonstrated when the values of output resistances  $R_o$  are equal to 250 $\Omega$ , 300 $\Omega$  and 350 $\Omega$ . The gain and NF variations with resistance variation of  $\pm 16.7\%$  are less than 1dB and 0.5dB, respectively. In addition, inductance  $L_o$  will affect output matching in the way of extending the bandwidth. Simulation results in Fig. 6 show that the gain variation is less than 0.2dB. Meanwhile, noise figure degradation is less than 0.5dB with inductance variation. In this paper,  $R_o = 300\Omega$  and  $L_o = 13.46\text{nH}$ .

### 3.3. Noise Analysis

The noise figure of the first stage is critical to the whole circuit, especially when the CG amplifier owns an effective power gain. The channel noise and gate-induced noise of M1b appearing at the LNA output is

$$\overline{i_{nd,M1b}^2} = 4kT \frac{\gamma}{\alpha} g_{m1b} \quad (33)$$

$$\overline{i_{ng,M1b}^2} = 4kT \frac{\delta\alpha\omega^2 C_{gs1b}^2}{5} \cdot \frac{g_{m1b}}{(g_{m1b} + g_{m2})^2} \quad (34)$$

The noise contribution from M1b is proportional to its transconductance, which is much smaller than  $g_{m1a}$ . The noise factor of the proposed linearized cascode CG-LNA can be calculated as follows:

$$F \approx 1 + \frac{\gamma}{\alpha} \frac{1}{g_{m1a} R_s} + \frac{\delta\alpha}{5g_{m1a} R_s} \left(\frac{\omega}{\omega_T}\right)^2 + \frac{R_{d1}}{(\omega^2 L_d^2 + R_{d1}^2) R_s g_{m1a} \left(\frac{Z_{in}(s)}{Z_{in}(s) + R_s}\right)^2} \quad (35)$$

$$+ \frac{\gamma}{\alpha} \frac{1}{g_{m1a} R_s} \cdot \frac{g_{m1b}}{g_{m1a}} + \frac{\delta\alpha}{5g_{m1a} R_s} \left(\frac{\omega}{\omega_T}\right)^2 \cdot \frac{g_{m1b}}{g_{m1a}} \cdot \frac{g_{m1b}^2}{(g_{m1b} + g_2)^2}$$

where  $\gamma$ ,  $\alpha$ ,  $\delta$  are process dependent parameters,<sup>18</sup> and  $Z_{in}(s)$  is derived in Eq. (22). In Eq. (35), the last two terms are the additional noise contribution from the linearization circuit. The 5<sup>th</sup> and 6<sup>th</sup> terms are the channel noise of M1b, which is smaller than the channel noise of M1a by a factor of  $g_{m1b}/g_{m1a}$  (0.27 in our design). To properly choose the size of M1a and M1b transistors, the optimum size of M1a and M1b are already set to allow the aforementioned noise and PD to take effect. Adding the auxiliary transistor M1b together with the main transistor M1a allows the equivalent  $g_m$  to reshape the LNA IIP3

drastically as can be seen in Fig. 7. Comparing Eq. (17) with Eq. (35), in the PD technique, the value of  $g_{m1b}/g_{m1a}$  in IIP3 and noise figure is different from that in  $g_m$  reduction by Eq. (18). Thus, the degradation in NF is slightly less than 0.4dB over the entire bandwidth. The PD technique does not affect the NF appreciably based on the above discussion. In this paper,  $g_{m1b}=8.7\text{mS}$  and  $g_{m2}=12.4\text{mS}$ .

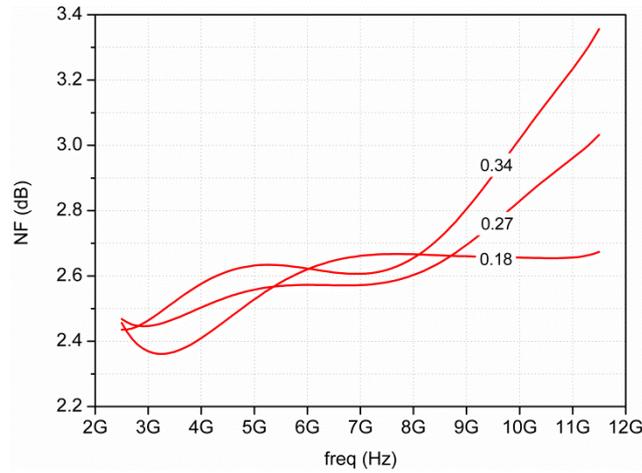


Fig. 7. NF versus  $g_{m1b}/g_{m1a}$  of 0.18, 0.27 and 0.34.

### 3.4. Process and Temperature Variations

To investigate the temperature sensitivity of the PD linearization technique, IIP3 simulations were conducted at three corners including fast process ( $-25^\circ\text{C}$ , corner 1), typical process ( $65^\circ\text{C}$ , corner 2) and slow process ( $100^\circ\text{C}$ , corner 3). In all cases, IIP3 tests are made in 100MHz tone spacing and  $\text{Pin}=-20\text{dBm}$ . The 4.5GHz, 8GHz and 10.5GHz in Table 1 are treated as the intermodulation frequencies. At the same frequency and the different process corners, IIP3 varies because  $g_{m1a}(T)$  and  $g_{m1b}(T)$  changes with temperature  $T$ . At the same process corner and the different frequencies, IIP3 also varies but this is due to the different characteristics and matching of MOSFETs.

Table 1. Simulation results of the proposed UWB LNA for three corners.

Linearity	Inter-modulation freq.	Corner 1	Corner 2	Corner 3
	4.5GHz	1.0	-2.1	-4.2
IIP3(dBm)	8GHz	6.6	6.2	4.4
	10.5GHz	2.7	-1.6	-3.0

### 3.5. Monte Carlo Simulation

The Monte Carlo simulations were performed to check the stability against the process and temperature variations and the mismatch of MOSFETs. To check the effect of process variation and the mismatch of MOSFETs, pre-layout simulation was conducted with a  $\pm 20\%$  variation in the sizes of M1a, M1b and M2 and for the typical process and 65°C corner. All parameters were simulated at 8GHz with two hundred simulation results.

Figure 8 shows the Monte Carlo simulation for S21. The mean value of 11.17dB and the standard deviation of around 0.02 are obtained. So S21 does not vary drastically with the mismatch. The simulation result of IIP3 is presented in Fig. 9, which indicates a center-oriented graph. IIP3 can decrease to 3.5dBm which is 2.5dB below the mean value. Considering that the initial simulation value of IIP3 is 6.2dBm for the typical process (corner 2), IIP3 tends to be worse with mismatches. Nevertheless, the simulated value of IIP3 is still 5dB higher than the largest IIP3 without the linearization method as will be shown later (in Fig. 14).

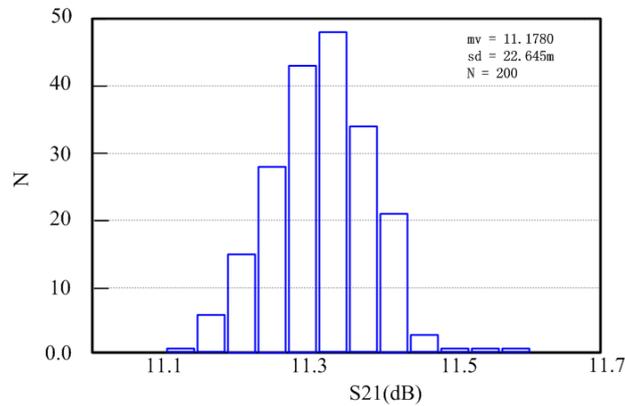


Fig. 8. Monte Carlo simulation results of S21.

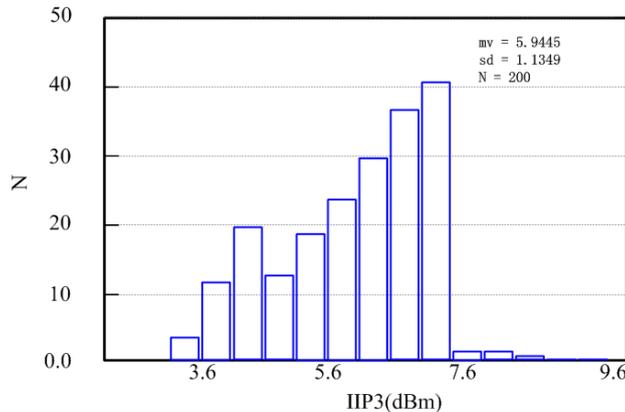


Fig. 9. Monte Carlo simulation results of IIP3.

#### 4. Simulation Results and Discussion

The proposed LNA was simulated using Cadence with CHRT 0.18  $\mu\text{m}$  RF process. By employing the folded-cascode topology, the supply voltage of the LNA can be reduced by one transistor overdrive. To satisfy the requirements for wideband matching and low-voltage operation, the supply voltage suitable for this LNA can reduce to 1V. However, for similar circuits in Refs. 15. and 19. , a supply voltage higher than 1V is needed. In order to reduce the power consumption, the width of M1b was chosen to very small.

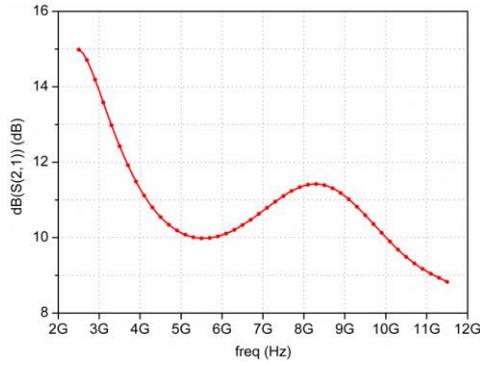


Fig. 10. Power gain (S21).

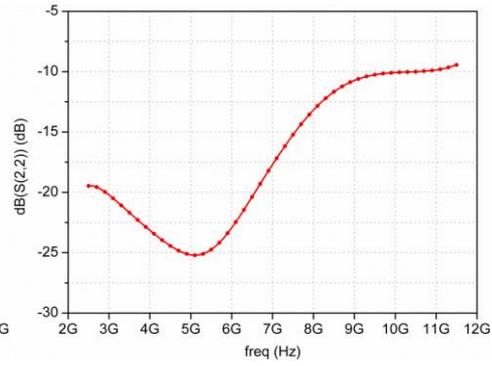


Fig. 11. Output reflection coefficient (S22).

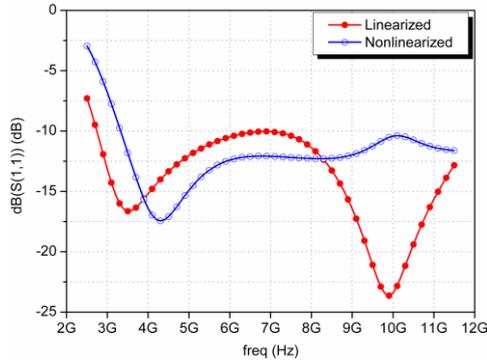


Fig. 12. Input reflection coefficient (S11).

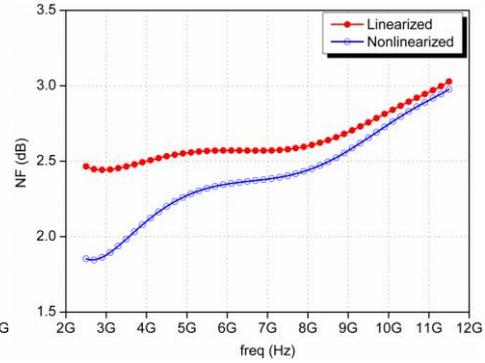


Fig. 13. NF of the proposed LNA.

In the design of the proposed CG-LNA, we chose  $W_{m1a}=4*28\mu\text{m}$ ,  $W_{m1b}=20\mu\text{m}$ ,  $W_{m2}=4*16\mu\text{m}$ ,  $W_{mB}=W_{mF}=4*13\mu\text{m}$ ,  $C1=1.0\text{pF}$ ,  $L1=1.8\text{nH}$ ,  $Ls=4.8\text{nH}$ ,  $Ld=1.93\text{nH}$ ,  $Lc=9.2\text{nH}$ ,  $Vb1=0.68\text{V}$ ,  $Vb2=0.79\text{V}$ . The maximum power gain is 15.0dB at 2.5GHz as shown in Fig. 10. The output reflection coefficient S22 and input reflection coefficient S11 are less than -10.7dB over the frequency range from 2.5GHz to 11.5GHz which are shown in Fig. 11 and Fig. 12, respectively. The NF is 1.8~2.9dB across the frequency band of interest as shown in Fig. 13. The isolation is less than -30dB. The pre-layout simulation indicates that the IIP3 improvement greater than -2.1dBm is achieved in the worst case at 4.5GHz, and an IIP3 of 6.2dBm is obtained at 8GHz as shown in Table 1

and Fig. 14. The post-distortion technique can improve the IIP3 by 5~10dB. Figure 15 shows the microphotography of the fabricated circuit with a chip area of 1.0\*1.1 mm<sup>2</sup> including the pads. Operated under a supply voltage of 1V, the post-layout simulation shows that the LNA consumes a DC power of 5.4mW and the IIP3 of 5.6dBm at 8GHz.

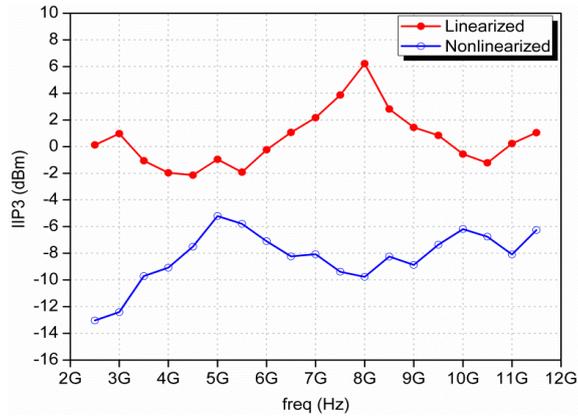


Fig. 14. Simulated IIP3 of CG-LNA with and without linearization, using 100MHz spacing two-tone with -20 dBm power level.

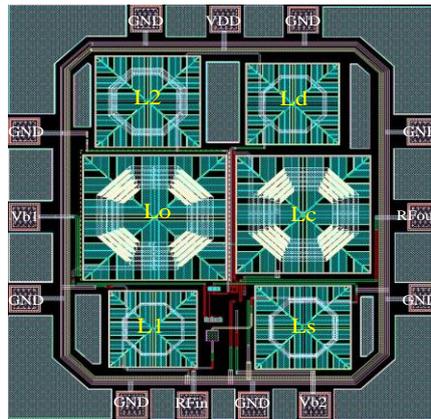


Fig. 15. Microphotograph of the proposed LNA.

Table 2 summarizes the performance of the proposed CG-LNA and comparison with the performances of some reported LNAs in the literature. From the data given in the table can be seen that the frequency range of the proposed LNA over 2.5GHz-11.5GHz due to embed a band-pass LC filter in the folded-cascode circuit, and full coverage of the maximum UWB standard. Moreover, the S11 are less than -10dB in the whole working bandwidth, it shows that the LNA possesses good input impedance matching within the entire 9GHz band. A post-distortion (PD) technique employing an auxiliary transistor is applied in the transconductance stage to improve the linearity, and the input third-order

intercept point (IIP3) reached 5.6dBm at 8GHz. The noise figure (NF) is lower than 4.0dB. The proposed UWB LNA achieves comparable IIP3 and its NF is even less than the one in the condition of the best linearity in Refs. 14 and 15. The LNA consumes 5.4mW power under a 1V supply voltage.

Table 2. Performance Summary and Comparison of the Recently Reported Broadband LNAs.

Ref	BW [GHz]	NF [dB]	S11 [dB]	S21 [max]	IIP3 [dBm]	Power [mW]	FOM I	FOM II	Tech. [um]	Topology
[1. ]	3.1-5.0	4.7-5.0	<-12.7	11.5	-8.0	5.7	0.24	0.16	0.18	Feedback
[10. ]	0.2-3.8	2.8-3.4	<-9	19.0	-4.2	5.7	5.66	2.15	0.13	CG-CS
[11. ]	2.3-6.0	4.8	<-7	12.7	10.6	8.3	0.95	10.9	0.13	Reuse-CS
[13. ]	0.2-5.2	3.5	--	15.6	0	21	1.16	1.16	0.065	Balun-CG
[14. ]	7.2-9.1	3.9-4.7	<-9	10.0	2.0	16	0.26	0.41	0.18	Cascade
[15. ]	2.5-10.0	2.7-3.3	<-10.2	10.0	3.5-9	2.6	6.6	36.5	0.13	Folded-CG-PD
[19. ]	3.1-10.6	2.1-2.9	<-9.9	16.5	-6.0	9	7.16	1.80	0.13	Feedback
This work <sup>a</sup>	2.5-11.5	1.8-2.9	<-10.7	15.0	6.2	5.3	10.9	45.4	0.18	Folded-CG-PD
This work <sup>b</sup>	2.5-11.5	3.2-4.0	<-10.0	12.8	5.6	5.4	5.64	20.5	0.18	Folded-CG-PD

a: the pre-layout simulation

b: the post-layout simulation

For the comparison of different topologies, we include two figures of merit (FOMs) in Table 2:

$$FOM\_I = \frac{Gain_{ave} [abs] \times BW [GHz]}{P_{dc} [mW] \times (F_{ave} - 1)} \quad (36)$$

$$FOM\_II = \frac{IIP3_{ave} [mW] \times Gain_{ave} [abs] \times BW [GHz]}{P_{dc} [mW] \times (F_{ave} - 1)} \quad (37)$$

where  $Gain_{ave}$  is the average gain,  $F_{ave}$  is the average noise factor over the frequency range, and  $P_{dc}$  is the power consumption of the LNA core.

From Eq. (36) and Eq. (37), the  $FOM\_I$  and  $FOM\_II$  are synthetically evaluating coefficient about LNA, the higher the value, the better the combination property.  $FOM\_I$ ,<sup>20</sup> which does not include linearity, and  $FOM\_II$ ,<sup>21</sup> which includes linearity,

From Table 2, our LNA also exhibits comparable  $FOM\_I$ , and has much better  $FOM\_II$  when compared to the other UWB LNAs. Therefore, through the comparison table, proved the proposed UWB LNA has excellent comprehensive performance even under an extremely low supply voltage.

Finally, we consider the stability of the proposed LNA circuit. The necessary and sufficient condition of amplifier is:

$$\begin{cases} k_0 > 1 \\ |\Delta| < 1 \end{cases} \quad (38)$$

where  $k_0$  is stability discriminant factor,  $\Delta$  and  $k_0$  can be calculated by:

$$\Delta = S_{11} \cdot S_{22} - S_{21} \cdot S_{12} \quad (39)$$

$$k_0 = \frac{1 - |S_{11}|^2 - |S_{12}|^2 + |\Delta|^2}{2|S_{12}||S_{21}|} \quad (40)$$

The corresponding parameters of our proposed novel CG-LNA is calculated, it can achieve stability condition.

## 5. Conclusions

In this paper, a low-voltage highly linear CMOS LNA has been proposed. The post-layout simulation results show that the designed LNA achieves a 5.6dBm IIP3 peak, a maximum gain of 12.8dB, and consumes 5.4mW power, under a 1V supply voltage. The proposed post-linearization technique improves the IIP3 by 5~10dB. The proposed LNA can be used in low-voltage wideband receivers for multi-standard systems such as UWB, Bluetooth, WLAN, ZigBee, WiMAX, etc. It is particularly suitable for high-speed mobile applications because of its high linearity.

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