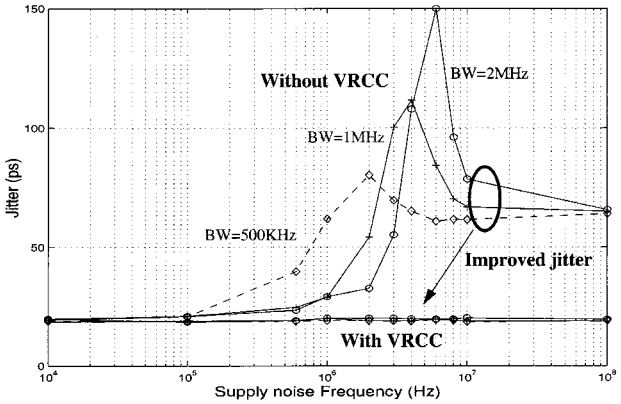

Fig. 15. PLL jitter having 500 K, 1 M, and 2 MHz loop bandwidth (with and without VRCC).

TABLE I
SNI–PLL PERFORMANCE SUMMARY USING CIRCUIT MODEL AND BEHAVIORAL MODEL

Specifications	0.35um CMOS circuit model	0.35um CMOS behavioral model
Cycle-to-Cycle jitter	$\pm 8ps$	$\pm 12ps$
Initial Lock In time	$10us$	$10us$
VCO tuning range	120MHz~800MHz	120MHz~800MHz
Vdd jump of 600mVpp	$\pm 80ps$ (with VRCC) $\pm 230ps$ (w/o VRCC)	$\pm 20ps$ (with VRCC) $\pm 220ps$ (w/o VRCC)
PLL jitter AC Power-Supply Sensitivity	$\pm 80ps$ (with VRCC) $\pm 600ps$ (w/o VRCC) at 20MHz/600mV Square wave	$\pm 21ps$ (with VRCC) $\pm 110ps$ (w/o VRCC) at 20MHz/600mV Square wave
CPU time of locking process	21700 sec.	610 sec.
CPU time of jitter simulation with a quiet supply	6050 sec.	220 sec.
CPU time of jitter simulation with a supply transient	6165 sec.	314 sec.

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Low-Power Fully Differential CMOS Filter for Video Frequencies

Yichuang Sun and Chris Hill

***Abstract*—This brief describes a new low-power fully differential second-order continuous-time low-pass filter for use at video frequencies. The filter uses a single active device in combination with MOSFET resistors and grounded capacitors to achieve very low-power consumption and large dynamic range. The ideal integrator is realized using an internally compensated op-amp consisting of only current mirrors and voltage buffers, while the lossy integrator is implemented by a single passive *RC* circuit. The filter has been simulated using a CMOS process. Results show that with a single 5-V power supply, cutoff frequency can be tuned from 3.5 to 8 MHz, dynamic range is better than 67 dB and power consumption is less than 1.7 mW.**

***Index Terms*—Active filters, analog circuits, CMOS circuits, low power design, op-amp.**

I. INTRODUCTION

In recent years continuous-time filters have played an increasingly important role in low-power high-frequency signal processing applications. Analogue filters often have much lower power consumption and require less chip area than a digital filter with the same characteristics. One approach to analogue filter design which is particularly well established is the MOSFET-C filters [1], [2]. MOSFET-C filters generally use op-amps embedded in *RC* circuits. This limits the high frequency performance of the circuit due to the limited bandwidth of the op-amp. Recent attempts to overcome this problem include the use of a BiCMOS process to produce an op-amp with a very large bandwidth [3] and use of alternative active elements such as a current conveyor [4]. So far in most continuous-time filter designs, multiple active devices have been used. This has limited the performance of power consumption and chip size and may not be suitable for application in stringent portable equipment.

This brief presents a design which takes advantage of the frequency response of an internally compensated op-amp to produce an integrator in a manner similar to that used in active-R filters [5]. To achieve low power consumption, small chip area and large dynamic range, only one amplifier is used for the second-order filter and the lossy integrator is realized using a simple MOSFET-C circuit. Compared with traditional two integrator loop filter designs that use at least two op-amps, the new realization requires only one op-amp. The filter is different from traditional single op-amp filters in that it is integrator based. It also differs from active-R filters since it uses the capacitor for the lossy integrator.

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The op-amp consists of only voltage buffers and current mirrors, thus simplifying the design and aiding integration.

The primary aims in the design of the filter are summarized below:

1) power consumption as low as possible;
2) design readily adaptable to integration: The design should have few or preferably no resistors in the filter signal paths and small capacitors, ideally grounded in order to minimize the effects of parasitics.
3) total harmonic distortion below 1%;
4) dynamic range greater than 60 dB;
5) implementation in a CMOS process;
6) tuneable cutoff frequency.

The brief is laid out as follows; Section II discusses filter structures; Section III examines practical aspects of the design and presents the transistor level design; and simulation results are given in Section IV followed by conclusions in Section V.

II. Filter Structure

Fig. 1 shows the structure of a commonly used second-order low-pass filter [6]. The circuit is comprised of three elements; an integrator, a lossy integrator, and a summing junction. If the circuit has unity feedback, the transfer characteristic of the filter can be derived as

$$\frac{V_{O2}(s)}{V_I(s)} = \frac{1}{s^2\tau_1\tau_2 + s\tau_1 + 1} = \frac{\omega_0^2}{s^2 + s\frac{\omega_0}{Q} + \omega_0^2} \tag{1}$$

giving the quality factor

$$Q = \left(\frac{\tau_2}{\tau_1}\right)^{1/2} \tag{2}$$

and the cutoff angular frequency

$$\omega_0 = \frac{1}{(\tau_1\tau_2)^{1/2}}. \tag{3}$$

The dc gain of the filter is equal to one.

From (3) it can be seen that variation of the cutoff frequency can be achieved by altering the value of the product $\tau_1\tau_2$. However, in order to maintain the Q of the filter at a constant level τ_2/τ_1 must remain a constant, i.e.

$$\frac{\tau_2}{\tau_1} = k. \tag{4}$$

This implies that the proportional adjustment must be the same for both time constants. It is also possible to have tuneable Q with fixed ω_0. This can be achieved by changing τ_2 and τ_1 with the same amount but opposite direction.

III. Implementation

Inspection of Fig. 1 shows that if a simple MOSFET-C stage is used as the lossy integrator only one active element is required to realize the ideal integrator and summer. The realization of Fig. 1 uses an internally compensated op-amp as the ideal integrator and the lossy integrator is synthesised with a simple *RC* circuit, as shown in Fig. 2. Compared with traditional two integrator loop filter designs that use at least two op-amps, the new realization requires only one op-amp. It should thus have reduced power consumption, reduced chip size and increased dynamic range. The filter in Fig. 2 is different from traditional single op-amp filters which use an op-amp embedded in a *RC* network and are not integrator based. It also differs from active-R filters since it uses the capacitor for the lossy integrator. The op-amp integrator has a differential input and its output impedance is low and not too dependent on frequency. In order to support a fully differential structure and also to minimize the distortion due to the MOSFET resistors [1] the op-amp must have two pairs of differential inputs and a pair of balanced output.

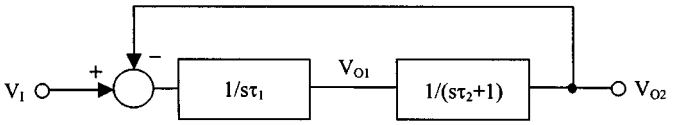

Fig. 1. Second-order filter structure.

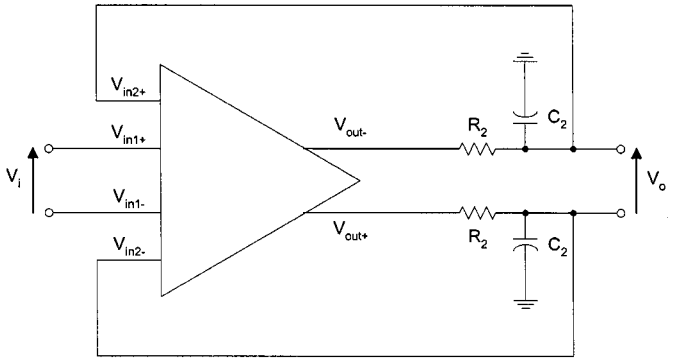

Fig. 2. Second-order op-amp MOSFET-C filter.

A. 4-Input 2-Output Op-Amp

Any op-amp is essentially a three stage amplifier: a differential input stage which is usually a transconductor; a transimpedance voltage amplification stage, with dominant pole compensation; and a buffer to lower the output impedance. The requirements of this particular design differ from a standard op-amp in two important ways: the input stage must be able to support a wide range of input voltage without clipping and the gain of the op-amp must be well controlled and tuneable, with respect to frequency. The design chosen is shown in Fig. 3. The structure is based on a number of interconnected current conveyors, each driving a resistance to control the transconductance of the input stage. In order to aid integration the design uses only two different circuit elements: voltage buffers and current mirrors as shown in Fig. 4. Because of the square law nature of the transistors the buffers possess good linearity and a maximum output current four times the bias current, giving good efficiency. In order to improve the output impedance of the current mirrors the output is via cascode transistors M3 which are biased from analogue ground.

If the output impedance of the current mirrors and the input impedance of the buffers are both sufficiently high, then the circuit will behave like an ideal integrator and have a transfer characteristic of

$$T_1(s) = \frac{g_m}{sC_1} \tag{5}$$

where g_m is the transconductance of the input stage given by

$$g_m = \frac{2}{R_1 + 2R_O} \tag{6}$$

where R_O is the output impedance of the buffers at the input. The output impedance of the buffers is desired to be as low as possible, as the presence of R_O limits the tuning range, especially at low values of R_1. For this reason, transistors M3 and M4 are chosen to be quite large. Simulation of this circuit shows R_O to be close to 3.5 kΩ.

Equation (4) requires that the same degree of tuning is applied to both time constants, i.e., $R_1 = R_2$ and the output impedance of the op-amp should equal $2R_O$. This is achieved by reducing the bias current at the

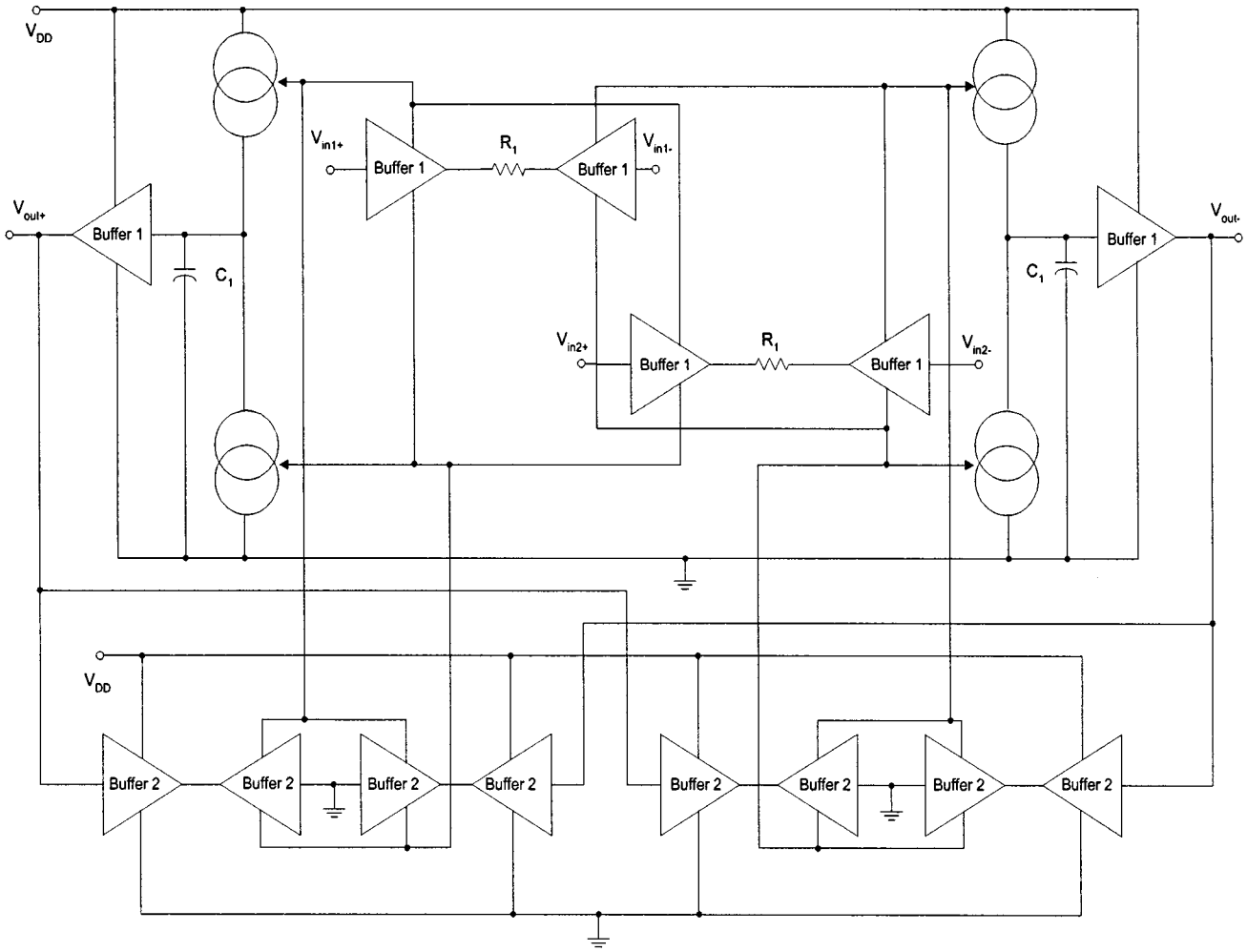

Fig. 3. Op-amp structure.

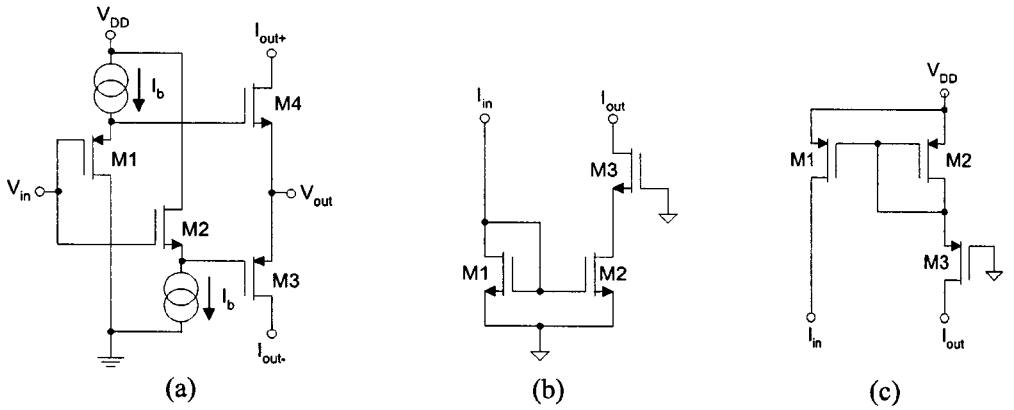

Fig. 4. Components of op-amp circuit. (a) Buffer. (b) N-channel mirror. (c) P-channel mirror.

outputs by a factor of 4, making the transfer characteristic of the lossy *RC* integrator

$$T_2(s) = \frac{1}{sC_2(R_2 + 2R_O) + 1}. \tag{7}$$

The dc voltage at the output of the op-amp is controlled by a common mode feedback network in order to provide the balanced output necessary to drive the MOSFET resistors. The common mode feedback circuit consists of eight buffers with dimensions different from the buffers at the input and output of the op-amp. The dc voltage at the op-amp output is kept at 2.5 V. Dimensions for transistors used are given in Table I.

B. Passive Components

The tuning range of the MOSFET resistors is very poor with a 5-V power supply and also conflicts with linear range requirements. This can be increased by adding further transistors in parallel [3]. This technique is illustrated in Fig. 5. Each MOSFET has its gate connected to either the tuning voltage $V_{\rm tune}$ or to ground effectively removing it from

TABLE I
TRANSISTOR DIMENSIONS AND BIAS CURRENTS

	M1 (μm)	M2 (μm)	M3 (μm)	M4 (μm)	I_b (μA)
Buffer 1	50/2	20/2	100/2	40/2	10 (input stage) 2.5 (output stage)
Buffer 2	12/2	5/2	24/2	10/2	2.5
N-Mirror	50/2	50/2	50/2	-	-
P-Mirror	120/2	120/2	120/2	-	-

TABLE II
DETAILS OF MOSFET RESISTORS AND PREDICTED CUTOFF FREQUENCIES

	Transistor dimensions	Maximum resistance (kΩ)	Minimum resistance (kΩ)	f_0 (MHz)
R_{nA}	2/2	39.2@V_{tune} = 4V	19.2@V_{tune} = 5V	2.4 to 5.9
R_{nB}	3/2	22.5@V_{tune} = 4V	8.2@V_{tune} = 5V	4.1 to 8

TABLE III
SUMMARY OF FILTER PERFORMANCE

Tuning voltage	f_0 (MHz)	Dynamic range (dB)	Power consumption (mW)	THD (%)
$V_{C1} = V_{tune}$, $V_{C2} = 0$	3.4 to 6.2	>67dB	1.68	<0.8%
$V_{C1} = 0$, $V_{C2} = V_{tune}$	5.0 to 8.0	>70dB	1.68	<0.3%

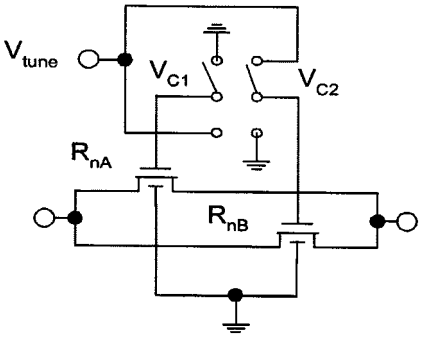

Fig. 5. Scheme for extending tuning range of MOSFET resistors.

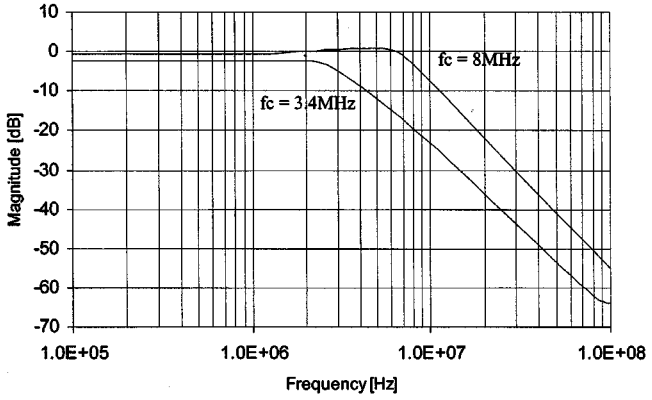

Fig. 6. Frequency response of filter (dB), showing the maximum extent of the tuning range.

the circuit. This design uses two parallel MOSFETs to give two overlapping tuning ranges, however additional transistors may be added to further increase the tuning range if desired.

In order to simplify the design and satisfy the conditions imposed in Section II the resistors used have identical values for R_1 and R_2. This leads to a convenient 4:1 ratio for C_1 and C_2 to achieve a Butterworth response ($Q = 1/\sqrt{2}$). Values chosen for this filter are 4 and 1 pF, respectively. Details of the resistors used are shown in Table II, together with predicted cutoff frequencies.

There can be other design procedures. For example, we may choose $C_1 = C_2$ and $R_1 = 4R_2$. The output impedance of the op-amp should then be equal to $R_O/2$.

IV. SIMULATION RESULTS

The filter was simulated using a 2-μm Level 2 CMOS process with $k_{\rm on} = 53.6\ \mu$A/V^2, $k_{\rm op} = 21.05\ \mu$A/V^2, $V_{\rm Tn} = 0.855$ V, and $V_{\rm Tp} = -0.8112$ V. The stimulated frequency response of the filter is shown in Fig. 6 and details of cutoff frequencies are shown in Table III. It can be observed that the upper cutoff frequencies match closely that predicted in Table II in Section III-B, although the lower cutoff frequencies are slightly higher than expected. It can also be seen that at lower bias voltages the dc gain drops by up to 2.4 dB. Both these effects are due to the finite output impedance of the current mirrors limiting the open loop gain of the op-amp. It can be noted that the Q of the circuit is slightly higher than expected, due to excess phase in the integrator.

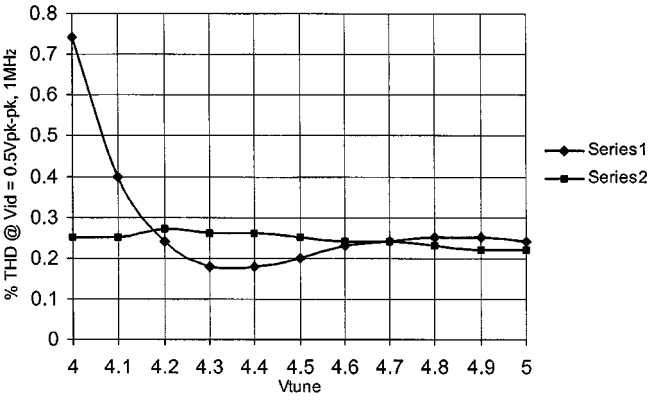

Fig. 7. THD (%) as a function of $V_{\rm tune}$ for a 1MHz 500-mV$_{\rm pk-pk}$ differential input signal. Series 1: $V_{C1} = V_{\rm tune}$; $V_{C2} = 0$ V. Series 2: $V_{C1} = 0$ V; $V_{C2} = V_{\rm tune}$.

Dynamic range was simulated using the definition of

$$\mathrm{DR} = 20 \log \left[\frac{V_{\max}}{(V_{\mathrm{ni}}^2)^{1/2}} \right] \tag{8}$$

where $V_{\max}$ is the input level where THD $= 1\%$ and $(V_{\mathrm{ni}}^2)^{1/2}$ is the mean-square-root input noise integrated over the bandwidth of the circuit. Simulation results show the DR to be in excess of 67 dB over the entire tuning range. As expected the DR increases as V_{tune} increases, due to increased linear range and reduced resistance in series with the input. Simulation also shows that power consumption of the filter is less than 1.7 mW, which is very low for two pole filters. Distortion performance is shown in Fig. 7 as a function of V_{tune} for a 1-MHz 500-$\mathrm{mV_{pk-pk}}$ differential input signal. Results are shown for both tuning ranges. A summary of simulated dynamic range, power consumption and distortion is given in Table III.

V. Conclusions

Presented in this brief is a differential second-order filter suitable for full integration in a standard CMOS process. The filter uses a structure based on MOSFET resistors and a single op-amp in order to reduce the complexity and power consumption of the circuit. The filter contains only grounded capacitors so as to minimize parasitic effects. Even order nonlinearities are cancelled by the use of a fully differential structure. Power consumption for the circuit is less than 1.7 mW. The filter cutoff frequency can be adjusted over one octave and the high impedance tuning port eliminates the need for a low impedance tuning voltage. A technique is described which overcomes the inherently poor tuning range of the MOSFET resistors.

This brief has verified the proposed ideas. Further work is underway to consider low supply voltage and high-Q filter design using sub-micron CMOS technology; quantify the chip area by practical implementation, although it is generally known that a single-amplifier biquad has smaller chip size than an multiple-amplifier biquad, as claimed in the brief; and evaluate other practical performances such as mismatch effects.

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CFOA Based Inverting Amplifier Bandwidth Enhancement

J. Bayard

***Abstract*—A theoretical study of the high frequency characteristic of an inverting amplifier based on a current feedback operational amplifier is presented. It is shown that the amplifier bandwidth and step response can be improved using a pole–zero compensation technique. Simulation and experimental results agree with the theory.**

***Index Terms*—Current feedback operational amplifier.**

I. Introduction

Compared with their voltage mode counterparts, current feedback operational amplifiers (CFOAs) have a wider bandwidth and also a higher slew rate. So, CFOA-based amplifiers have a higher frequency response than that of voltage mode operational amplifiers and are increasingly used in analog signal processing [1]–[8]. A study on CFOA-based noninverting amplifiers has already been described [9]. So, in this brief we will only focus on CFOA-based inverting amplifiers. We will demonstrate that their good high frequency response can be further improved by choosing an optimal value for the feedback resistor and by using a pole zero compensation technique.

II. Feedback Resistor Optimization

The CFOA equivalent circuit is shown in Fig. 1 and the topology for a CFOA-based inverting amplifier is shown in Fig. 2, where for now we assume that $C_1 = C_2 = 0$. For an ideal CFOA ($i_y = 0$, $i_z = i_x$, $v_x = v_y$ and $v_0 = v_z$) a nodal analysis leads to the following closed-loop gain:

$$\frac{v_0}{v_i} = -\frac{R_2}{R_1}. \tag{1}$$

This value is a good approximation of the amplifier response for the lowest frequencies but not for higher frequencies where the simple approach, assuming an ideal CFOA, fails. To understand the high frequency response of CFOA-based amplifiers, a two-pole model can be used to describe the open-loop transfer function

$$v_0 = \frac{i_x}{(1+\tau s)} \frac{R_T}{(1+\tau_1 s)}. \tag{2}$$

The dominant pole $\omega_1 = 1/\tau_1$ is due to the current source output impedance. The time constant τ_1 is equal to $R_T C_T$ where R_T is the current source output resistance and C_T the parasitic capacitance on the node. The second pole τ is due to the CFOA first stage current mirrors. Taking into account (2) the closed-loop gain becomes a two-pole characteristic equation

$$\frac{v_0}{v_i} = -\frac{R_2}{R_1} \frac{1}{R_2 \tau C_T s^2 + R_2 \left(C_T + \frac{\tau}{R_T} \right) s + 1 + \frac{R_2}{R_T}}. \tag{3}$$

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